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Engineering high-performance vertical cavity lasers SAND--96-2789C

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Abstract - The cw and high-speed performance of vertical cavity surface emitting laser diodes (VCSELs) are affected by both electrical and optical issues arising from the geometry and fabrication of these devices. Structures with low resistance semiconductor mirrors and Al-oxide confinement layers address these issues and have produced record performance including 50% power conversion efficiency and modulation bandwidths up to 20 GHz at small bias currents.

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A. Introduction

Vertical cavity surface emitting lasers (VCSELs)[1] exhibit a number of properties that make them attractive alternatives to conventional laser or light-emitting diodes. These attributes include compatibility with economical batch manufacturing using microelectronics methods; circular, low divergence, surface-normal output beams from one or two-dimensional arrays that simplify system requirements for optics and packaging; and properties derived from their small size such as low threshold current, single longitudinal mode operation, and intrinsic high speed. Despite these advantages, earlier devices exhibited some performance problems associated with excess electrical and optical losses. This paper reviews our efforts to reduce these losses in order to improve device efficiency. Section B reviews heterojunction grading to reduce electrical losses, and section C summarizes work on oxide-confinement for reducing optical losses. Section D briefly highlights a theoretical treatment for determining the maximum power conversion efficiency. A secondary consequence of the technology developed for high efficiency was enhancement of high speed operation as discussed in section E.

B. Electrical Losses: DBR Grading

The high reflectivity multilayer semiconductor mirrors in many VCSELs also provide a path for current injection. Heterojunctions between high and low index semiconductors usually have large energy band offsets that form potential barriers which inhibit carrier flow. This problem can be particularly serious in p-type mirrors or distributed Bragg reflectors (DBRs) because the large hole mass reduces tunneling and thermionic emission. While the heterojunction resistance can be reduced by increased doping, one cannot arbitrarily increase doping densities throughout the structure, because doing so also increases optical absorption. A more effective solution is alloy grading at interfaces, often in conjunction with varied doping profiles such as increased doping at interfaces[2], delta doping[3], and modulation doping[4]. Initial demonstrations of interface grading used a single narrow region of intermediate alloy composition inserted between the high and low index layers[5]. Such step grading profiles substantially reduce the differential resistance at large electrical biases, but typically result in DBR voltage drops of 1 V or more even at modest current densities of 1 kA/cm².

More continuous variations in alloy composition across the interface further reduce DBR voltage. In conventional molecular beam epitaxy (MBE), the alloy composition changes discontinuously between values determined by the fixed fluxes of a limited number of Al and Ga effusion cells. Alternatively, superlattices with effective intermediate compositions can be created by alternating thin layers of just two compositions. The latter technique provides the ability to vary the effective alloy composition using a minimum number of cells simply by varying the duty cycle of the superlattice. The period of such superlattices, typically ~2 nm, should be less than or comparable to the carrier tunneling length which can be as short as ~0.3 nm for holes due to their large effective masses. Thus superlattice grading has the

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disadvantage of requiring thousands of shutter operations per VCSEL growth. True alloy grading can also be achieved by MBE through variation of the cell temperatures[6]. The cell temperature variation technique was used to realize the grading configuration shown in Figure 1a[7]. The DBR composition was ramped continuously from $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ to $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ and back again to $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ by cyclically varying the Al and Ga effusion cell temperatures in complementary fashion. Three piecewise linear segments were used at each interface. The remaining potential barriers resulting from this grading profile are small enough that the current-voltage relationship is linear for such mirrors.

In addition to the resistance of DBRs to vertical current flow, other properties including electrical lateral resistance, thermal resistance, and optical reflectivity must be considered in the design of DBR grading. If vertical electrical resistance is dominated by heterojunction barriers it can be reduced by long graded regions and less extreme composition variations, but these approaches degrade other properties. Intermediate alloy compositions have the lowest electrical and thermal conductivity, and optical reflectivity is highest for abrupt AlAs/GaAs heterojunctions. Thus the alloy grading should be concentrated at the approach to the high band gap material where it has the most benefit for reducing the vertical electrical resistance. This consideration motivates the grading profile shown in Figure 1b[8]. It has less alloy content in the flat regions as well as a more narrow transition region in between. Despite the steeper grade, this design when implemented with metalorganic chemical vapor deposition (MOCVD) had a lower resistance than the three segment per interface design grown by MBE. Important advantages that MOCVD offers over conventional MBE is easy grading of alloy composition and the use of carbon as a p-type dopant which has lower diffusivity and is more readily activated in AlAs than Be[9].

Figure 1. Two mirror grading designs used in the development of low resistance, high efficiency VCSELs. Design (a) was implemented with Be doped MBE using cell temperature variation to achieve alloy grading, and design (b) was implemented with C doped MOCVD. The solid line in the plots which can be read on the right axis as aluminum composition also show the nonequilibrium (zero field) valence band minimum hole energy with respect to the value for GaAs on the left axis. The equilibrium valence band potential with respect to the Fermi level is indicated with the dashed curve read against the left hand axis.

Other significant contributions to the voltage drop in VCSELs are the lateral spreading and contact resistances. Both contributions are accentuated in laterally contacted geometries,

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such as those used in top emitting devices. The points in Figure 2 show the measured device resistance for VCSELs defined by proton implantation. The two groups of points correspond to the three segment per interface and uniparabolic designs shown in Figure 1. Each group may be fitted with the expression[10] $R = R_L / (2\pi r) + R_V / (\pi r^2)$, where the first term accounts for the contact, lateral, and constriction contributions, and the second term accounts for the heterojunction resistance. The curves in Figure 2 are fits to experimental data using this equation. The fitting parameters are $R_L = 4.1$ and $1.0 \Omega\text{-mm}$ and $R_V = 2.6 \times 10^{-5}$ and $9.8 \times 10^{-6} \Omega\text{-cm}^2$ for the upper and lower curves, respectively. For both curves, the $1/r$ term dominates for device radii $r > 1 \mu\text{m}$ emphasizing the importance of reducing lateral, and contact resistance in top-emitting VCSELs. This is accomplished in part by the inclusion of an extra $\lambda/2$ layer of heavily doped GaAs at the surface of the MOVPE lasers with the uniparabolic mirror[8].

Fabrication also influences the lateral resistance of annularly contacted VCSEL structures. Damage caused by proton implant increases both bulk and contact resistivity. To minimize detrimental effects of the implant, the implant dose is made as low as possible. Excessive damage can be partially annealed in a furnace or through operation of the laser [11]. The sensitivity of contact resistance to implant damage can be reduced by increasing the doping level near the surface, for example by using beryllium delta doping in conjunction with thin InGaAs caps[10] or heavy carbon doping also permits high ($p > 5 \times 10^{19}$) in the cap.

Figure 2. Series resistance versus active region radius for proton implanted VCSELs with two DBR designs described in the text.

Figure 3. Light output power and voltage as a function of current drive for implant confined VCSELs. (a) Two large $30 \mu\text{m}$ diameter lasers show either up to 21% power conversion efficiency or threshold voltages as low as 1.47 V. (b) A smaller $8 \mu\text{m}$ diameter laser provides up to 4 mW of single-mode output power with nearly 40 dB of transverse mode suppression.

The incorporation of low resistance mirrors of the design shown in Figure 1b into InGaAs quantum well VCSELs grown by MOCVD and fabricated with proton implantation resulted in improved performance[12]. Large area devices exhibited record high power conversion efficiencies of 21% as shown in Figure 3a. However, this efficiency level was reached at a relatively high power of 12 mW which was much larger than the 1 mW level required for many applications of interest for VCSELs. While smaller VCSELs exhibited some useful properties such as single-mode powers over 4 mW as shown in Figure 3b, they did not reach the efficiency levels seen in large area devices. The primary source of this limitation was the anomalous scaling of threshold current with laser size as seen in Figure 4. For proton implanted devices, the minimum threshold current was obtained for lasers approximately 12 μm in diameter. Smaller lasers actually had increased threshold currents.

C. Optical Losses: Oxide Confinement

Increasing threshold current with decreasing laser size below $\sim 10 \mu\text{m}$ was attributed to the inadequacy of thermal lensing to laterally confine light to the unimplanted region in small lasers[13]. The VCSEL is a high Q, plane-plane resonator that allows substantial diffraction. This results in optical loss as the light migrates laterally into unpumped regions. Even small losses are important to VCSEL operation since losses must be less than the maximum roundtrip gain of $\sim 1\%$. As laser size decreases, the perimeter to area ratio increases and such peripheral losses begin to dominate, eventually driving up the threshold current. In order to scale VCSELs to small lateral dimensions, the optical field must be confined to the pumped region by built-in index structure stronger than that due to thermal lensing. Reports of very low threshold currents in small diameter, oxide-confined, planar VCSELs with dielectric mirrors[14] indicated that such lasers didn't suffer from the same diffraction limitations as implant-confined devices. The use of wet thermal oxidation to convert AlGaAs to an insulating, low index alumina film[15] had previously been applied to edge-emitting lasers.

Figure 4. The scaling of threshold current with VCSEL size for implant-confined (circles) and oxide-confined (squares) devices fabricated from the same wafer.

Figure 5. Scanning electron micrograph of a portion of a VCSEL's epitaxial structure showing varying lengths of oxide (dark) depending on AlGaAs composition.

In order to apply the oxide confinement to VCSELs with monolithic semiconductor mirrors, it was advantageous to develop a technique that limited the oxidation of high aluminum content layers in the majority of the upper mirror stack. It was found that the oxidation rate of AlGaAs was very sensitive to a few percent of gallium composition. By varying the composition from $x=0.92$ to 0.98 for example, specific layers of the mirror stack could be oxidized much further than others[16] as seen in Figure 5. This allowed one or more layers closest to the active region to be oxidized to constrict current and confine light while the majority of the mirror remained unaltered in order to conduct current. At small diameters, the threshold current of oxide-confined VCSELs was substantially less than that of implant-confined ones as plotted in Figure 4. This in combination with higher slope efficiencies resulted in high power conversion efficiencies even for small devices. An output power of

1 mW was generated with an electrical input of 2 mW for a 50% power conversion efficiency as shown in Figure 6[17] for a triple InGaAs quantum well VCSEL.

Figure 6. The output power (solid line) and voltage (dashed line) vs. current characteristics of an $\sim 8 \times 8 \mu\text{m}$ oxide confined VCSEL exhibiting 50% power conversion efficiency at the 1 mW level.

Figure 7. The normalized optimum PCE from equation (1) (solid curve) and the number of times threshold where it occurs from equation (2) (dashed curve) along with the normalized optimum DQE (dotted curve) as functions of the normalized loss voltage.

D. Theoretical efficiency limitations

The theoretical limits on electrical-to-optical power conversion efficiency (PCE), $\eta_{PC} = P/(IV)$, have been considered in a model where both the output power, P , and applied voltage, $V = V_d + IR$, are linearly dependent on the current, I [19]. Here R is the resistance and V_d is an idealized (extrapolated zero current) turn-on voltage. The result for the maximum PCE is

$$\eta_{PC,max} = \frac{V_\phi}{V_d} \eta_i \left(1 - \frac{2}{N}\right) \left(1 - \frac{1}{N}\right) \quad (1)$$

where η_i is the internal quantum efficiency, and the photon voltage is defined as $V_\phi \equiv hc/q\lambda$ in terms of the wavelength, λ , and the fundamental physical constants h , c , and q . The conditions for maximum PCE include an optimum gain region design and output transmission and operation at an optimal current, $I = NI_{th}$, at N times threshold current, I_{th} . The parameter N is related to a universal parameter, the loss voltage, $V_L = I_L R$, according to

$$N^2(N-2) = \frac{V_d}{V_L} \quad (2)$$

where I_L is Corzine's loss current[20]. The loss current is proportional to the internal loss of the laser and can be thought of as the threshold current for a similar diode with no output transmission and appropriately scaled gain region. So the maximum PCE is dependent on the product of the loss, L , and resistance which appears in the loss voltage, $V_L \propto LR$. A plot showing the dependence of the normalized maximum PCE and required operating current as a function of normalized loss voltage is shown in Figure 7.

E. High speed VCSELs

The developments implemented for high efficiency VCSELs also enhance high speed operation. Low resistance mirrors decrease parasitic RC time constants and improve the impedance match. Both low resistance mirrors and monolithic oxide-confined structures[16] promote operation to many times threshold prior to thermal rollover by lowering threshold currents and providing efficient operation. The oxide also provides good optical confinement for high photon densities.

Figure 8 shows a schematic cross section of a high speed VCSEL with a corresponding small signal equivalent circuit. Coplanar waveguide pads designed for on wafer probing were placed on a 5 μm thick polyimide to reduce the capacitance between the pad and the conducting substrate to approximately 50 fF. Initially, lasers were grown on n-type substrates and the mesa was not implanted. This approach resulted in InGaAs quantum well lasers with bandwidths up to 16 GHz [21] which exceeded the previous reported maximum bandwidth for implant confined VCSELs[22]. However, such lasers as well as comparable GaAs quantum well, 850 nm lasers exhibited poles in the electrical response in the 1-5 GHz range. Parametric measurements and modeling indicated that this was due to the high capacitance of the thin oxide layer. The device capacitance was reduced by implanting the mesa area lying outside the active region. The non-radiative recombination associated with the deep implant damage may also reduce the charge storage associated with diffusion underneath the oxide region. Additionally, the top mirror was made n-type requiring growth on a p-type substrate. The low lateral resistance of the top n-type mirror reduces the overall resistance and promotes more uniform current injection that extends single mode operation.

Figure 8. Schematic cross section of high speed VCSEL structure with equivalent circuit.

Figure 9. Fiber coupled power (solid) and voltage (dashed) vs. bias current for (a) $4 \times 4 \mu\text{m}^2$ and (b) $8 \times 8 \mu\text{m}^2$ high speed VCSELs. The markers in (b) indicate bias and emitter coupled logic drive levels from a 50 Ω source for signals shown in Figure 12a (squares) and 12b (circles).

The resulting laser diodes, based on five GaAs quantum wells, feature DC characteristics that are important for high speed modulation. Figure 9a shows quasi-static light-current and voltage-current characteristics indicating a submilliampere threshold current, operation to several times threshold before thermal rollover, good efficiency coupled into the fiber, and moderate resistance for this size of device ($\sim 4 \times 4 \mu\text{m}^2$). The laser also operated in the fundamental mode to approximately 4 mA as necessary to obtain increasing photon densities in

the mode. Other similar sized devices remained single-mode at all operating currents. The characteristics for a larger, multimode device ($\sim 8 \times 8 \mu\text{m}^2$) are shown in Figure 9b.

The small signal response of the 850 nm VCSELs as a function of bias current was measured using a calibrated vector network analyzer with on wafer probing and a 30 GHz photodetector connected through approximately 2 m of the multimode fiber. Figure 10 shows the modulation response of the lasers. The modulation response at various bias currents was fit with a traditional damped resonator model to extract the resonant frequency and equivalent damping frequency ($\gamma/2\pi$). These quantities for a $\sim 4 \times 4 \mu\text{m}^2$ laser with 0.5 mA threshold current are plotted in Figure 11a along with the -3dB bandwidth. At low bias currents, the bandwidth and resonant frequency increase in proportion to the square root of the current above threshold as expected from the conventional rate equation analysis. The rate of increase in this region yields a modulation current efficiency factor (MCEF) of 14.2 GHz/ $\sqrt{\text{mA}}$ which is slightly lower than the highest value we previously reported for oxide confined VCSELs with InGaAs quantum wells[21]. The resonant frequency increases steadily to 15 GHz at 2.7 mA and then becomes nearly constant. The -3dB bandwidth is as high as 21.5 GHz. The dependence of the damping rate on resonance frequency, as shown in Figure 11b, was examined to determine the intrinsic frequency response of the laser. A fit of the data for resonance frequencies below 15 GHz produced a K-factor of 0.159 ns corresponding to a maximum intrinsic bandwidth of 58 GHz. Damping rates for higher resonance frequencies fell

Figure 10. Frequency response of (a) single mode, $4 \times 4 \mu\text{m}^2$ and (b) multimode, $8 \times 8 \mu\text{m}^2$ VCSELs coupled to a high speed detector for various laser bias currents

Figure 11. (a) Resonance frequency (squares), -3dB frequency (circles), and equivalent damping frequency ($\gamma/2\pi$) (triangles) as a function of square root of current above threshold. (b) Fit of damping rate's (γ 's) parabolic dependence on resonance frequency to determine the intrinsic frequency response of the laser.

above this fit yielding a K-factor of 0.227 ns. The actual bandwidth is limited to less than 58 GHz by heating, multimode operation, and electrical circuit effects. Higher bandwidths should be achieved by combining better heating sinking, designs for extended single-mode operation, and fabrication on semi-insulating substrates to reduce pad capacitance.

Large signal, digital modulation experiments were also performed. Figure 3 shows eye diagrams during a 6 Gb/s test using $\sim 8 \times 8 \mu\text{m}^2$ multimode lasers driven with 2^7-1 pseudo-random bit sequence (PRBS) emitter-coupled logic (ECL) signals for two different bias levels as indicated in Figure 9b. When both drive levels are above threshold there is an open eye and rising and falling edges cross in the center as seen in Figure 12a. However, when the lower drive level falls below threshold, substantial pattern dependent jitter results as seen in Figure 12b. Under the latter bias conditions turn on delays range from 50 to 120 ps when the laser is off for 0.2 to 1.5 ns, respectively. Thus, despite the low threshold of these lasers, operation without prebias would be restricted to data rates less than approximately 1Gb/s. When properly biased and adjusted, bit error rates as low as 10^{-13} were observed in preliminary investigations at data rates of 12 Gb/s.

Figure 12. Eye diagram generated by 6 Gb/s digital modulation of a multimode VCSEL linked by 2 m of multimode fiber to a photodetector and ~ 9 dB inverting amplifier without filtering. The bias currents were (a) 4 mA and (b) 7 mA as illustrated in Figure 9b.

F. Conclusions

VCSEL performance has improved rapidly over the past decade and is currently being commercialized. Electrical loss issues and solutions discussed in this paper are pertinent to present commercial devices. Research devices have reached even higher levels of performance, and oxide confinement in particular has played a crucial role. Remaining issues to be addressed by future VCSEL device research include transverse mode control, carrier confinement, and acceptable performance at wavelengths beyond the 670-980 nm range.

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