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LATENT INTERFACE TRAPS AND 1/*f* NOISE IN IRRADIATED MOS DEVICES

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35-word Abstract

A delayed increase in 1/*f* noise is observed for pMOS transistors showing latent radiation-induced interface-trap buildup. The latent interface traps and increased noise appear to result from the same thermally activated process, likely involving hydrogen.

DISCLAIMER

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Summary

A strong correlation has been observed between MOS $1/f$ noise and O vacancies in the SiO_2 gate oxide [1]. Hydrogen-related defects are also common in irradiated MOS devices [2-6]. A particularly striking effect that has been attributed to hydrogen is very long term, delayed ("latent") interface-trap buildup in MOS transistors [6,7]. It has been proposed that latent interface-trap buildup occurs because the motion of protons released during irradiation can be retarded by interactions with O vacancies in the SiO_2 [6]. If so, one might expect low-frequency noise measurements to be sensitive to this hydrogen motion and/or to subsequent interactions at or near the Si/SiO_2 interface. We have performed a detailed comparison of time-dependent net-oxide and effective interface-trap densities with $1/f$ noise levels through irradiation and annealing for MOS transistors showing significant latent interface-trap buildup. We find a strong increase in $1/f$ noise that precedes the latent interface-trap buildup. These results suggest the increased noise may be due to defects in the near-interfacial oxide associated with the interactions of slowly transporting protons.

The devices in this study were 4 μm long, 32 μm wide pMOS transistors with 50 nm gate oxides manufactured by Oki Semiconductor, known from previous work to exhibit latent, thermally activated interface-trap buildup [7]. Radiation-induced net-oxide (ΔN_{ot}) and effective interface-trap (ΔN_{it}) charge densities were estimated via the subthreshold technique of Winokur et al. [8]. This method does not distinguish between the effects of "true" interface traps and fast border traps on MOS transistor subthreshold stretchout [6,9]. For that reason we refer to ΔN_{it} as the "effective" interface-trap charge density. Unfortunately, the Oki transistors used in this study do not have a separate substrate contact, so charge pumping techniques cannot be used to try to distinguish between interface and border trap effects, as has been done in some previous studies [5,6,9].

Noise measurements were performed at room temperature at various gate (V_g) and drain (V_d) biases with a HP 3562A Dynamic Signal Analyzer [10]. The background noise with $V_d = 0$ V was typically much lower than the device $1/f$ noise, and was subtracted to obtain the excess noise S_V. The normalized noise power spectral density $K \equiv S_V f(V_g - V_{th})^2 V_d^{-2}$ [1], where f is the frequency and V_{th} is the threshold voltage, was obtained by averaging values between 10 and 40 Hz. For all noise measurements shown, $S_V \sim 1/f^{\alpha}$, with $\alpha \approx 1.0 \pm 0.1$ [11]. Before irradiation, the value of the Hooge figure-of-merit $\alpha_H = S_V N_c f / V_d^2$ [$\approx K (\varepsilon_{ox}/t_{ox})(A/q)(V_g - V_{th})^{-1}$, where N_c is the number of carriers, ε_{ox} is the oxide dielectric constant, t_{ox} is the oxide thickness, A is the area, and $-q$ is the electronic charge] is $\sim (1.5 \pm 1.0) \times 10^{-7}$ for these devices, a level comparable to the low noise of JFETs [1,12]. This may indicate buried-channel (i.e., bulk) conduction in these pMOS devices [12], at least before radiation exposure. After preirradiation noise measurements, the devices were exposed to Co-60 γ-ray irradiation at $V_g = 6$ V and 25°C at 92 rad(SiO_2)/s. The devices were then subjected to various annealing treatments. The drain current and gate voltage were adjusted to maintain constant V_d and $V_g - V_{th}$ for noise measurements through the irradiation and annealing sequences to simplify comparisons with previous work and with noise models in the literature [1,10,12-16].

In Fig. 1 we show ΔN_{ot} and ΔN_{it} for a pMOS Oki transistor irradiated at $V_g = 6$ V, then annealed at various temperatures and biases. During irradiation (time $t < 800$ s), both ΔN_{ot} and ΔN_{it} increase significantly, as expected for these non-radiation-hardened devices [17]. Through 25°C anneal at 6 V ($800 \text{ s} < t < 6 \times 10^5$ s), ΔN_{ot} decreases logarithmically with anneal time [6,7,17]. Values of ΔN_{it} first decrease slightly after irradiation, and then increase near the end of the 25°C, 6 V anneal [6,7]. When the temperature is raised to 50°C ($t \sim 6 \times 10^5$ s) and higher, while maintaining 6 V bias, the decrease in ΔN_{ot} accelerates with increasing anneal time and temperature. In contrast, ΔN_{it} more than doubles between $t = 6 \times 10^5$ s (25°C) and $t = 2 \times 10^6$ s (100°C) before saturating, consistent with latent interface trap buildup [6,7]. When the temperature is raised to 175°C, ΔN_{it} decreases dramatically due to interface-trap annealing [18]. The decrease in ΔN_{it} continues when the bias is switched to −6 V at 175°C, while ΔN_{ot} increases slightly after this bias switch [6]. Upon cooling the devices to 100°C and returning to 6 V bias, ΔN_{it} increases slightly and ΔN_{ot} decreases again.

In Fig. 2 we compare the normalized $1/f$ noise and ΔN_{it} through the irradiation and anneal sequence of Fig. 1. These noise measurements were performed at $V_d = 0.4$ V and $V_g - V_{th} = -1$ V [13,14]. There is a remarkable correlation between K and ΔN_{it} in Fig. 2 throughout

the entire irradiation and anneal sequence, approximately of the form ln $K \sim \Delta N_{it}$. This is consistent with the observation that the noise of some pMOS power transistors correlates with ΔN_{it} [16], but contrasts with the close link between $1/f$ noise and oxide trap density seen in nMOS transistors [1,10,14]. However, the strong increase in K during the initial 25°C, 6 V anneal precedes the latent increase in ΔN_{it} in Fig. 2 by at least 4 x 10^5 s (~ 4.5 days). Moreover, K increases by a factor of ~ 50 for times between 2 x 10^5 s and 2 x 10^6 s, while ΔN_{it} increases by a factor of ~ 2.7. This approximately exponential increase in noise with increasing defect density is not predicted by any of the standard number or mobility fluctuation models of noise in MOS transistors [1,13,15]. So it does not appear to be just the increase in ΔN_{it} that causes the increased noise in these devices. However, the striking correlation between K and ΔN_{it} through the entire irradiation and anneal period in Fig. 2 certainly suggests a strong link between the *processes* that lead to the enhanced $1/f$ noise and latent interface-trap buildup and annealing in these devices.

In Fig. 3 we show ΔN_{ot} and ΔN_{it} for a second group of devices irradiated to 75 krad(SiO_2) at 25°C and annealed at ± 6 V bias at 100°C. At this higher annealing temperature, both the reduction in ΔN_{ot} and latent buildup of ΔN_{it} are accelerated [6,7]. Switching from positive to negative anneal bias increases the densities of both defect types; returning to positive bias decreases the densities of each [6]. In Fig. 4 noise measurements are compared to ΔN_{it} for this irradiation and anneal sequence. These noise measurements were performed at V_d = 0.2 V and $V_g - V_{th}$ = –2 V. (The specific bias conditions for the noise measurements did not affect the trends in the data, as verified by checking the response at several biases other than those reported here [11].)

We now compare the results of Figs. 2 and 4 during the initial 6 V anneal. Similar to Fig. 2, the strong increase in K in Fig. 4 precedes the increase in ΔN_{it}. However, the delay between the increase in noise and ΔN_{it} is only about 4000 s (~ 1.1 h) at 100°C in Fig. 4, compared to at least 4 x 10^5 s delay at the lower annealing temperatures in Fig. 2. The overall magnitudes of the increases in noise and effective interface-trap densities are otherwise similar in Figs. 2 and 4. Hence, the results of Figs. 2 and 4 strongly suggest that the latent interface-trap buildup and the increase in $1/f$ noise in these Oki transistors are due to a single thermally activated process. In previous work, the activation energy for latent interface-trap buildup in Oki transistors was estimated to be ~ 0.47 eV [10]. The similarity of the acceleration of the noise and latent interface trap buildup rates in Figs. 2 and 4 suggest this activation energy is also appropriate for describing the increased postirradiation $1/f$ noise in these devices. However, it is interesting that, at this lower annealing temperature, the $1/f$ noise level in Fig. 4 *decreases* when the anneal bias is switched to –6 V, then increases when the bias is returned to 6 V [14]. This is in contrast to ΔN_{ot} (Fig. 3) and ΔN_{it} (Figs. 3 and 4) which show the opposite pattern when the bias is switched. This reinforces our previous point that the same process leads to the increased $1/f$ noise and latent interface-trap buildup, but neither ΔN_{ot} or ΔN_{it} itself determines the noise level.

Recently, it has been suggested that the process that leads to latent interface-trap buildup in oxides having high concentrations of O vacancies in the SiO_2 gate oxide may be similar to the process by which conventional interface-trap buildup occurs in irradiated MOS transistors, only slower [6]. That is, radiation exposure releases hydrogen related species (e.g., protons) in the SiO_2, which begin to drift under a positive electric field to the Si/SiO_2 interface. In oxides with low O vacancy densities, protons can reach the interface in tens or hundreds of seconds, initiating the interface trap buildup process [2-6]. In oxides with higher O vacancy densities, like these Oki transistors, the protons appear to have their transport slowed, and may even be captured by shallow traps associated with the O vacancies [6]. Within the context of this model, the increase in $1/f$ noise in Figs. 2 and 4 may be caused in part by (1) a dramatic increase in the density of border traps and/or slow interface traps with energy levels and positions appropriate for metastably exchanging charge with the Si during the noise measurements, (2) an increase in the scattering rate associated with these defects, and/or (3) proton motion near the interface. It seems plausible that (1) and (2) would occur as protons begin to reach the near-interfacial region, capture an electron to form atomic hydrogen, with some ultimately reacting at the interface to form interface traps. The increase in noise may occur as the protons move into the near-interfacial region and begin creating new border traps [1,6,9], with the subsequent increase in interface traps occurring when the protons reach the interface and begin creating interface traps [2-6]. The hydrogen transport process

may also lead to a crossover from buried-channel to near-surface conduction in these devices [12], as hydrogen passivates some boron dopants in the Si surface layer. During these processes, the motion of the protons themselves may also contribute to the noise. The bias switching response of the noise, especially in Fig. 4, suggests at least some of these processes are reversible, especially for moderate anneal temperatures. This will be discussed in more detail in the full paper for these and other devices showing similar effects.

In conclusion, we have found that the long-term delayed increase in $1/f$ noise and latent interface-trap buildup in irradiated Oki pMOS transistors with high O vacancy densities are evidently caused by a common thermally activated process. The results are consistent with recent work attributing latent interface-trap buildup to retarded proton motion in oxides with high O vacancy density [6]. These results suggest a significant role for hydrogen-related species not only in interface trap formation in irradiated MOS devices, but also in increasing their $1/f$ noise. This is a potentially significant performance and reliability concern for non-radiation-hardened MOS devices exposed to ionizing radiation over long periods of time. This may also be a concern for the operation of pMOS dosimeters under positive bias, where $1/f$ noise can limit sensitivity [19], as we will also discuss in the full paper.

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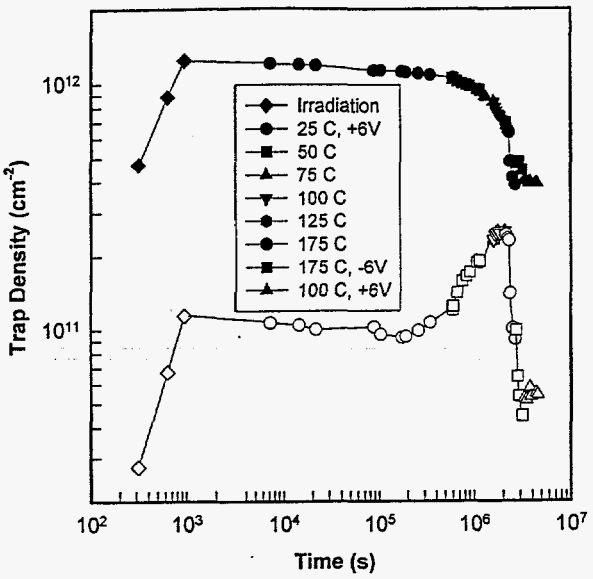

Fig. 1: Net oxide-trap (solid symbols) and effective interface-trap (open symbols) charge densities for pMOS Oki transistors with 50 nm oxides irradiated at 25°C to 25, 50, and 75 krad(SiO_2) at V_g = 6 V (diamonds), and then annealed at ± 6 V bias for various times and temperatures.

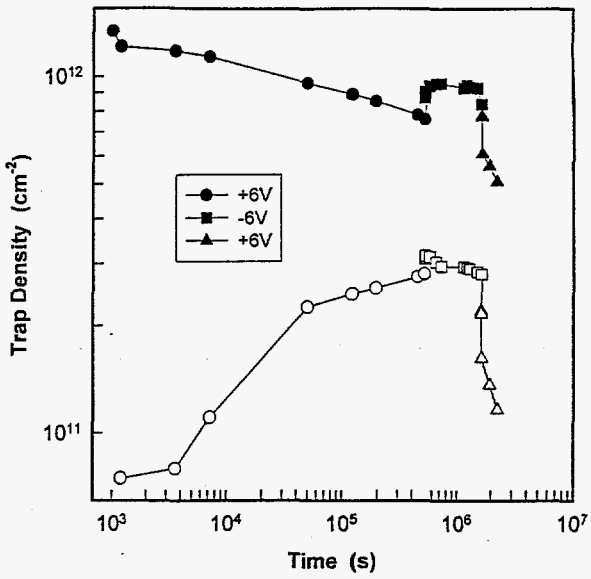

Fig. 3: Net oxide-trap (solid symbols) and effective interface-trap (open symbols) charge densities for pMOS Oki transistors with 50 nm oxides irradiated at 25°C to 75 krad(SiO_2) at V_g = 6 V, and then annealed at 100°C at ± 6 V bias.

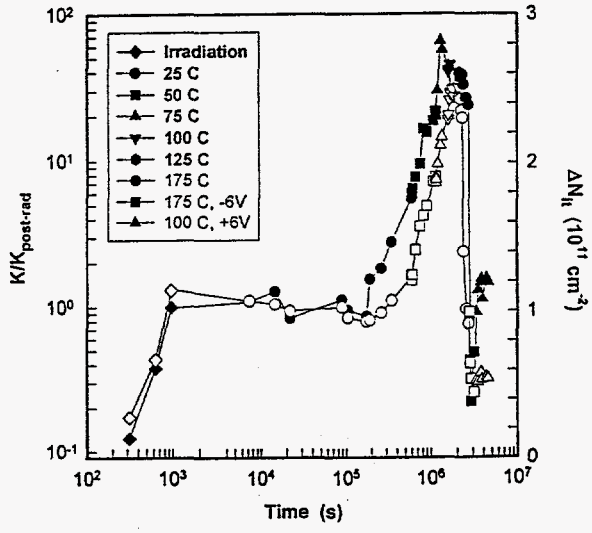

Fig. 2: K normalized to its level immediately after 75 krad(SiO_2) irradiation (left hand scale, solid symbols) and effective interface-trap densities (right hand scale, open symbols) for the irradiation and anneal sequence of Fig. 1. For reference, the value of K was 8.4 x 10^{-14} V^2 before irradiation, and was 3.4 x 10^{-10} V^2 after irradiation to 75 krad(SiO_2), but before anneal.

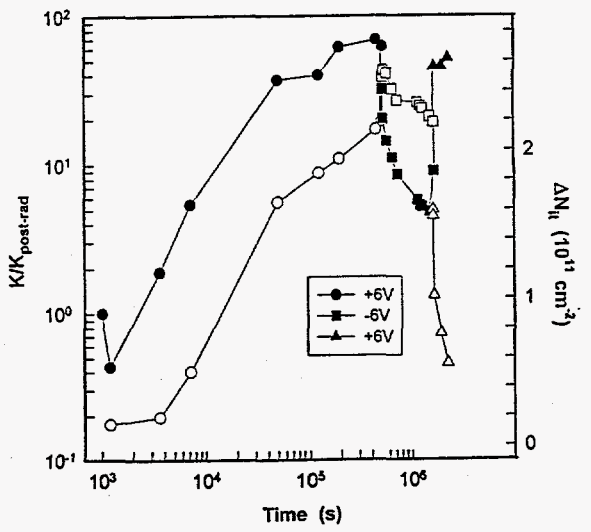

Fig. 4: K normalized to its level immediately after 75 krad(SiO_2) irradiation (left hand scale, solid symbols) and effective interface-trap densities (right hand scale, open symbols) for the irradiation and anneal sequence of Fig. 3. For reference, the value of K was 4.2 x 10^{-13} V^2 before irradiation, and was 3.2 x 10^{-11} V^2 after irradiation to 75 krad(SiO_2), but before anneal.