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Application of A Novel Silicon Thin-Film Transfer Technology to a Liquid Crystal Display

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I BACKGROUND.

The increasing demand for portable electronics is driving the silicon microelectronics world to investigate silicon-on-insulator (SOI) materials and technologies in the quest to provide low-power, low-voltage, high speed systems. The technical advantages of SOI are lower leakage currents, higher speeds, better threshold voltage control, immunity to latch-up and lower soft error rates than bulk silicon technology. Some application areas in which SOI is expected to have an impact are: memory chips (DRAM); smart power electronics; radiation-hard electronics; microelectromechanical systems (MEMS); integrated electrooptics; and high temperature electronics. SOI takes on many forms from the low-tech amorphous-silicon (a-Si), ubiquitous in active matrix liquid crystal displays (AMLCD), to crystalline silicon materials produced by sophisticated techniques such as SIMOX and UNIBOND [1]

Amorphous-silicon technologies succeed in providing a low-mobility transistor, less than $1 \text{ cm}^2/\text{V-s}$, with adequate performance for low-speed applications such as flat-panel displays. Many disadvantages of a-Si, such as low mobility, difficulty of doping and high threshold voltage, are outweighed by unique advantages such as high breakdown voltages and low deposition temperatures suitable for cheap large-area glass substrates. Precisely due to these drawbacks it is unsuitable for fabrication of high-density, high-speed, and small-area silicon electronics. Recent improvements in laser processing of amorphous silicon (a-Si) materials has permitted the improvement of a-Si characteristics by laser recrystallization techniques and promises to extend the performance characteristics of a-Si [2].

A SOI material system which offers better performance characteristics than a-Si is polysilicon-on-quartz requiring process temperatures in excess of 950°C [3]. It offers higher mobility transistors and lower threshold voltages than a-Si technology and is favored for applications such as printers and displays to achieve improved performance notwithstanding higher production costs.

A proprietary high-performance silicon-on-glass hot-wire recrystallization and thin-film silicon transfer technology has been developed by Kopin for AMLCD applications [4]. Beginning with an amorphous silicon layer on a patterned and oxidized silicon surface, a hot wire passed over the surface melts the a-Si material causing high quality grain recrystallization seeding from holes in the oxide pattern reaching down to the underlying silicon. Subsequent processing forms devices in islands of recrystallized silicon. A transfer process to a glass substrate is achieved by releasing one or more of the underlying dielectrics from the silicon islands, dropping off the silicon wafer and adhering the top layer of electronics to the glass surface using adhesive. However, besides being a delicate manufacturing operation and therefore potentially low yielding, it is a niche processing technique and cannot easily be adapted to high density circuits due to limitations imposed by the seed holes and the lower than bulk quality of the recrystallized silicon.

The most promising SOI technologies are SIMOX and UNIBOND. The former requires a heavy dose of oxygen implantation, followed by a high temperature anneal to create a thin film of crystalline silicon on a thin buried oxide. At the present time oxygen implant doses of $4 \times 10^{17}/\text{cm}^2$ to create the oxide layer and temperatures in excess of 1300°C are required to form the best SIMOX material. UNIBOND, a recent innovation[1], uses a dose of $5 \times 10^{16}/\text{cm}^2$ of H^+ to form a subsurface defective layer. After bonding the wafer to a second silicon holding substrate the first wafer separates at 550°C . UNIBOND is expected to be competitive with the best SIMOX. The

quality of the silicon thin-film generated using these approaches is bulk standard and the market for silicon microelectronics made using these substrates is expected to grow substantially in the next few years. The principal barriers for this technology are the starting substrate cost, about \$550 for an 8" SOI wafer versus \$130 for an 8" bulk wafer, and the necessity to redesign circuits to be fabricated in SOI.

The concepts and work introduced in this paper are a unique implementation of SOI distinct from the standard techniques outlined above. The object of this research effort is to find a convenient method to convert standard bulk silicon wafers with completed circuits to SOI-like configurations without the non-recurring engineering (NRE) costs. The LLNL technology, called START (Silicon Transfer to ARbitrary Substrate), uses standard bulk silicon wafers *after* the circuits have been conventionally fabricated. This technology attempts to combine the advantages of commercial bulk silicon electronics, such as cost and functionality (diversity of available circuit designs), with SOI advantages such as improved device isolation and increased speed without being penalized by substrate cost and NRE. This implementation is the first time the operation of standard thin-film silicon microelectronics has been demonstrated on non-silicon substrates. An outline of the procedure is as follows. The silicon wafer is bonded face down to a holding substrate. Silicon material, except what is required for device operation, is selectively removed by patterning and etching stopping on the underside of the isolation oxide. Isolated islands are formed containing single or multiple devices. Islands are held in place by the combination of holding substrate, bondline material, and the pre-existing matrix of interconnect materials and surface dielectrics resident on the original silicon surface. Bond pads on the silicon surface are accessed from the reverse side, for test purposes, by etching the isolation oxide cover, or by a pattern and etch step if a protective coating is deposited over the islands. Several of the attributes of standard SOI such as latch-up, substrate-induced crosstalk elimination, and field inversion prevention may be emulated by exercising this post-processing transfer of fully fabricated silicon wafers. The bonding and silicon removal can be performed onto many substrate types including plastics and thin-foil materials. Unique advantages include light transmission through a transparent substrate between the islands, and capacitance reduction since interconnect-to-substrate capacitance is mostly eliminated. In this work, the transfer process is applied to bulk silicon NMOS substrates. Ongoing work is determining the applicability of the transfer process to commercial bulk silicon CMOS substrates.

In part II of this paper the silicon fabrication, transfer processes and results are outlined. In part III the application of the technology to an active matrix liquid crystal display is described.

Part II

II.1 Silicon Fabrication.

PMOS devices and circuits are fabricated in a $2\mu\text{m}$ process of breakdown voltage greater than 20V. Four inch diameter silicon $\langle 100 \rangle$ wafers of resistivity $10\text{-}20\Omega\text{-cm}$ are used. A field oxide thickness of $6000\text{\AA}$ is grown in steam at 1000°C for 2 hours. Active areas are masked and etched into the isolation oxide and a $400\text{\AA}$ gate oxide is grown followed by a $4500\text{\AA}$ polysilicon deposition. The polysilicon is doped in a liquid source furnace cycle prior to patterning to form the gate and electrode regions. The source and drain are simultaneously doped using an ion implantation of boron at 40keV and a dose of $1 \times 10^{15}/\text{cm}^2$. The dopant is annealed at 900°C for 30 minutes in a nitrogen ambient. The back-end steps are the same as above. An undoped low-temperature $2000\text{\AA}$ thick oxide is deposited and contacts are patterned and etched in a CHF_3/O_2 plasma. A $0.5\mu\text{m}$ Aluminum/1% Silicon layer is deposited and patterned to define the interconnects. A forming gas anneal is performed at 300°C for 15 minutes. The final preparatory step prior to bonding is removal of the backside oxide in a wet chemical etch. Circuits and transistors are tested before bonding.

Figure 1. (a) Forward drain current versus drain voltage for PMOS transistors before and after transfer to Corning 7059 glass, using gate voltages of -1, 1, 3, and 5V. The transistor size is $21\mu\text{m}/4\mu\text{m}$. (b) Reverse drain current versus drain voltage for the same devices. Differences in device performance before and after transfer are attributed to measurements taken at different locations on the silicon wafer.

The forward drain current versus drain voltage characteristic of a PMOS transistor on silicon is shown in Figure 1A with gate voltage as a parameter. The gate voltages are 1, -1, -3, and -5V. The device has a drawn width of $21\mu\text{m}$ and length of $10\mu\text{m}$. The reverse drain current versus gate voltage characteristics are shown in Figure 1B. The forward breakdown characteristics of a PMOS transistor on silicon are shown in Figure 2. The device has a breakdown voltage higher than 20V since the substrate doping is about $1\text{e}15/\text{cm}^3$.

Figure 2. Forward breakdown drain current versus drain voltage for a PMOS transistor, before and after transfer to Corning 7059 glass, using gate voltages of 0, -10, -20, and -30V. The transistor size is $21\mu\text{m}/10\mu\text{m}$. Differences in the latter characteristics are attributed to measurements taken on different wafers before and after transfer.

II.2 The Silicon Transfer Process

The silicon transfer process described in this section is performed on wafers fabricated in PMOS. The wafer, placed on a support substrate, is separated from the support using shims or spacers while epoxy is introduced at the edge as shown in Figure 3A. The epoxy wicks in by capillary action to fill the void between the two substrates, as illustrated in Figure 3B. Masterbond epoxy product number EP112 was selected due to its excellent resistance to the chemical solutions commonly used in silicon processing, its high optical clarity, its high shore hardness value of 93, and low viscosity of less than 200cps. A thermoset cycle of 110°C for 2 hours followed by 150°C for 3 hours is employed to achieve a bonded pair as depicted in Figure 3C. Corning 7059 glass shaped in the form of a silicon wafer and 1.1mm thick is selected as the holding substrate. This glass type is commonly employed in the manufacture of flat-panel displays due its remarkable surface quality and optical clarity, and sodium content less than 1ppm.

Figure 3. An illustration of the assembly process of the bonding pair. (a) the circuit wafer is inverted over the holding substrate (glass) and spaced apart using shims. A metal foil connector is applied to the edge of the silicon wafer before setting the epoxy. (b) An epoxy, Masterbond EP112 is wicked in from the edge. (c) after the epoxy has spread evenly throughout the space the wafer pair epoxy bondline is thermoset at 110°C for 2 hours and 150°C for 3 hours.

Figure 4. The wafer is immersed in a 3:1 $\text{H}_2\text{O}:\text{KOH}$ solution at 100°C to remove the silicon substrate. A cross-section of the silicon wafer is shown in the solution. The wire represents the metal foil after bonding. The wafer is thinned to about $10\mu\text{m}$ in a timed etch.

The silicon wafer backside is thinned as close as possible to the device layer. The thinning technique depicted in Figure 4 is employed in this work. The bonded pair is inserted in a heated beaker of 3:1 $\text{H}_2\text{O}:\text{KOH}$ at 100°C stopping at about $10\mu\text{m}$ of silicon thickness using a timed etch. The etch requires approximately 3 hours for a 4" diameter, $525\mu\text{m}$ thick silicon wafer. The glass surface is minimally attacked during the etch and maintains its surface finish quality.

An important feature of the transfer process is maintaining the backside surface quality of the silicon wafer before and after the silicon thinning in preparation for the final island patterning step. Since silicon wafer total thickness variations (TTV) are of the order of $1\mu\text{m}$, optimal results are achieved by maintaining less than $1\mu\text{m}$ average wafer backside surface roughness, and the TTV constant. Thinning may be performed using a mix-and-match of several techniques. Grinding and polishing may be used to thin the wafer and provide a satisfactory surface finish but maintaining the TTV is inordinately expensive for most applications. The etch solution employed in this work is sensitive to wafer doping concentration. Low doped p-type wafers maintain initial surface roughness throughout the etch period, however, n-type wafers show an "orange peel" effect with average surface roughness of about $10\mu\text{m}$ peak-to-peak. To achieve optimum surface finish after the wet KOH chemical etch, an initial silicon polish may be performed using a $\text{HF}:\text{HNO}_3$ solution [5]. In another approach, N-/N+ epitaxial wafers are selected as the wafer substrate. After a timed etch to $50\mu\text{m}$ of silicon thickness, the wafer is electrochemically etched to remove the remaining N+ material leaving a uniform and smooth epitaxial layer to perform the final step[6]. Etching solutions sensitive to changes in doping concentration levels (called Hi/Low solutions) or dopant types may also be used to delineate the epitaxial layer, however, this requires undesirably large volumes of $\text{HF}:\text{HNO}_3:\text{CH}_3\text{COOH}$ acid mixtures to be generated, an acid system with a brief useful lifetime [7]. Silicon spray etching equipment may also be employed to thin the wafer. SEZ (America) model RST 101 formulates one $\text{HF}:\text{HNO}_3$ for silicon removal at an average of $63\mu\text{m}/\text{min}$ and a second $\text{HF}:\text{HNO}_3$ formulation for silicon polishing [8]. After definition of the thin silicon layer, patterning and etching is performed to delineate the device islands on the holding substrate surface.

Figure 5. Patterned islands are prepared and transferred to Corning 7059 glass. (a) $5\mu\text{m}$ island patterns at densities of 1000 lines per inch (lpi) and 500 lpi in reflected light and (b) in transmitted light.

For display applications, patterned islands are prepared and transferred to Corning 7059 glass. In Figure 5, $5\mu\text{m}$ island patterns at densities of 1000 lines per inch (lpi) and 500 lpi are shown in (A) in reflected light and in (B) in transmitted light. The latter image indicates the significant aperture, or light transmitting region area compared to light blocking region area, of this technology. Traditional a-Si technology cannot achieve more than about 30% aperture ratio for pixels of $25\mu\text{m}$ dimension due to the large area consumed by the a-Si transistor. Crystalline silicon technology is limited only by feature size of the transistor technology and metal linewidth to achieve aperture ratios in excess of 80% even for $25\mu\text{m}$ pixels.

II.3 Device Performance after Transfer.

Silicon wafers containing PMOS devices have been bonded to Corning 7059 glass substrates and thinning followed by lithographic patterning has been performed to transfer a thin film of silicon microelectronics. The device characteristics equivalent to Figure 1A and 1B, measured on devices after transfer are shown in the same figures indicated in red. The “before” and “after” device measurements are taken from different wafers. Differences in the characteristics are attributed to variations in device parameters from one wafer to another. The device characteristics are sufficiently similar to claim that the transfer process does not affect the device performance.

The forward breakdown voltage characteristics of a PMOS transistor on silicon after transfer to glass are shown in Figure 2. The breakdown voltage exceeds 25V. Differences in breakdown voltage characteristics are attributed to measurements taken on different wafers.

III Application to a Liquid Crystal Display

In this section, the application of the LLNL transfer scheme to a flat-panel display technology is described. A conventional liquid crystal display (LCD) is composed of two Indium Tin Oxide (ITO is a conductive transparent metal) coated glass plates separated by a narrow space of approximately $3\text{-}10\mu\text{m}$ filled with a voltage-sensitive liquid crystal material. Polarizers are placed on either side of the glass plates to permit optical viewing of the liquid crystal switching. Rows of ITO lines on each glass plate are orthogonally opposed and pixels are located at the crosspoints. Conventional large-area, for example, laptop, LCDs suffer from an inability to display video rate images due to the length of the ITO rows and columns and parasitic capacitive effects. In an Active Matrix Liquid Crystal Display (AMLCD) a transistor is placed at each pixel

node to provide storage control for video speed applications. The silicon transfer technology described in this work permits the formation of crystalline thin-film silicon electronics on flat-panel display glass substrates. By taking full advantage of this ability pixel transistors, and driver and signal processing electronics may be implemented on the same glass substrate using a chip or wafer transfer scheme. The area in the vicinity of the silicon circuits and devices is free of light blocking material allowing the passage of light through the holding substrate and between the devices.

Figure 6. The 10x10 pixel array circuit on silicon. The die size is 8x8mm and the devices are 21/10mm. A blow up of one pixel is shown in the inset. The pixel electrode is 4500Å polysilicon which has a yellow tinge when viewed in transmission.

Figure 7. A photomicrograph of two completed 8x8mm display chips side-by-side.

Display circuits are designed and fabricated on silicon wafers and consist of a simple 10x10 crosspoint matrix with an active device at each node as illustrated in Figure 6. A photomicrograph of two completed display chips side-by-side is shown in Figure 7. The circuit die size is 8mmx8mm and the pixel size is 600 μ m. The large pixel size is selected to facilitate assembly and testing. The pixel electrodes are polysilicon for the transmissive display and aluminum/1% silicon for the reflective display. The polysilicon thickness of 4500 $\text{\AA}$ is thin enough to be transparent with a slight yellow tinge. Reflective display elements are constructed on the silicon wafer surface, prior to transfer, to verify the functionality of the silicon circuit. Circuits are transferred to glass and excess silicon is removed. Two types of LCD display are assembled over the circuits. The first system uses a polymer dispersed liquid crystal (PDLC) paste bladed onto the circuit surface and dried [9]. An ITO coated polyester is selected to form the opposing electrode. Since the PDLC material has a low wetting angle on ITO, it is possible to achieve isolated pixel light switching of the active matrix elements as shown in Figure 8(a). Voltages of as much as 20V are required for the PDLC system. A second system is assembled using conventional liquid crystal material, ITO coated glass substrates and polarizers to demonstrate larger area pixel switching. Lower switching voltages of 5-10V are used. The display in off-state is shown in Figure 8(b). A first row is shown switching in Figure 8(c) and a second row in Figure 8(d).

Figure 8. (a) Isolated pixel light switching of reflective active matrix elements using PDLC. Voltages of as much as 20V are required for the PDLC system. A second system is assembled using conventional liquid crystal material, ITO coated glass substrates and polarizers to demonstrate larger area pixel switching. Lower switching voltages of 5-10V are used. (b) The display in off-state. (c) A first row is shown switching (d) and a second row.

IV Conclusion

A novel technique for forming thin films of crystalline silicon on non-standard substrates has been demonstrated. The method requires bonding the circuit side of a fabricated wafer to a holding substrate and removing the silicon wafer followed by patterning and etching to form independent regions of devices and circuits. Access to bond pads for testing also requires no patterning. Deposition of a passivation layer requires one post-patterning step for wire bond pad openings. Device behavior is the same before and after transfer. Flat-panel display quality glass is used as a holding substrate to demonstrate the application of this technology to a liquid crystal display. A 10x10 PMOS pixel circuit is designed and transferred to glass. Transistors and pixels are shown to function after completion of the transfer process.

Ongoing work is concentrating on applying this technology to improving the radiation resistance of commercial bulk silicon fabrication processes. Glass is used as a holding substrate, however, many other substrate types are suitable and the use of flexible substrates such as polymer materials and thin-foil metals is presently being investigated. Applications for flexible substrates include smart cards where flexible microelectronics is essential to avoid chip breakage.

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References

- [1]. Aspar, B.; Bruel, M.; Zussy, M.; Cartier, A.M. "Transfer of structured and patterned thin silicon films using the Smart-Cut(R) process." *Electronics Letters*, 10 Oct. 1996, vol.32, (no.21):1985-6.
- [2]. Yale Sun; Sheau Chen; Ping Mei; Boyce, J.B. "Excimer laser annealing process for polysilicon TFT AMLCD applications." (Conference Record of the 1994 International Display Research Conference and International Workshops on Active-Matrix LCDs and Display Materials Proceedings of 1994 International Workshop on Active-Matrix LCDs (AMLCD), Monterey, CA, USA, 10-13 Oct. 1994). Santa Ana, CA, USA: SID, 1994. p. 134-7.
- [3]. Kobayashi, M.; Nakazono, T.; Mori, K.; Nakamura, H.; et al. "High-mobility poly-Si TFTs with tungsten-polycide gate for 1.9-Mpixel HDTV LCD projector." 1994 SID International Symposium Digest of Technical Papers. SID. Edited by: Morreale, J., Santa Ana, CA, USA: SID, 1994. p. 75-8.
- [4]. Salerno, J.P. "Single crystal silicon AMLCDs." (Conference Record of the 1994 International Display Research Conference and International Workshops on Active-Matrix LCDs and Display Materials Proceedings of 1994 International Workshop on Active-Matrix LCDs (AMLCD), Monterey, CA, USA, 10-13 Oct. 1994). Santa Ana, CA, USA: SID, 1994. p. 39-44.
- [5]. Stoller, A.I.; Speers, R.F.; Opresko, S. "A new technique for etch thinning silicon wafers". *RCA Review*, June 1970, vol.31, (no.2):265-70.
- [6]. van Dijk, H.J.A.; de Jonge, J. "Preparation of thin silicon crystals by electrochemical thinning of epitaxially grown structures." *Journal of the Electrochemical Society*, April 1970, vol.117, (no.4):553-4.
- [7]. Kern, W. "Chemical etching of silicon, germanium, gallium arsenide, and gallium phosphide." *RCA Review*, June 1978, vol.39, (no.2):278-308.
- [8]. L. Columbo. "Wafer Back Surface Film Removal", p193-196, *Semiconductor Fabtech*, Fourth Edition
- [9]. Takizawa, K.; Kikuchi, H.; Fujikake, H.; Namikawa, Y.; et al. "Polymer-dispersed liquid crystal light valves for projection display application." (Display Technologies, Hsinchu, Taiwan, 17-18 Dec. 1992). *Proceedings of the SPIE - The International Society for Optical Engineering*, 1992, vol.1815:223-32.

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