The Oxide Defined VCSEL-based Smart Pixels for the Optical Database Filter

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Abstract

This paper presents the construction of the smart pixel arrays which perform AND and XOR functions with three-input and one-output optical signals for the application of an optical database filter. The device is based on oxide confined VCSELs bump bonded to GaAs MESFET pixels. The MSM photodetectors are monolithically integrated with MESFETs.

Keywords: Smart pixels, VCSELs, Oxidation, bump bonding, optical database filter

Introduction

For the application of an optical database filter [1], an oxide defined VCSEL array is integrated with MSM photodetectors and MESFETs in a pixelated structure. The pixelated structure is created by flip chip bump bonding the VCSELs onto pads with in the pixels using a coplanar bonding technique[2]. This solves the packaging problem of the oxide confined VCSEL array due to its non-coplanar structure, and has the advantage of low interconnect capacitance and few wire bonds. This technique also provides more flexible device design than other bump-bonding techniques or monolithic integration of VCSELs with integrated circuits.

Smart Pixel Structure and Design

A block diagram of the basic function of the smart pixel is shown in Fig.1. The data and projection masks are the optical inputs to the XOR gate. The output of the XOR is ANDed with the selection mask optical input. The optical inputs are directed into the MSM detectors. The output of the smart pixel is a VCSEL.

Fig. 1. Database Filter Pixel Functional Block Diagram

In order to directly bond the VCSELs onto the pixels, a coplanar back-emitting VCSEL structure [3] was used, which as shown in Fig.2(a). This requires etching the wafer down to the n-mirror. A gold post is electroplated onto the exposed n-mirror to achieve the coplanar contact structure. An additional electroplating is needed to get gold posts on both p- and n-contact for pressure bonding. Fig.2(b) shows the flip-chip bonding of the VCSEL onto the pixel chip. The two chips are aligned by using an infrared light source to view through the chips. Ultra-sonic pressure is used to make the contact. Then the epoxy is flowed between the chips to increase the robustness and

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protect the front faces of the chips during the substrate removal. An AlAs layer is used as a stop etch layer for the substrate removal.

Fig.2 (a) The structure of flip-chip back-emitting VCSEL , (b) Bump bonding the VCSEL onto pixel chip

Oxide defined VCSELs are used to achieve low threshold current and single mode output, allowing smaller drive transistors and detectors, lower power density, and thus more dense arrays and higher speed performance are possible. The device mesa size is $40\mu\text{m}$, and the oxide confined aperture is designed to be $7\text{--}8\mu\text{m}$. The desired output power of the VCSEL is about $100\mu\text{W}$.

The photodetectors and electric circuits are monolithically integrated on a GaAs chip [4]. The layout of the pixel chip is shown in Fig.3. GaAs MSM photodetectors are used for the purpose of high speed. The electric circuits include 2-input AND and XOR gates and laser driver.

Fig.3 Smart Pixel Layout

Fabrication Procedure

The VCSEL wafer was grown by MOCVD on a GaAs substrate. First a $1000\text{\AA}$ AlAs etch stop layer for selective substrate removal was grown, followed by a $200\text{\AA}$ GaAs oxidation barrier. Above and beneath the active

layer are two $\text{Ga}_{0.02}\text{Al}_{0.98}\text{As}$ layers which are used as oxidation layers. The n-mirror was designed to have a lower reflectivity than the p-mirror for the purpose of back emitting. The wafer was made into flip chip back emitting VCSEL arrays through the following processes (Fig.4),

- A $40 \times 40 \mu\text{m}^2$ mesa etch was formed by reactive ion etch (RIE). The etching depth depends on the thickness of p-mirror and the cavity which is about $5 \mu\text{m}$. Then the $\text{Ga}_{0.02}\text{Al}_{0.98}\text{As}$ layers were oxidized at 430°C with about 85°C vapor for 25 minutes to obtain $7\text{--}8 \mu\text{m}$ oxide confined apertures.
- P-contacts and n-contacts were E-beam evaporated. The p-contact is composed of $500\text{\AA}$ Ti and $1500\text{\AA}$ Au, while n-contact composes $250\text{\AA}$ Ge, $520\text{\AA}$ Au, $150\text{\AA}$ Ni and $1000\text{\AA}$ Au. For an even current distribution there is a $5 \mu\text{m}$ wide contact trace surrounding the device mesa.
- Coplanar n-contact and $10 \mu\text{m}$ gold posts on both p and n-contacts were electroplated.
- An isolation etch was also performed by RIE. The etch depth is only critical in the minimum limitation which must reach the GaAs substrate.

Fig.4 VCSEL Fabrication Processes Diagram

The pixel IC was fabricated by the Vitesse foundry through the MOSIS service. Since the bonding pads on the IC are aluminum, a layer of base metal, $400\text{\AA}$ Ti, $3000\text{\AA}$ Ni, $400\text{\AA}$ Au and $4000\text{\AA}$ InSn, was evaporated on the bonding pads.

The actual bonding process of the IC and the VCSEL array is carried out in the mask aligner which is equipped with an infrared light source for viewing through the chips. The mechanically bonded chips are then transferred to the ultra-sonic pressure stage. The InSn solder is noticeably sticky. Thus the two chips are stuck together during the transfer. 4 pounds of force is used to press the bonded chips at 180°C while the ultra-sonic is applied.

A bead of the epoxy is placed on the side of the bonded chips with an optical fiber. The epoxy then has to wick neatly between the chips. The chip is exposed to UV for half an hour which cures and hardens the epoxy. The VCSEL substrate is then polished with Bromine Methanol till it is very thin. The remaining substrate is selectively removed in a $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ etchant. The AlAs etch stop layer is removed in a HF dip. Finally, the epoxy is removed by plasma etch.

Results

Figure 5 shows the VCSEL before bonding to the pixel chip and substrate removal. Before bonding the VCSELs on the IC, we measured the laser characteristics by probing the bonding pads directly. Several test structures with top emitting apertures were designed to do the measurement. Figure 6 shows the top emitting optical output power and the voltage across the VCSEL versus the injected current. The threshold current is 4.2mA and the voltage is 1.8V. The threshold current is a lot bit high because the p-mirror reflectivity was designed with the Au p-contact. However, the top emitting test structure has an aperture on the p-contact, thus the p-mirror reflectivity is low. The series resistance is about 100Ω .

Fig. 5 VCSEL chip before substrate removal

Fig.6 L-I and V-I curves of the top emitting VCSEL

To test the individual smart pixel for optical power conversion in switching, one of the three MSM photodetectors is illuminated and the VCSEL is wire bonded to the IC on an aluminum substrate. The test result is shown in Figure 7. The incident optical power that switches the pixel is about $7\mu\text{W}$.

Fig.7 Smart Pixel Optical Switching Characteristic

The pixels with the VCSELs bonded on the electric circuit is shown in Figure 8. Figure 8 (a) and (b) show the top and 3-D view respectively. It is clear that the alignment is good, which means the alignment was not lost during ultra-sonic processing. Figure 8 (c) shows the 4x4 smart pixel array. The IC is designed with a 4x4 array and several test structures at the edge. While the bonding yield was high, the contact resistance was also high. This cause of the contact resistance is not presently known and is under investigation.

(a) Top View of the smart pixel (b) SEM Photo of the smart pixel (c) 4x4 array of bonded VCSELs

Fig. 8 Bump Bonded Smart Pixel

Conclusion

We fabricated VCSEL-based smart pixel array for the application of database filter and preliminary results have been obtained. The threshold current of the top emitting VCSEL is about 4.2mA and the photodetector switch optical power is about 7μW. The bonding yield can be improved by coplanar the bonding pads on the electric chip.

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