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Planar Surface-Micromachined Pressure Sensor with a Sub-Surface, Embedded Reference Pressure Cavity

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ABSTRACT

Planar, surface micromachined pressure sensors have been fabricated by an extension of the chemical-mechanical polishing (CMP) process. CMP eliminates many of the fabrication problems associated with the photolithography, dry etch, and metallization of non-planar devices. Furthermore, CMP adds additional design flexibility. The sensors are based upon deformable, silicon nitride diaphragms with polysilicon piezoresistors. Absolute pressure is detected by virtue of reference pressure cavities underneath the diaphragms. Process details are discussed and characteristics from many devices are presented.

1. INTRODUCTION

Recently, there has been a great deal of interest in micromachined sensors and actuators. The Microelectronics Development Laboratory (MDL) at Sandia National Laboratories has developed a surface micromachined pressure sensor which is intended to be used as a modular building block for microsystems applications. One desirable feature of a modular approach is to have a robust manufacturing process, so that fabrication steps of different types of devices do not interfere with each other. An example of this concept is integrating MEMS with CMOS by embedding the MEMS in a subsurface trench prior to CMOS fabrication[1]. A key technology toward embedded structures is the chemical mechanical polishing (CMP) process. CMP has received much attention as a method to planarize interlevel dielectrics and metal interconnects and vias at the end of an integrated circuit fabrication process[2]. Shown in Figure 1, the process involves polishing a wafer on a rotating pad in the presence of a slurry. Typically CMP can be used to achieve local thickness uniformity of ± 2-5% and highest to lowest spot difference of 1500 Å[3]. The driving force for planarization in IC fabrication is the shrinking depth of focus budgets for sub-0.5 μm i-line lithography. CMP also has many perceived advantages, such as reducing defect densities[3].

In the area of micromachining, CMP has been applied to surface micromachining to create pressure sensors[4] as well as IC's monolithically integrated with MEMS devices[1]. CMP holds great promise for micromachining processes containing more than 2 μm step heights. CMP was used by one group to improve the optical quality of surface-micromachined polysilicon devices[5]. Other techniques for planarization have been reported such as double LOCOS[6,7] and plasma planarization[8]. These methods provide local planarization only. Plasma planarization and related technologies based upon spin coatings are pattern dependent, and therefore require careful design of mask sets. In contrast, CMP is considered a global planarization technique. Diaphragm- and cavity-based devices, such as pressure sensors, flexural plate wave sensors, micro-hotplates, and micro flow channels stand to gain from planar processes. Some of the structural advantages are illustrated in Figure 2. Well defined plate boundary conditions simplify mechanical behavior analysis. Also, the ≈2 μm cavity height

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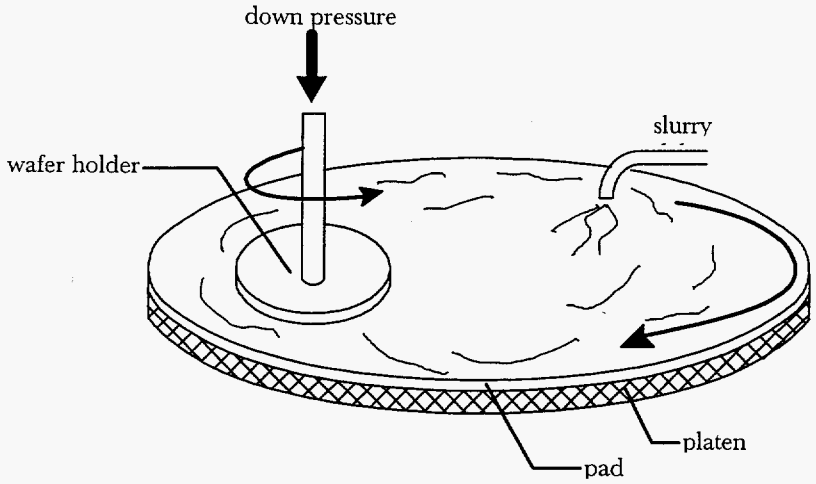

Figure 1. Schematic of CMP process. Adapted from reference 9.

limitation imposed by LOCOS or photolithography processes are overcome. Larger cavity heights could lead to reduced squeeze film damping, greater flexibility for flow channels, and improved thermal isolation for micro-hotplates. Other types of devices, such as microengines, high-aspect ratio accelerometers, and micromechanical fluid pumps also benefit from application of CMP[1].

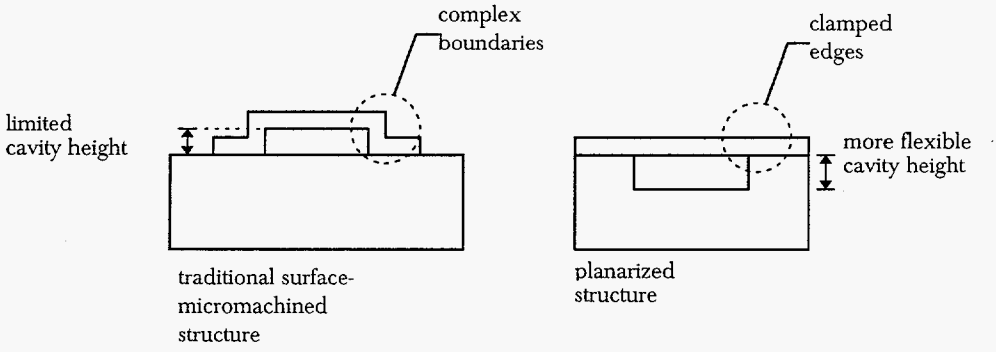

Figure 2. Structural advantages of planarized cavity-based devices.

2. EXPERIMENTAL

Design considerations for diaphragm geometry and piezoresistor placement have been reported elsewhere for the sensors presented in this paper[10] and similar sensors[7]. The principal difference between the sensors described here and previously reported sensors is the application of CMP to remove large step heights. The fabrication process is shown schematically in Figure 3. In the first step, two separate trenches are etched into the silicon substrate (Figure 3(a)). The first trench is shallow (0.3 μm) while the second trench is deeper (2 μm). The shallow trench serves as a narrow etch port which can be easily sealed at a later point in the process. Once the trenches are etched, a silicon nitride liner (0.3 μm) is deposited. Then the trenches are refilled with CVD oxides (Figure 3(b)). In the case of nitride diaphragms, a 1.2 μm oxide/ 0.1 μm 5% Boron 5% Phosphorous doped LPCVD oxide / 1.2 μm oxide stack is deposited. The borophosphosilicate glass is used to shorten the release etch time. For polysilicon diaphragms, 2.4 μm oxide film used. Then, the wafers are polished using a colloidal fumed silica slurry (Cabot SS-12) and a polyurethane pad (Rodel IC1000/Suba IV) (Figure 3(c)). Then the diaphragm material (low stress silicon nitride or fine-grained polysilicon) is deposited and patterned for etch ports (Figure 3(d)). The release etch is performed (1:1 HF:HCl , 1 hour) and the wafers are rinsed, dried, and sealed (Figure 3(e)). An air 'drip dry' is adequate for diaphragms up to 250 μm in diameter. However, stiction is occasionally observed for larger structures. The diaphragms are sealed by a 0.3 μm low stress silicon nitride

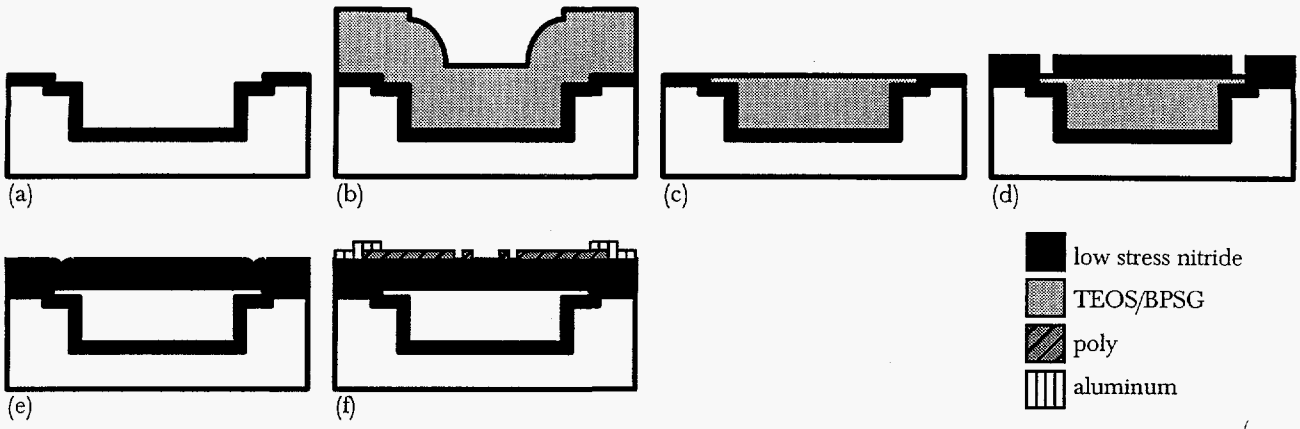

Figure 3. Schematic fabrication process for nitride diaphragm sensor. Dimensions are not to scale. (a) Etch two separate patterns in substrate and deposit nitride liner/polish stop. (b) Deposit thin oxide (BPSG) and thick oxide (TEOS). (c) Polish oxide stack. (d) Deposit diaphragm nitride, and pattern release etch holes. (e) Release etch diaphragm and seal with nitride. (f) Deposit, pattern, and implant poly; deposit and pattern aluminum.

deposition. Since the deposition is done in a LPCVD system, near-vacuum persists in the cavity after sealing and serves as a reference pressure.

Once the diaphragms have been sealed, special rinsing and drying techniques are no longer needed. Processing continues with the deposition and ion implantation of the polysilicon piezoresistors. An implant of phosphorus at 80 keV with a dose of $3{\cdot}10^{14}/cm^2$ was chosen to maximize the gauge factor of the polysilicon[11]. After implant, the polysilicon is patterned. Finally, aluminum metallization is deposited and patterned, and the devices are ready to be tested.

The processes used to fabricate these surface-micromachined pressure sensors are entirely CMOS compatible. Wet cleans, depositions, plasma etches, and photolithography are all performed using the same equipment set that is used for Sandia's 0.5 μm CMOS. The use of materials optimized for micromechanics, such as low stress nitride or fine-grained polysilicon, presents few problems for integration with CMOS. Furthermore, sealed diaphragms up to 250 μm in diameter are mechanically robust and survive stresses generated by immersion in aqueous solutions, and spin rinse drying.

There are many stages in the fabrication sequence where CMP improves the manufacturability of the sensor. Most of these improvements are related to the absence of a large step heights. In the conventional, nonplanar process the sacrificial oxide is on the surface of the wafer, leading to a 2 μm step height (see Figure 4(a)). The presence of this step height creates problems with creating etch access ports in nitride diaphragms: typically the sidewalls of the diaphragms are attacked by the plasma etch and become weakened. This is solved by using a CVD oxide hard mask for the etch. The problems associated with depositing and patterning both polysilicon and nitride are more difficult to overcome. Thicker photoresist is required for larger step heights and hence pattern fidelity can be degraded.

While polysilicon step coverage over large step heights is excellent, anisotropically plasma etching thin (0.1 μm) films is difficult. After the plasma etch has broken through the 0.1 μm thickness of the poly film, ~ 1.9 μm remains on the sidewalls of the diaphragm. Because removing these 'stringers' is difficult, an isotropic etch is typically used. Ideally, only 0.1 μm of poly on either side of a line would be underetched, but in practice, the amount of underetch is difficult to control.

Similar problems that arise for poly also exist for aluminum. The aluminum (0.1 μm thick) is etched in a wet etch solution of phosphoric, acetic, and nitric acids instead of a plasma etch. This wet etch is also difficult to control. Typically, 1 μm features do not reliably survive this etch, while 2 μm features do. Since aluminum is most commonly deposited by sputtering or evaporation, incomplete step coverage is expected. To alleviate this problem, a shunt layer of heavily doped polysilicon can be placed underneath the aluminum to carry current

over large steps.

While it has been demonstrated that surface micromachined pressure sensors can be made without the use of planarization techniques, these types of sensors pose many fabrication issues. In the absence of step heights, minimum feature sizes can be achieved with the use of thinner layers of photoresist. Furthermore anisotropic dry etches can be used on both polysilicon and aluminum, and the shunt layer can be removed altogether.

3. RESULTS AND DISCUSSION

Finished nonplanar and planar devices are shown in Figure 4. Details of the fabrication process to create the nonplanar devices are given in reference 10. The silicon nitride diaphragms were ≈ 1 μm thick, while the polysilicon diaphragms were ≈ 2 μm thick with an additional 0.6 μm low stress nitride seal. A cross sectional scanning electron micrograph of a diaphragm seal is shown in Figure 5.

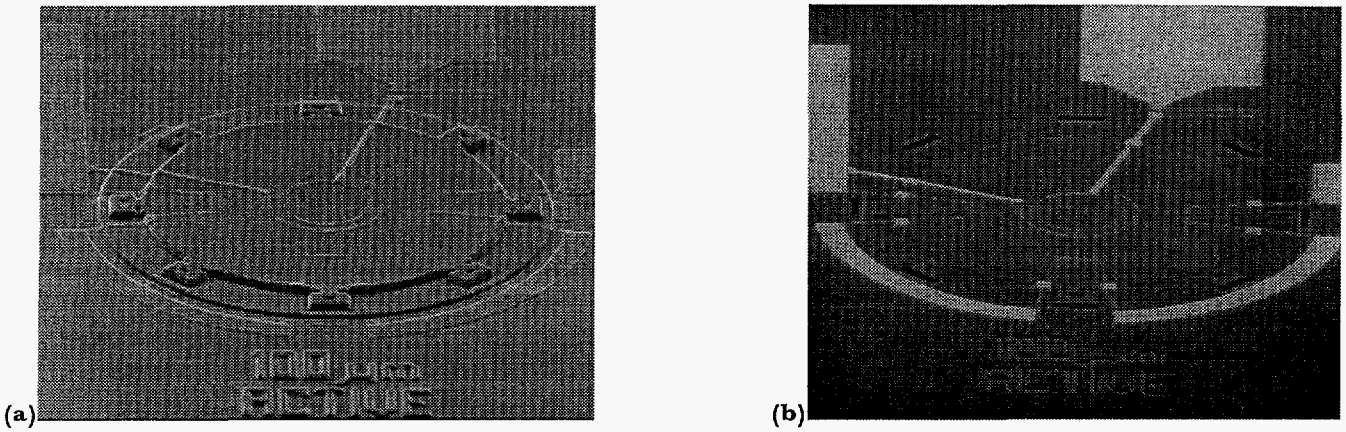

Figure 4. (a) Non-planar and (b) planar pressure sensor diaphragms. Etch access ports on planar sensor are approx. 0.8 μm deep, but do not cause processing difficulties with photolithography, dry etch, or metallization. Diaphragms are 100 μm in diameter.

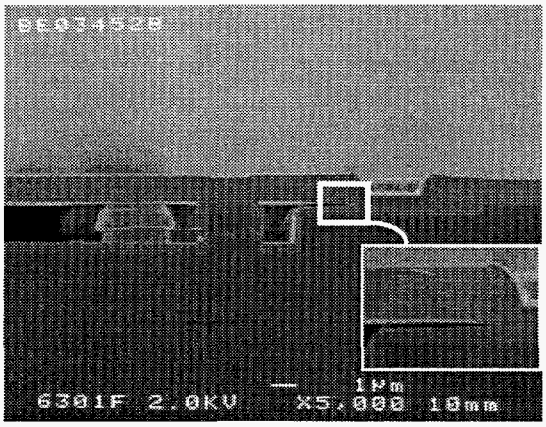

Figure 5. Cross section of diaphragm seal of silicon nitride diaphragm. Inset shows the seal region in more detail.

Typical output characteristics of different sized nitride and polysilicon diaphragm sensors are plotted in Figure 6 (a) and (b), respectively. Diaphragm sizes of 50, 100, 150, and 200 μm diameter were used. Both types of sensors exhibit behavior that would be unexpected from small deflection plate theory. Large deflection theory, coupled with the inclusion of residual thin film stress can explain most of the behavior in both types of sensors. Low stress silicon nitride diaphragms can have as much as 100 MPa built in tensile stress, which greatly reduces

the mechanical sensitivity of the diaphragms to pressure, such that the 100, 150, and 200 μm sensors all have similar pressure sensitivity at low pressures. In the polysilicon sensors, there is much less built in stress, and the pressure sensitivities are more differentiated. The 200 μm sensor has a negative pressure sensitivity which may be due to an incomplete oxide etch. This behavior is currently under investigation.

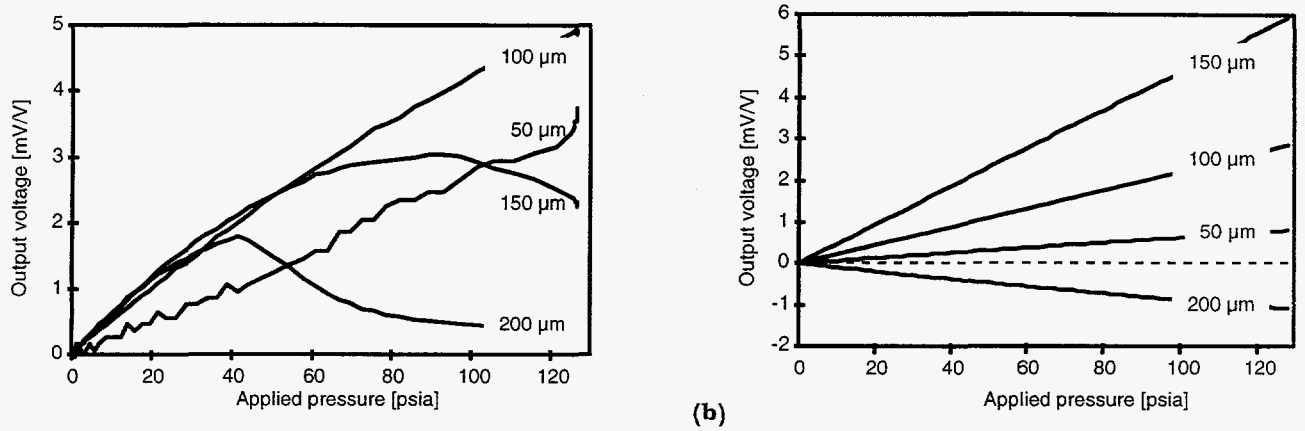

Figure 6. Output curves for (a) nitride and (b) polysilicon diaphragms. Curves have been normalized to have zero offset voltage. Offset voltages are given by histograms in Figure 7 and Figure 8.

The data from Figure 6 can be fitted to a second order polynomial using the least squares method:

$$\frac{V_{out}}{V_{in}} = C_2P^2 + C_1P + C_0$$

where V_{out}, V_{in}, and P are output voltage, applied bridge voltage, and pressure. The coefficients C_0 C_1 and C_2 are the offset voltage, sensitivity, and nonlinearity, respectively. Since the above equation is normalized to input voltage, the units of volts appear in the denominator of all of the coefficients. For nitride diaphragms, which have pressure curves that roll over at high pressure, the high pressure data is truncated to attain a good fit. Histograms of these characteristics from 37 nitride dice and 64 polysilicon dice are shown in Figure 7 and Figure 8, respectively.

The nitride sensors were generally much more sensitive than their polysilicon counterparts, due primarily to differences in the thicknesses of the diaphragms. Also, the nitride sensors generally had higher offset voltages spread over a wide range, whereas the polysilicon sensors had smaller offset voltages with tighter distributions.

4. CONCLUSION

Planar pressure sensors have been fabricated and tested. The sensors are based on nitride or polysilicon diaphragms with polysilicon piezoresistors. All materials and processes were CMOS compatible. Fabrication details were presented and discussed. Offset voltage, sensitivity, and nonlinearity of several sensors were extracted from least squares fits of measured data.

5. ACKNOWLEDGMENTS

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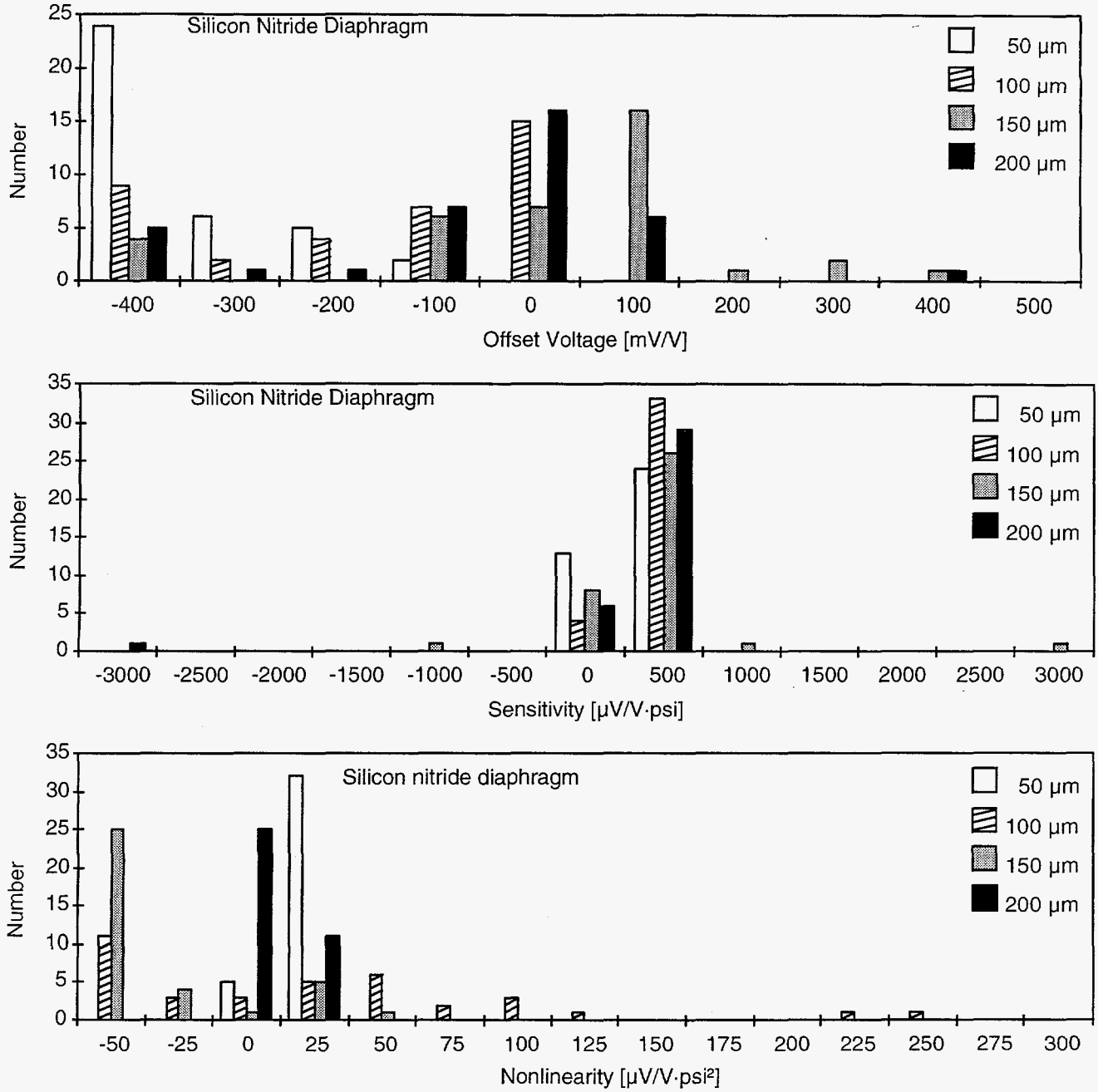

Figure 7. Sensor characteristics for nitride sensors.

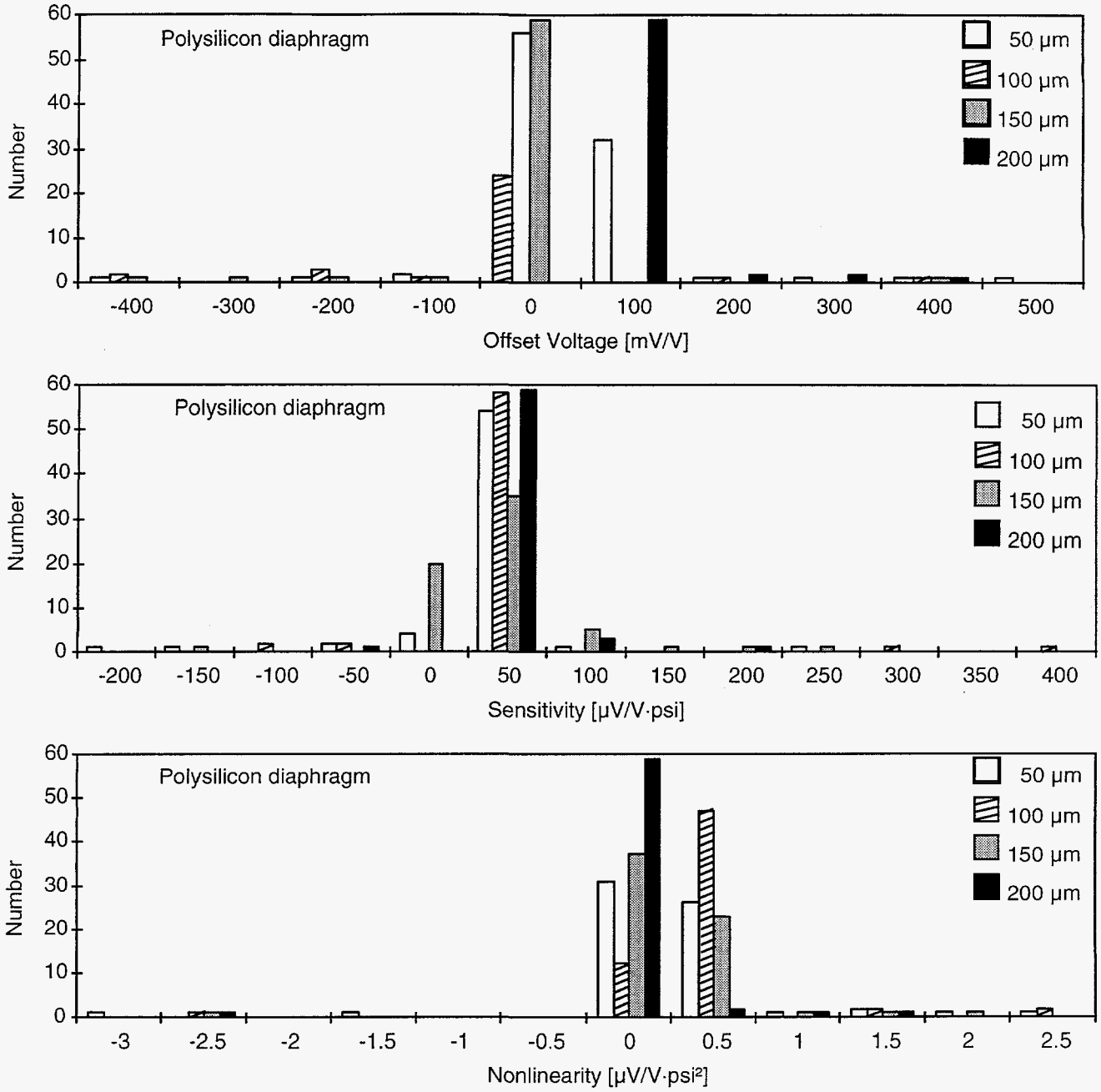

Figure 8. Sensor characteristics for nitride sensors.

6. REFERENCES

[1] J.H. Smith, S. Montague, J.J. Sniegowski, J.R. Murray, and P.J. McWhorter, "Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS", *Technical Digest, The 1995 International Electron Device Meeting, IEDM 95,* IEEE, pp. 609-612 (December 1995).

[2] W.L. Guthrie, W.J. Patrick, E. Levine, H.C. Jones, E.A. Mehter, T.F. Houghton, G.T. Chiu, and M.A. Fury, "A four-level VLSI bipolar metallization design with chemical-mechanical planarization", *IBM Journal of Research and Development*, **36**(5), pp. 845-857 (Sept. 1992).

[3] P. Singer, "Chemical-mechanical Polishing: A New Focus on Consumables", *Semiconductor International*, pp. 48-52 (February 1994).

[4] R.D. Nasby, D.L. Hetherington, J.J. Sniegowski, C.A. Apblett, J.H. Smith, C.C. Barron, W.P. Eaton, and P.J. McWhorter, "Application of Chemical Mechanical Polishing to Planarization of Surface-Micromachined Devices", *Technical Digest: 1996 Solid State Sensors and Actuators Workshop, Hilton Head '96*, pp. 48-53 (1996).

[5] A.A. Yasseen; S.W. Smith, M. Mehregany, and F.L. Merat, "Diffraction grating scanners using polysilicon micromotors", *Proceedings, IEEE Micro Electro Mechanical Systems*, pp. 175-180 (1995).

[6] H. Guckel, and D.W. Burns, "Planar Processed Polysilicon Sealed Cavities for Pressure Transducer Arrays", *Technical Digest: IEEE International Electron Devices Meeting, IEDM '86*, pp. 223-225 (1984).

[7] D.W. Burns, "Micromechanics of integrated sensor and the planar processed pressure transducer," Ph.D. Thesis, Department of Materials Science, University of Wisconsin at Madison, 1988.

[8] Y.X. Li, P.J. French, and R.F. Wolffenbuttel, "Plasma Planarization for Sensor Applications", *Journal of Microelectromechanical Systems*, **4**(3), pp. 132-138.

[9] S.R. Runnels, L.M. Eyman, "Tribology Analysis of Chemical-Mechanical Polishing", *Journal of the Electrochemical Society*, **141**(6), pp. 1698-1701.

[10] W.P. Eaton and J.H. Smith, "Characterization of a Surface Micromachined Pressure Sensor Array", *Proceedings of the SPIE, Micromachined Devices and Components*, **2642**, pp. 256-164 (1995).

[11] P.J. French and A.G.R. Evans, "Piezoresistance in polysilicon and its applications to strain gauges", *Solid State Electronics*, **32**(1), pp. 1-10 (1989).