

**HAZARDS AND CONTROLS AT THE SANDIA NATIONAL LABORATORIES
MICROELECTRONICS DEVELOPMENT LABORATORY**

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The Microelectronics Development Laboratory (MDL) contains 30,000 ft², which includes 10,000 ft² of Class 1 clean room space. There are 20 laminar flow Class 1 clean room bays. The MDL supplies several, full-flow process technologies which produce complementary metal oxide semiconductor (CMOS) integrated circuits using 150 mm diameter silicon wafers. All gases, chemicals and physical hazards used in the fabrication processes are controlled to levels well below regulatory requirements. Facility engineering controls in the MDL include toxic and pyrophoric gas monitoring, interlocks, ventilation, substitution and chemical segregation. Toxic and pyrophoric gases are monitored continuously inside processing tools as well as through the exhaust lines, gas cabinets, the valve boxes, and in general work areas. The toxic gas monitoring systems are interlocked to gas shutoff valves and have both low and high level alarms. In-use process gases are stored in exhausted cabinets. All chemicals and gases are segregated by chemical type.

The processes are organized into eight sector areas that consist of photolithography, wet processes, dry etch, ion implant, metals, diffusion, chemical vapor deposition (CVD) and chemical mechanical polishing (CMP). Each morning, engineering, safety and facilities personnel meet to review the equipment and wafer lot status and discuss processing issues.

There are over 300 steps in the wafer fabrication process. The minimum feature size is 0.5 μ m and there are 3 metal interconnect levels as shown in cross section in Figure 1.

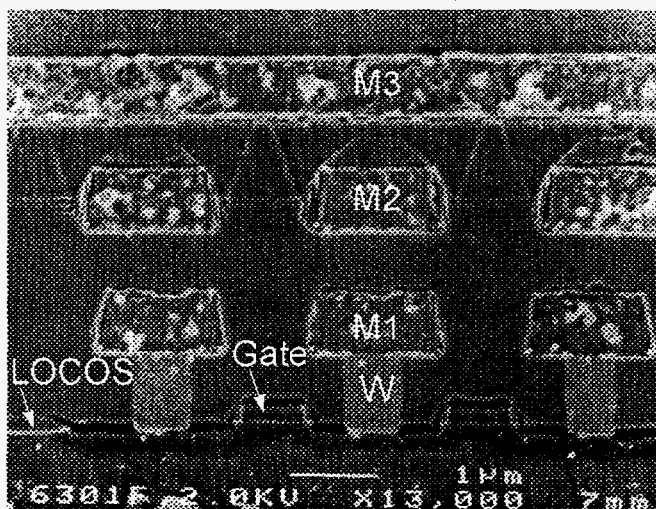


Figure 1 - Cross section of 3-level metal technology.

MASTER

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WET PROCESSING

The wafers are cleaned in exhausted wet benches with solutions that may contain sulfuric acid, hydrofluoric acid, ammonium hydroxide or other corrosive chemicals. A cassette containing several wafers is placed into the bath for cleaning. The cassette is then removed, placed into a rinse tank, and rinsed with deionized water. They are rinsed until all traces of chemicals are removed. The cassette is then placed into the spin rinse dryer where the wafers are dried. Automatic chemical processing systems are also used for cleaning. The potential exposure to chemicals is limited to filling the canisters and changing the filters. Personal samples for inorganic acid exposure are collected using low flow samplers and washed silica solid sorbent tubes in accordance with NIOSH method 7903.

Before field oxidation, the wafers are cleaned with a sulfuric acid/hydrogen peroxide solution followed by a hydrofluoric acid solution. Next, they are cleaned in Standard Clean 1 (SC-1), ammonium hydroxide/peroxide and hydrochloric acid/peroxide followed by Standard Clean 2 (SC-2), hydrochloric acid/hydrogen peroxide. After field oxidation, the wafers are cleaned in a hydrofluoric acid solution and rinsed. Then, the nitride is stripped in hot phosphoric acid.

Similar cleans are used before gate oxidation, before nitride sidewall nitride deposition, before titanium is sputtered onto the wafers for titanium silicide, and before the first interlevel dielectric multiple deposition/etch.

The wafers are cleaned with N-methyl 2-pyrrolidone (NMP) before tungsten via fills and before and after metal stack deposition. Passive dosimeters are used for personal monitoring of NMP.

PHOTOLITHOGRAPHY

Photolithography is used to produce each of the 15 mask levels of the wafer. To form the N+ source/drain regions, the wafers are coated with photoresist, exposed, developed and UV hardened.

Before photoresist coating, a wafer is first baked and primed in a vapor prime oven. Vapors of an adhesion promoter, usually hexamethyldisilazane (HMDS) are drawn into the chamber, coating the wafer's surface. After priming, the chamber is exhausted into the solvent exhaust system. The wafer is transported from the priming chamber to the photoresist coating chamber where photoresist (resin, UV sensitive initiator and solvent) is spun onto the wafer. After the photoresist has been spread over the wafer, the edge of the spinning wafer is sprayed with an "edge-bead remover" (propylene glycol monomethyl ether acetate). Passive dosimeters are used for personal monitoring. Glycol ethers with known reproductive toxicity are not used in the MDL. The waste photoresist and edge-bead remover that is spun off the wafer is collected in a can under the coating chamber for disposal as hazardous waste. The entire process has local exhaust ventilation. The wafer is then aligned to a mask in the exposure system. A UV light is shown through the mask onto the wafer, exposing the photoresist under the transparent portions of the mask. The wafer is then transported into a spin chamber for spray developing. While the wafer spins, an alkaline developer (dilute tetramethyl ammonium hydroxide) is dispensed onto the surface. The developer solution dissolves the photoresist in the areas that were exposed to the UV light.

Next, arsenic is implanted using arsine. Then the photoresist is removed in a dry etch process and the wafers are cleaned with a sulfuric acid/peroxide solution. After cleaning, the implant is annealed in a vertical thermal reactor and driven in at 900° C. using nitrogen.

In forming the P+ source/drain regions, the wafers are coated with photoresist, exposed, developed and UV hardened. Boron is implanted using boron trifluoride. Then, the photoresist is stripped using an oxygen plasma and a sulfuric/nitric acid solution. After stripping, the wafers are cleaned in a sulfuric acid/peroxide solution. Then the implant is annealed.

When patterning the contacts, the wafers are coated with photoresist and contrast enhancement material (aqueous solution containing resin and a photoactive compound), exposed, developed and UV hardened. The contacts are then dry etched. The resist is stripped using an oxygen plasma and N-methyl-2-pyrrolidone (NMP).

DIFFUSION

The diffusion process is used to grow various dielectric silicon dioxide films. Vertical thermal reactors are used for this purpose. During the oxidation process, a portion of the silicon wafer is consumed in the growing oxide. High purity steam is generated inside the oxidation tube by the burning of hydrogen in oxygen. Temperatures range from 600° to 1,100° C. Nitrogen is used as a carrier gas and/or a purge gas. Emissions from the equipment chambers are routed through a burnbox and scrubber before being emitted into the atmosphere. All gases used are plumbed directly into the equipment through stainless steel lines and the equipment is exhausted.

Diffusion is also used for gate oxidation. Sacrificial oxide is grown in a vertical thermal reactor using 1-1-1 trichloroethane. The sacrificial oxide is stripped using a hydrofluoric acid solution followed by sulfuric acid/peroxide, SC1 and SC2. Then the gate is oxidized in a vertical thermal reactor using dry oxygen at 900° C. After oxidation, boron is implanted in an ion implanter.

DRY ETCH

When fabricating the source/drain regions, the photoresist is removed in a dry etch process using RF energy to create an oxygen plasma which strips the photoresist. Radio frequency (RF) energy is used to cleave chemical bonds to produce a plasma containing oxygen radicals. The oxygen radicals react with the resist to oxidize it to water, carbon monoxide and carbon dioxide. RF is monitored with an RF meter for the appropriate frequency using IEEE and ACGIH guidelines. The wafer is then wet etched with a sulfuric/nitric acid solution.

An anisotropic dry etch process is used to etch silicon nitride when fabricating nitride sidewalls. Plasma etching is used to etch the silicon nitride. Silicon nitride is etched with a fluorine or chlorine containing gas such as carbon tetrafluoride, trifluoromethane, sulfur hexafluoride or nitrogen trifluoride. Silicon tetrafluoride is a byproduct.

ION IMPLANT

Ion Implant is used after gate oxidation. Boron is implanted using boron trifluoride. The ion implanter produces a boron ion beam and directs this beam so that the ions are uniformly implanted across and into the target silicon wafer. The implant process hazards are high voltage, toxic gases and mechanical hazards. They are controlled by automation, interlocks and shielding.

Phosphorous, using phosphine, is implanted during polysilicon gate fabrication. Arsenic, using arsine, is implanted during N+ source/drain fabrication. Personal monitoring for inorganic arsenic is in conformance with the arsenic standard.

CHEMICAL VAPOR DEPOSITION (CVD)

A CVD process is used to form the polysilicon gates. Amorphous polysilicon is deposited using low pressure chemical vapor deposition (LPCVD) in a vertical thermal reactor. The precursors are silane and hydrogen. Silane is heated to 800° C. yielding silicon and hydrogen. It dry etches the polysilicon not covered by resist. Phosphorus is implanted using a 15% phosphine 85% hydrogen gas.

The silicon nitride spacer is deposited onto the wafer in a vertical thermal reactor using a low pressure chemical vapor deposition (LPCVD) process. Silicon nitride grows onto the oxide layer. Chemical vapor deposition requires the decomposition of a gas to generate the chemical species of interest which is deposited on the wafer in solid form. The precursors for silicon nitride are dichlorosilane, nitrogen and ammonia. The byproducts of the decomposition, hydrochloric acid and ammonium chloride are pumped to a burnbox. The burnbox heats the chemicals to produce more benign chemicals. The result of the combustion is then pumped to a scrubber. There is continuous monitoring for dichlorosilane and ammonia.

The CVD process is also used in forming the first interlevel dielectric. A plasma enhanced tetraethyl orthosilicate (PETEOS) multiple deposition/etch deposits an oxide layer which conforms to the surface topography of the wafer. The precursor is tetraethyl orthosilicate (TEOS). The reaction byproducts are water vapor and ethylene (C₂H₄).

CVD is also used to form tungsten via fills. After titanium and a titanium nitride liner are sputtered onto the wafer for tungsten via fill fabrication, tungsten is deposited using a chemical vapor deposition process. The precursors are typically tungsten hexafluoride, silane and hydrogen. The byproducts are hydrofluoric acid in gas form, silicon tetrafluoride and hydrogen. These are pumped under negative pressure to a burn box and scrubber. The wafers are then planarized with chemical mechanical polishing and the tungsten studs are recessed using a sulfur hexafluoride with an argon plasma.

CVD is used for the final passivation. A complex circuit design may require 15 or more layer patterns to create the final integrated circuit (IC). The final passivation step contains a chemical vapor deposition (CVD) of p-glass. Phosphosilicate glass (PSG) contains phosphorus. The precursors for this reaction are silane, oxygen, nitrogen, and phosphine. The reaction byproducts are water vapor and undecomposed phosphine and silane. This is exhausted into a burnbox for combustion, decomposition and oxidation and then scrubbed. The toxic gas monitoring system monitors continuously for silane and phosphine.

METAL DEPOSITION

Metal deposition is used to form titanium silicide (TiSi₂). First, titanium is sputtered onto the wafers. RF is used to sputter the titanium onto the wafer in a stainless steel chamber. The titanium target is bombarded with argon ions to release titanium ions. These atoms form a film on the wafer.

Titanium silicide is formed in a rapid thermal annealer with a nitrogen atmosphere. The unreacted titanium is wet etched in an ammonium hydroxide/peroxide solution. The final titanium silicide is formed using a rapid thermal annealer with argon. Titanium alloys with silicon

at the gate and wells to form titanium silicide. Personal monitoring for metals during maintenance activities is in accordance with the applicable OSHA or NIOSH methods.

In forming the tungsten via fills, a titanium pre-liner is sputtered onto the wafers using RF. This is followed by a rapid thermal anneal at 600° C. using nitrogen. Titanium and a titanium nitride liner are then sputtered onto the wafer.

To form the metal stack, titanium, aluminum copper and titanium nitride are sputtered onto the wafers. The wafers are then coated with photoresist which is exposed, developed and UV hardened. Then the metal stack is dry etched.

CHEMICAL MECHANICAL POLISHING (CMP)

In fabricating the first interlevel dielectric, an oxide layer conforming to the surface topography is deposited. The films are planarized by rotating the wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry. CMP is used to eliminate depth of focus problems for submicron lithography and defects associated with metal thinning that can occur over steep topography. Another CMP process is used for planarizing CVD tungsten filled vias. The slurry in this case consists of an alumina abrasive (closer to the hardness of tungsten than silica) and an oxidizer of tungsten metal such as potassium iodate or ferric nitrate. There is local exhaust ventilation on the tool. This is followed by a double-sided brush scrub and CMP decontamination.

SUMMARY

Sandia National Laboratories has comprehensive ES&H and industrial hygiene programs. In addition, there are programs specific to the MDL. Hazards are assessed in the MDL with periodic walkthroughs, continuous toxic and pyrophoric gas monitoring and personal monitoring. All chemicals and gases proposed for use in the MDL are reviewed by the industrial hygienist and must be approved by a manager before they are purchased. All new equipment and processes are reviewed by a hazard and barrier committee and cannot be used in the MDL without the committee's approval and an IH hazard assessment. Overall risk of operating the MDL has been reduced to a level that is as low as reasonable achievable for this research facility.

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