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Materials and Process Development for the Monolithic Interconnected Module (MIM) InGaAs/InP TPV Cells

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Introduction

Four major components of a thermophotovoltaic (TPV) energy conversion system are a heat source, a graybody or a selective emitter, spectrum shaping elements such as filters, and photovoltaic (PV) cells. Most TPV systems under consideration envision utilizing planar one-junction low bandgap (Eg) PV cells. III-V materials such as InGaAs/InP, GaSb, and InGaSbAs/GaSb are examples of the cells currently used. These devices commonly have high output short-circuit current densities (J_{sc}), in the range of 2-10 A.cm⁻², and low open-circuit voltages (V_{oc}), in the range of 450-550 mV. In a TPV system, however, these cells are connected in series to create a high voltage/low current configuration, in order to keep resistive power losses (i.e., I^2R) to acceptable levels.

Another approach to achieving a high voltage/low current configuration is to fabricate a device, where small area PV cells are monolithically series connected. We have termed this device a monolithic interconnected module (MIM). A MIM device has other advantages over conventional one-junction cells, such as simplified array interconnections and heat-sinking, and radiation recycling capability via a back surface reflector (BSR). These advantages, as well as, the electrical performance of MIM devices are discussed in detail in the preceding paper in these proceedings¹. We will, therefore, confine the contents of this article to the MIM materials, process development, and some optical results.

To fully take advantage of the BSR, MIM devices require the use of semi-insulating (S.I.) substrates that are transparent to infrared (IR) radiation. Also, to facilitate processing and fabrication, stop-etch layers are needed to be incorporated into the cell structure. As a result, in practical terms, only the InGaAs/InP cell materials are suitable candidates for MIM fabrication. The MIM structures we have processed and tested were, therefore, comprised of several p/n InGaAs cells deposited on semi-insulating InP and monolithically interconnected in series. The front, back, and interconnect metallizations were performed at the same time, and access to both positive and negative terminals were made from the top side of the module. The series connections from one cell to the next were made by interconnects which were electrically insulated from active regions of the module by dielectric barrier layers. InGaAs MIM devices were successfully processed with two different bandgaps: 0.55 eV and 0.74 eV. Schematic plan and cross-sectional views of a MIM device are shown in figure 1.

Figure 1.—schematic view of a MIM device, plan view (top), cross-sectional view (bottom).

The successful fabrication of InGaAs/InP MIM devices entails the development and optimization of several key components and processes. These include: isolation trench via geometry, selective chemical etching, contact and interconnect metallization, dielectric isolation barrier, back surface reflector (BSR), and anti-reflection (AR) coating.

The selection, development, and testing of the materials and processes described above for MIM fabrication will be described in the following sections.

Isolation trench via geometry and chemical etching

Minimizing the non-photoactive areas in MIM devices will result in maximizing the cell output power density. The non-photoactive areas include the isolation trench vias around the cells, positive and negative busbars, and metal grid fingers and interconnects. The isolation trench vias are responsible for electrically isolating the cells, as well as, isolating the MIM device from other devices on the InP wafer. They are made by chemically etching the InGaAs and InP layers of the MIM structure down to the S.I. InP substrate (see figure 1).

To investigate the minimum trench via width that could be imaged by ultraviolet (UV) photolithography and etched by wet chemical solutions, we designed a photomask with space

widths ranging from 1 to 10 μm . The photolithography process employed in our labs increased the actual space widths in the photoresist by about 2 μm . As a result, the smallest opening in the photoresist increased to about 3 μm and the widest to about 12 μm .

Selective etchant solutions were used to create trench vias of desired depth. Room temperature concentrated HCl was used to etch InP layers. This etchant does not attack InGaAs. $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ (3:4:1 vol.) was used to etch InGaAs layers with bandgaps (E_g) of 0.55 and 0.74 eV. InP is impervious to this solution. The smallest width via (i.e., 3 μm) was successfully etched down to the S.I. InP substrate. In addition to vertical etching, both solutions etched the semiconductor laterally underneath the photoresist. This lateral undercut was about 3-4 μm on each side of the via, for a vertical etch depth of 7-8 μm . We also used an alternative InGaAs selective etchant solution of $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ (1:2:4 vol.). This solution also laterally etched the semiconductor underneath the photoresist. The undercut produced by this etchant was, however, 1-2 μm greater than what was observed with the $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ solution.

As a result, using the HCl and the H_3PO_4 -based solutions, the narrowest trench via that was produced was about 12 μm wide. A cross-sectional SEM micrograph and a schematic drawing for this via is shown in figure 2.

Figure 2.—Cross-sectional SEM micrograph of a chemically etched trench via (top), schematic representation (bottom).

As shown in the figure, (111) and (211) semiconductor planes produced by etching the (100) surface, result in v-shaped vias. The outward slope of the via walls are crucial in successful MIM fabrication processing because they allow for the subsequent deposition of the dielectric barrier layer. V-shaped vias are only attained when the device geometry is properly aligned with

the crystallographic orientation of the S.I. InP wafer. Using Sumitomo supplied S.I. InP wafers, for example, the long dimensions of the busbars and interconnects in figure 1 are aligned parallel to the wafer primary flat (PF) to produce v-shaped vias. We also found that alignments that are a few degrees ($\pm 5^\circ$) off will not change the slope geometry significantly. An alignment perpendicular to the PF, on the other hand, will result in inwardly sloped (111) and (211) planes.

In addition to minimizing the width of the trench vias, we designed a photomask set that would reduce the interconnect width from our original design value of $300\text{ }\mu\text{m}$ to a new value of about $50\text{ }\mu\text{m}$. The interconnect area (see figure 1) includes the trench via, the back contact, and the front contact (excluding grid fingers and busbars).

In our original process sequence, trench vias were etched to a depth of $7\text{--}8\text{ }\mu\text{m}$ down to the S.I. InP. This was followed by another etch ($\sim 3\text{ }\mu\text{m}$) down to the lateral conduction layer (LDL), for the back contact (see figure 1). Our new design, reversed this procedure by carrying out the back contact etch first, followed by the trench via etch. In this case the via is located inside the back contact etch area. This configuration is shown in figure 3. By performing the via etch after the back contact etch, the via etch depth is reduced from its original value of $7\text{--}8\text{ }\mu\text{m}$ to $\sim 5\text{ }\mu\text{m}$. This in turn results in smaller lateral undercutting. As seen in figures 2 and 3, the total via width was reduced from 12 to $8\text{ }\mu\text{m}$.

Figure 3.—cross-sectional SEM micrograph of an interconnect area with Cr-Au contacts (top), schematic representation (bottom).

Also shown in figure 3 are the dielectric barrier layer and the back contact metal area. The interconnect design of figure 3 allows for the widths of the metal contacts and etch vias to be minimized, and at the same time, provides sufficient tolerance for alignment inaccuracies and dimensional changes which occur in photolithography and chemical etching processes.

Contact and interconnect metallization

The two most important requirements for a suitable metallization system to our MIM devices are: 1) adequate adhesion of the contacts to InP, InGaAs, and dielectric barrier layers, and 2) minimum specific contact resistivity (ρ_c) values in the $10^{-6} \Omega\text{-cm}^2$ range to both n- and p-type InGaAs. In the following sections these requirements are addressed.

Metal Adhesion

Most contact metallization systems we tested adhered very well to both InP and InGaAs. They were not, however, very adherent to any dielectric layers. We experimented with several contact systems. These were: Au-Ge-Au, Ag-Au, Cr-Au, and Ti-Au. We had used the Au-Ge-Au system in our previous works with InGaAs planar cells². This contact system had exhibited ultra-low ρ_c values on both InGaAs and InP doped layers, but its adhesion to dielectric layers or to angled semiconductor surfaces proved to be poor. This is illustrated in figure 4, where Au-Ge-Au was deposited on Ta_2O_5 , InGaAs, and InP in an interconnect area.

Figure 4.—cross-sectional SEM micrograph of an interconnect area with Au-Ge-Au (0.1-0.1-3 μm) metallization.

To improve adhesion, we replaced the Au layer in contact with the substrate with Ag, Cr, and Ti layers. These layers are known to have better sticking characteristics than Au to most substrate materials. We found that Ag behaved similarly to Au (figure 5), whereas, Cr and Ti, capped with Au, were very adherent to all surfaces (figures 6 and 3). Both Cr-Au and Ti-Au, deposited on Ta_2O_5 , passed our tape-pull and scratch tests.

Figure 5.—Cross-sectional SEM micrograph of an interconnect area with Ag-Au (3-1 μm) metallization.

Figure 6.—Cross-sectional SEM micrograph of a trench via area with Cr-Au (0.05-2 μm) metallization resting on Ta_2O_5 .

As seen in figures 4 and 5, Au-Ge-Au and Ag-Au contacts have lifted from dielectric coated areas, as well as, from some of the semiconductor corner areas. This no doubt is due to the presence of internal stress forces in the deposited films. The “air bridges” thus formed may pose long term reliability issues with these cells. The use of adherent contacts, such as Cr-Au (figure 6) and Ti-Au will alleviate such concerns.

Contact Resistivity

In addition to being very adherent, the metal contacts to MIM devices must have low contact resistivities. We measured the ρ_c values for each of the four metal systems tested in the previous section. The metals were deposited onto highly-doped p-type ($1\text{E}19 \text{ cm}^{-3}$) and n-type ($1\text{E}19 \text{ cm}^{-3}$) InGaAs epi-layers. The transmission line method (TLM) was used to make the

resistivity measurements. None of the contact systems were heat treated prior to TLM measurements. The ρ_c measurement results are shown in figures 7 and 8.

Figure 7.—Specific contact resistivities for Au-Ge-Au (0.1-0.1-3 μm), Ag-Au (3-1 μm), Cr-Au (0.05-2 μm), and Ti-Au (0.05-2 μm) on p-InGaAs.

Figure 8.—Specific contact resistivities for Au-Ge-Au (0.1-0.1-3 μm), Ag-Au (3-1 μm), Cr-Au (0.05-2 μm), and Ti-Au (0.05-2 μm) on n-InGaAs.

As seen in the above figures, ρ_c values for Au-Ge-Au to both n- and p-type InGaAs were extremely low. In fact, some of the values measured on n-InGaAs were near the theoretical minimum (in the $10^{-9} \Omega\text{-cm}^2$ range). Cr-Au and Ti-Au contacts, on the other hand had ρ_c values in the high $10^{-6} \Omega\text{-cm}^2$ range on p-type, and in the high $10^{-7} \Omega\text{-cm}^2$ range on n-type InGaAs. These values were, on average, about an order of magnitude higher than what is measured with Au-Ge-Au. They are, however, low enough that their contribution to the I^2R resistive losses in the cell remain negligible.

Dielectric Isolation Barrier

The function of the dielectric barrier is to electrically isolate the p- and n-type regions of each cell, thereby, preventing the shorting of the cell by the interconnect metallization (see figure 1). The dielectric must, therefore, be highly insulating and be free of pinholes. We examined three dielectric materials. They were, Ta_2O_5 , spin-on glass (SOG), and Si_3N_4 . Ta_2O_5 was electron-beam deposited. Accuglass 211 SOG, purchased from Allied Signal, was spin coated at 3000 RPM, and subsequently heat treated at 250°C for 15 minutes. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit Si_3N_4 . All dielectrics had thicknesses in the range of 2000-3000Å.

We designed metal-semiconductor-dielectric test structures to characterize these dielectrics. These test structures enabled us to measure the current-voltage (C-V) characteristics of the dielectrics (i.e., dielectric constant, resistivity, and breakdown strength), and to measure whether the films had pinholes

Unlike Si_3N_4 , Ta_2O_5 and SOG appeared to contain many pinholes and shunting paths. Consequently, their dielectric constant and breakdown strength could not be measured. Si_3N_4 , on the other hand, showed far better dielectric properties than the other dielectrics. In figure 9, the measured resistivity values for all the dielectrics tested are shown..

Figure 10.—Resistivity data for Ta_2O_5 , SOG, and Si_3N_4 .

As seen in the figure, Si_3N_4 had far greater resistivity than either Ta_2O_5 and SOG. Also, the true resistivity of Si_3N_4 was, in fact, greater than the value of $1.4\text{E}10 \text{ } \Omega\text{-cm}$ shown in the figure. We could not determine an exact resistivity value because in our C-V measurement set up, the maximum DC resistance we can measure is limited to $100\text{M}\Omega$. It should also be noted that unlike with the Si_3N_4 , the shunting effects of pinholes are represented in the measured values of resistivities for Ta_2O_5 and SOG. In other words, the actual resistivity values for Ta_2O_5 and SOG may be higher were it not be for the presence of pinholes in their structure.

In addition to having a very high resistivity, Si_3N_4 had a breakdown strength of greater than 1.3MV-cm^{-1} , and a dielectric constant of 5.3. These values indicate that the Si_3N_4 fabricated in our facilities is suitable for use in our MIM devices.

Back Surface Reflector (BSR)

A back surface reflector (BSR) is deposited on the non-electrically active (i.e., S.I. InP) back side of a MIM device (see figure 1). Its function is two folds. Since the semi-insulating InP substrate is transparent to infrared radiation, a BSR layer can reflect the long wavelength IR radiation (i.e., out-of-band) back to the radiation (heat) source. This recycling of the non-useful radiation increases the total TPV system efficiency. A BSR also reflects that portion of the in-band radiation which is not absorbed by the active regions of the cell in the first pass through. This, in effect, enables these photon to pass through the cell again, thus increasing the probability of their absorption. This has the effect of increasing the cell power output.

An ideal BSR should exhibit 100% reflectivity in all wavelengths. Practical BSRs, such as pure gold and silver, exhibit reflectivities in the range of 90% for most of the wavelengths of interest. Au and Ag reflectivities, as measured through S.I. InP, are shown in figure 10.

Figure 10.—Reflectivity data for Au and Ag BSRs on S.I. InP.

Our modeling of optimum BSR layers indicated that by interposing a MgF_2 layer ($\sim 4300\text{\AA}$ thick) between InP and Au or Ag, longer wavelength ($>2\mu\text{m}$) reflectivity can be enhanced. In addition, the MgF_2 layer physically isolates the metallization from the InP substrate, thereby eliminating any long term room temperature aging effects, which may lead to metal-InP interfacial optical degradation³. The reflectivity measurements for the MgF_2/Au and MgF_2/Ag on S.I. InP are shown in figure 11.

Figure 11.—Reflectivity data for MgF_2/Au and MgF_2/Ag BSRs on S.I. InP.

A comparison of data in figures 10 and 11 indicates that the presence of MgF_2 enhances reflectivity by a few percent for $\lambda \geq 2 \mu\text{m}$. It is also interesting to note that MgF_2/Ag showed better reflectivity than MgF_2/Au , whereas, Au-only had better reflectivity than Ag-only. We found, however, that MgF_2/Ag and MgF_2/Au are not practical BSRs due to the very poor adhesion of Au and Ag to MgF_2 . Both Au and Ag were easily scratched off the MgF_2 surface by gently rubbing them with tissue paper. Ag or Au films could also be readily lifted off the MgF_2 surface by pulling them with tweezers.

To improve adhesion, we introduced very thin ($\sim 50\text{\AA}$) layers of Cr and Ti between MgF_2 and Au. We then measured the reflectivity of $\text{MgF}_2/\text{Cr-Au}$ and $\text{MgF}_2/\text{Ti-Au}$ on S.I. InP. This is shown in figure 12.

Figure 12.—Reflectivity data for $\text{MgF}_2/\text{Ti-Au}$ and $\text{MgF}_2/\text{Cr-Au}$ BSRs on S.I. InP.

As seen in the figure, the reflectivity of $\text{MgF}_2/\text{Cr-Au}$ was unacceptably low in all the wavelengths of interest. $\text{MgF}_2/\text{Ti-Au}$, on the other hand, showed comparable reflectivity to MgF_2/Au in the $>2\mu\text{m}$ region. The reflectivity in the shorter wavelength range was, however, very low.

Anti-Reflection (AR) Coating

To minimize the reflection off the surface of MIM devices, we modeled two AR coating designs for use with cells with bandgaps of 0.74 eV and 0.55 eV. These AR coatings can be deposited by sequential evaporation of ZnS and MgF_2 . The optimized thicknesses for the ZnS layers were 1686 $\text{\AA}$ for the cell with $E_g=0.55$ eV, and 1413 $\text{\AA}$ for the cell with $E_g=0.74$ eV. The optimized thicknesses for the MgF_2 layers were 2771 $\text{\AA}$ for the cell with $E_g=0.55$ eV, and 2343 $\text{\AA}$ for the cell with $E_g=0.74$ eV. The calculated reflectivities for these AR coatings on InGaAs are shown in figures 13 and 14.

Figure 13.—Calculated reflectivity data for ZnS/MgF₂ AR coating on InGaAs with $E_g=0.55$ eV, 0-100% reflectivity (left), 0-10% reflectivity (right).

Figure 14.—Calculated reflectivity data for ZnS/MgF₂ AR coating on InGaAs with $E_g=0.74$ eV, 0-100% reflectivity (left), 0-10% reflectivity (right).

As shown in the figures, the calculated reflectivities for both structures are $\leq 1\%$, for the desired range of wavelengths. The performance of the deposited ZnS and MgF₂ layers should match their calculated values closely. We routinely deposit these films, with a range of thicknesses, for photovoltaic applications, and their measured reflectivity matches our modeling results quite consistently.

Summary

The selection, development, and testing of the materials and processes used for MIM fabrication was described. These included: isolation trench via geometry, selective chemical etching, contact and interconnect metallization, dielectric isolation barrier, back surface reflector, and anti-reflection coating. The main specific results obtained in our work is summarized below:

1. Etched trench vias, as small as, $8\ \mu\text{m}$ wide were developed. Interconnect areas with widths of only $50\ \mu\text{m}$ were also fabricated.

2. The selective etchants for fabricating these vias were: concentrated HCl to remove InP, and the $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ (3:4:1 vol.) solution to remove InGaAs.
3. Cr-Au and Ti-Au metallizations systems were determined to be suitable for use as ohmic contacts to n- and p-InGaAs. They were also found to be very adherent to various dielectric isolation barrier films.
4. The dielectric properties of PECVD-deposited Si_3N_4 barrier layer, was found to be far superior to Ta_2O_5 or SOG.
5. Ti-Au/ MgF_2 and Au-only BSRs had very high reflectivity in the IR region, when deposited on S.I. InP. Also, both BSRs adhered well to the substrate.
6. We designed and modeled two optimized AR coatings for use with MIM devices with bandgaps of 0.55 eV and 0.74 eV. The double-layer AR coatings were comprised of ZnS and MgF_2 layers. The calculated reflectivities for both structures were $\leq 1\%$, for the desired range of wavelengths.

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