# Electrical test structures replicated in silicon-on-insulator material

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## 1. ABSTRACT AND KEYWORDS

Measurements of the linewidths of submicrometer features made by different metrology techniques have frequently been characterized by differences of up to 90 nm. The purpose of the work reported here is to address the special difficulties that this phenomenon presents to the certification of reference materials for the calibration of linewidth-measurement instruments. Accordingly, a new test structure has been designed, fabricated, and undergone preliminary tests. Its distinguishing characteristics are assured cross-sectional profile geometries with known side-wall slopes, surface planarity, and compositional uniformity when it is formed in mono-crystalline material at selected orientations to the crystal lattice. To allow the extraction of electrical linewidth, the structure is replicated in a silicon film of uniform conductivity which is separated from the silicon substrate by a buried oxide layer. The utilization of a Silicon-On-Insulator (SOI) substrate further allows the selective removal of substrate material from local regions below the reference features, thus facilitating measurements by optical and electron-beam transmission microscopy. The combination of planar feature surfaces having known side-wall slopes is anticipated to eliminate factors which are believed to be responsible for methods divergence in linewidth measurements, a capability which is a prerequisite for reliable certification of the linewidths of features on reference materials.

Keywords: calibration, linewidth, MEMS, metrology, microlithography, SOI, standards

## 2. PROBLEM ADDRESSED

### 2.1 Methods divergence in linewidth metrology

Linewidth-metrology instruments may be classified into one of three groups according to the physics of the metrology process. The first is the beam-scattering group which reverse-models a feature's properties from an image and includes optical- and electron-beam reflection and transmission methods. The second group consists of the scanning probe methods, principally atomic force and scanning-tunneling microscopies. Instruments of this group deconvolve a feature's cross-sectional geometry from the profile collected by the probe. The third group is electrical metrology which provides a quantity called the electrical linewidth. Instruments of each group have their own advantages and limitations in wafer and mask fabrication-process control. However, there tend to be disparities between measurements of the linewidth of features made by instruments from any pair of different groups, these disparities being characteristic of the respective groups. For example, several authors have independently reported the tendency of electrical measurements of the linewidths of conducting features to be significantly less than corresponding SEM measurements.[1,2,3] As a consequence of this and related observations, linewidth metrology is said to exhibit methods divergence. Disparities between electrical linewidth measurements, which are a direct link to device performance, and measurements made by other techniques favored for in-line testing, are of particular concern. A first objective of the work described here is identifying the sources of methods divergence.

### 2.2 The importance of a standard definition of linewidth

In cases where a user wishes to have a physical standard for whatever purpose, it is clear that measurements extracted from it should not exhibit methods divergence. In other words, any two correctly-operating metrology instruments from the same, or from different, metrology-instrument groups must extract the same linewidth measurements from the physical standard. However, because instruments from different groups respond to different physical properties of a given feature, it is not surprising that they generally report different values of its linewidth. Accordingly, a prerequisite to a physical standard's certification is the definition of which of the various properties of its reference features, such as those exemplified in Figure 1, constitutes its linewidth. Whereas a standard definition of the linewidth of a feature having an arbitrary cross-sectional profile geometry does in fact exist,[4] this definitional standard

This work was supported by the United States Department of Energy under Contract DE-AC04-94AL85000. 

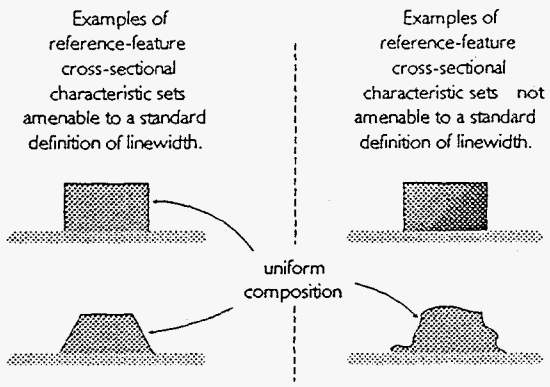


Figure 1. Examples of reference-feature cross-sectional characteristics amenable, and otherwise, to a standard definition of linewidth.

does not in general provide for the impact of possible transverse compositional variations which could variably affect the measurements of its linewidth by instruments from different groups. A standard definition that does so is unlikely to be devised. Therefore, the availability of a physical standard is compromised by lack of a standard definition of the linewidth of a feature having an arbitrary cross-sectional profile geometry and transverse compositional variations. This is certainly true if the arbitrary cross-sectional profile geometry and transverse compositional variations are unknown. However, there is a potential work-around of this limitation, to be described here, which is understood to be of value to a range of users having different applications. Reducing the work-around option to practice is a second objective of the work being reported here.

### 2.3 Summary statement of purpose

If an artifact were available whose features had a definitive cross-sectional geometric profile, other than its absolute dimensions, and whose features also had a known transverse compositional uniformity on a microscopic scale, then not only could the standard definition of linewidth be applied, but any residual methods divergence could reasonably be attributed to the respective instrument, either on a group or on an individual basis. Consequently, the artifact could be certified to serve as a physical standard for the practice of linewidth metrology. A key requirement is the macroscopic configuration of the artifact to meet the requirements of linewidth extraction by the entire range of metrology instruments used in wafer fabrication. Once the properties of definitive cross-sectional geometric profile and transverse compositional uniformity are provided, a driving consideration is testability for electrical linewidth because this quantity is not indefinite with respect to properties such as effective probe-tip shape or particle-beam modeling algorithm selection. The summary purpose of the work being reported is to configure, fabricate, and evaluate such an artifact for diverse purposes including probe-tip shape evaluation, particle-scattering algorithm development, and instrument calibration.

## 3. THE PROPOSED SOI SOLUTION

The proposed solution to the challenge of methods divergence is to devise an artifact having the following properties:

- the reference-feature linewidth is unambiguously defined. This requirement is met by fabricating reference features having cross-sectional profiles with properties consistent with an unambiguous linewidth-parameter value. Figure 1 illustrates some such cross sections.
- the linewidths of reference features are measurable by the full range of commonly-practiced metrology instruments/techniques and particularly by electrical methods.

There are additional requirements of normal linewidth reference-material practice:

- the material of the features, and the substrate which supports them, must be compositionally uniform.
- the geometry of the features must be uniform along their lengths: specifically, the cross-sectional profile geometry of a particular feature must be constant, which precludes any sidewall roughness.

The substrates should also conform to mechanical requirements for rigidity and compatibility with traceability instrumentation. The artifacts to be described in this paper have the potential of possessing all the attributes stated above.

### 3.1 MEMS implementations

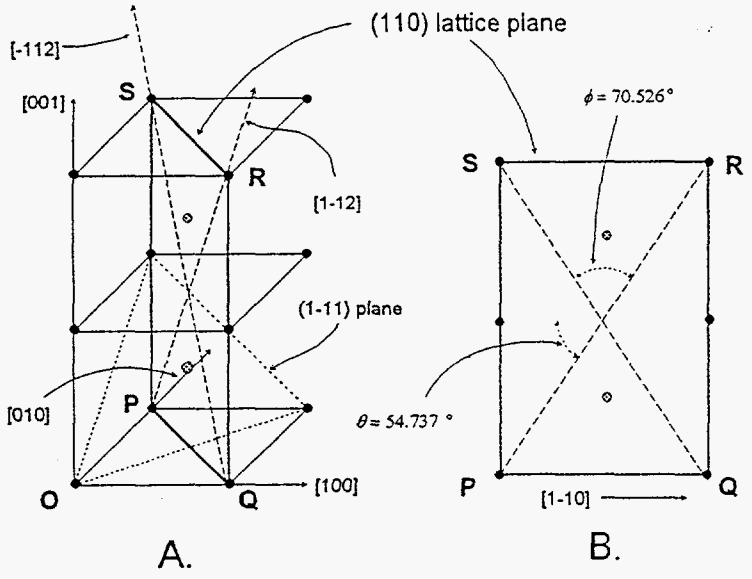


Figure 2. Applicable trigonometry of the (110) plane having coplanar [-112] and [1-12] vectors.

Micro-Electro-Mechanical Systems (MEMS) is the technology of fabricating miniature mechanical structures in bulk material or in solid-material films through patterned etches. Structures include miniature sensors, actuators, or mechanical components.[5] The use of a monocrystalline base material, and an etch which is anisotropic as a result of its preferentially etching in the directions of particular crystallographic planes, is a special tool in the fabrication of three-dimensional structures. These structures have the orientations of their post-etch surfaces controlled by the crystallography of the lattice. An etch of 19 wt. % of KOH in water at 80°C is commonly used to define structures in bulk silicon material having {111}-planar faces.† That is, the {111} planes are the slowest etching planes, and therefore, material surfaces exposed at the completion of an etch are either those that are protected by some *in-situ* masking or those having one of the orientations of the {111} family. Early applications of plane-selective anisotropic etches include decorating structural faults on exposed crystal surfaces for classifying the material's defect-count[6] and establishing ingot-material orientation. Other applications have included etching narrow grooves for VMOS technology.[7]

Applicable trigonometry of the (110) plane, containing the [-112] and [1-12] vectors, for the case of the silicon lattice is shown in Figure 2. The key trigonometrical attribute of cubic lattices, such as that of silicon, is that members of the {111} family of planes intersect members of the {110} family of planes orthogonally along lines coinciding with the directions of the <112> family of vectors. In Figure 2A, for example, the (1-11) plane intersects the (110) plane orthogonally, the line of intersection having a [-112] direction. It thus follows that, if intersecting line features having vertical sidewalls are to be patterned on {110} surfaces, these intersecting line features must be drawn in the [1-12] and [-112] directions, respectively. The trigonometry of the cubic lattice determines that the acute angle between the intersecting line features is $\phi = arctan(1/\sqrt{2}) = 70.526°$. The features are oriented at $\theta = 90 - \phi/2 = 54.737°$ to the [1-10] direction, within the (110) plane, as indicated in Figure 2B, where the plane of the paper coincides with the (110) crystallographic plane.

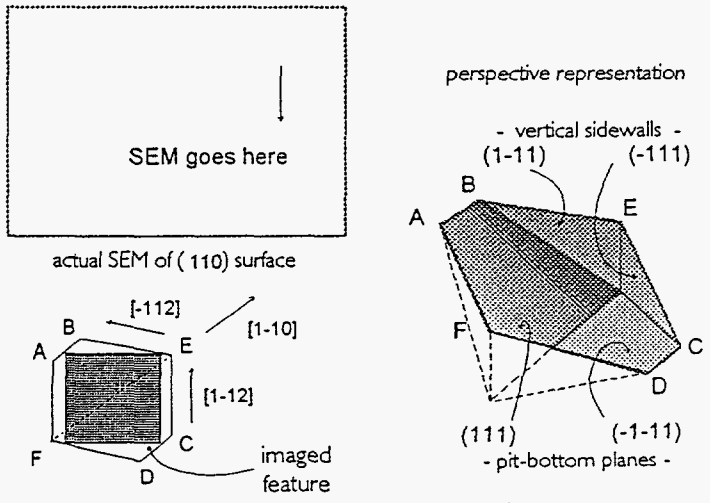


Figure 3. *The proper selection of the orientation of the silicon lattice with the edges of photolithographic features results in control of the feature geometry in three-dimensions. Note the imaged feature from which the pit was replicated.*

† Orientation notation convention: specific planes are indicated by parenthesizing the components of their normal vectors. For example, (100), (010) and (001) are three mutually-orthogonal planes. The notation {100} is the family of three planes. Similarly, [111] is a specific direction, and <111> means the family of all like directions (with any selection of the vector components being negative).

In general, the appropriate selection of both the orientation of the silicon lattice with the edges of photolithographic features used to mask the KOH etch, and the surface plane of the wafer, results in control of the feature geometry in three-dimensions. Surfaces of structures not having {111} planarity must be protected by the lattice's interface with another material such as silicon nitride, or silicon dioxide, during etching. An actual example is shown in the SEM reproduced in the upper left of Figure 3. In the lower left of Figure 3 is shown the approximate size and orientation of the lithographic feature which was defined on the [110] surface and etched to produce the pit shown in the SEM. Preferred etching of non-{111} planes resulted in the formation of the pit extremities ABCD. The perspective inset on the right identifies the lattice planes coincident with the inside surfaces of the pit. All of these planes are of the {111} family, including the four vertical sidewalls.

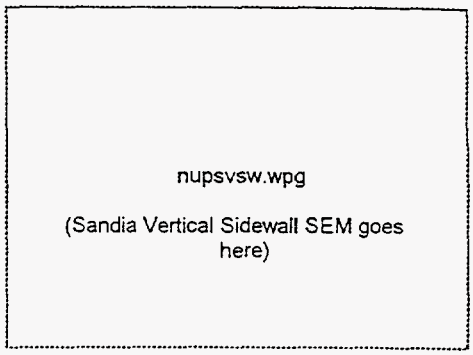


Figure 4. A grating of features having vertical sidewalls fabricated at Sandia National Laboratories. The *in-situ* oxide masking material, appearing as caps over the features, had not been removed when this SEM micrograph was made.

A recently-announced artifact made by etching a {110} bulk silicon surface resist patterned as a grating, having features with submicrometer pitch aligned in a <112> direction, is an example of a MEMS implementation of a reference material. The precisely-vertical {111} feature-sidewalls generate high-levels of contrast for the pitch calibration of electron-beam linewidth systems.[8] This work followed earlier reports on linewidth metrology of isolated lines with similar characteristics.[9] A pictorial example of a grating of features having vertical sidewalls fabricated at Sandia National Laboratories during the course of the work being reported here is illustrated in Figure 4.

### 3.2 Silicon-On-Insulator substrates

Silicon-On-Insulator (SOI) substrates have a surface layer of semiconductor-grade silicon separated from the remaining substrate material by an insulating layer. Otherwise, they resemble silicon wafers and are compatible with semiconductor-wafer processing equipment. Integrated circuits are formed in the surface layer through the application of the same wafer processing that is used for forming such circuitry on ordinary bulk-silicon wafers. The principal motivation for SOI development was the need for radiation-hardened latchup-free devices for space and military applications. However, the higher starting-material expense is offset by higher device speed through the elimination of parasitic capacitances to the bulk substrate and enables a higher device density.[10] Two different state-of-the-art SOI implementations are used in the work being reported here and these are described briefly in sections 3.2.1 and 3.2.2 below.

#### 3.2.1 SIMOX Silicon-On-Insulator material

In the early 1980s, silicon-on-sapphire was the leading technology for CMOS-SOI implementations. Although the recrystallization of films of poly- and amorphous-silicon deposited on oxide was studied as an alternative technical approach, SIMOX (Separation by the IMplantation of OXygen) became the technology of choice for radiation-hard CMOS implementations in the early 1990s. SIMOX wafers are prepared by implanting heavy dosages of $\approx 10^{18}$ cm$^{-2}$ of oxygen at energies of about 180 keV and annealing.[11] Selection of the proper annealing conditions results in a buried layer of silicon dioxide which electrically insulates the surface layer through which the oxygen ions were implanted, as illustrated in Figure 5 showing resultant typical layer thicknesses. The surface layer retains

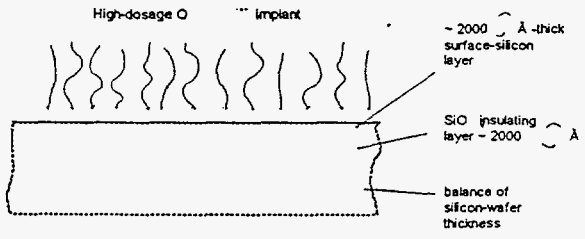


Figure 5. Selection of the proper annealing conditions results in a buried layer of silicon dioxide which electrically insulates the surface layer through which the oxygen ions were implanted.

qualities, such as silicon-lattice integrity, required for the fabrication of state-of-the-art CMOS circuitry with enhanced transconductance.

### 3.2.2 BESOI material

The second SOI implementation featured in the current work is Bonded and Etched-Back Silicon-On-Insulator (BESOI).[12] In this technology, two silicon wafers are thermally oxidized and then, with their oxidized surfaces in contact, are subjected to bonding at elevated temperatures in inert atmospheres which bonds the oxide films into a single layer. The result is a single wafer assembly which is etched back on one side to provide a surface layer of semiconductor-grade monocrystalline silicon. This implementation offers significantly more flexibility in the selection of the buried insulating layer's parameters and the doping levels, for example, of the silicon lattice adjacent to it.

## 3.3 Implementing MEMS technology on SOI substrates

A unique and novel facet of the work reported here is applying MEMS micromachining technology to the formation of CD-metrology structures on SOI material. A fortunate attribute of the KOH etch used for sample feature delineation is that it etches the silicon-dioxide barrier layers of SIMOX and BESOI substrates relatively slowly compared to its dissolution of non-(111) silicon surfaces. Accordingly, planar electrical test structures can be fabricated to enable the extraction of electrical linewidth measurement by techniques paralleling those used for planar structures patterned in chromium films on quartz or polysilicon on gate oxide, for example. However, it is necessary to carefully manage the replication of intersecting lines, which is trivial in the chromium-on-quartz implementation, but which has to be more carefully considered for the SOI case. Two SOI configurations which can provide intersecting lines, a special requirement of electrical test structures, delineated within the active silicon layer, are described below. They are distinguished by different respective crystallographic options afforded by the trigonometry previously illustrated in Figure 2. The two implementations are identified here as the Vertical-Sidewall (VSW) option and the Sloping-Sidewall (SSW) option.

### 3.3.1 Vertical-sidewall configuration

With regard to the VSW option, and according to the descriptions rendered in Section 3.1, features drawn in the [-112] direction have vertical sidewalls coinciding with the (1-11) plane after KOH etch. Further inspection of Figure 2, shown previously, reveals that features correspondingly drawn in the [1-12] direction also have vertical-side walls coinciding with the (-111) direction.

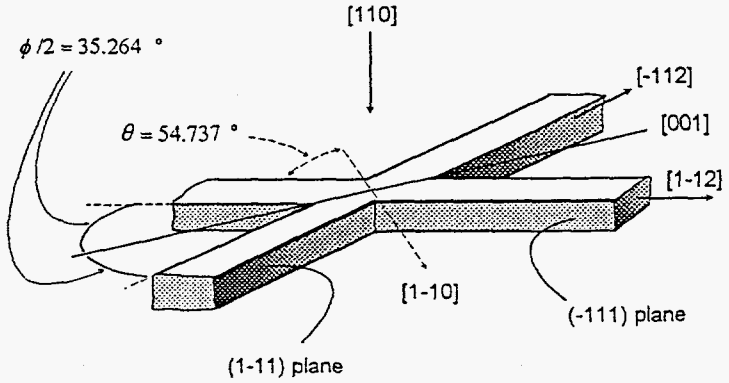


Figure 6. Intersecting features having vertical sidewalls must be oriented at $\theta = 90 - \phi/2 = 54.737°$ to the [1-10] direction within the (110) plane.

Thus, it follows that, if line features having vertical sidewalls, and which are intersecting, are to be patterned on {110} surfaces, they must be drawn in the [1-12] and [-112] directions, respectively. The trigonometry of the cubic lattice, as described in the discussion of Figure 2 in section 3.1, determines that the acute angle between the intersecting lines is $\phi = arctan(1/\sqrt{2}) = 70.526°$. For the particular case of Figure 2, they must also be oriented at $\theta = 90 - \phi/2 = 54.737°$ to the [1-10] direction, within the (110) plane, as indicated in the perspective drawing in Figure 6. Alternatively stated, they must be oriented at $\pm\phi/2 = 35.263°$ to the [001] direction, as shown.

When intersecting vertical-sidewall features are replicated on the {110} surfaces of bulk material, the 109.474° obtuse inside corner is cleared by the KOH etch and leaves a clean "vertical" line of intersection of the {111}feature sidewalls. However, with no supplementary processing, the 70.526° acute inside corner develops a (111)-plane facet

Figures 7 and 8.

which extends to the substrate surface as shown in ~~Figure 7, Figure~~ 8. The formation of the facet can be prevented, however, to leave a vertical-line intersection when the structure is fabricated on SOI substrates according to the process to be described in section 4.3.

### 3.3.2 Sloping-sidewall (SSW) implementation

The same crystallographic properties that provide the features with vertical sidewalls shown in Figure 4 lead to a second MEMS architecture with potential usefulness for linewidth reference materials. Even though this second architecture is not characterized by sidewalls that are vertical, its sidewalls are just as planar and smooth as those described in 3.3.1. Figure 8 shows an architecture of orthogonally-intersecting line features with their lengths aligned with <110> crystallographic vectors replicated on {100} surfaces. The features are characterized by sidewalls coincident with {111} planes and have slopes relative to the substrate surface of $\theta = 54.737°$.

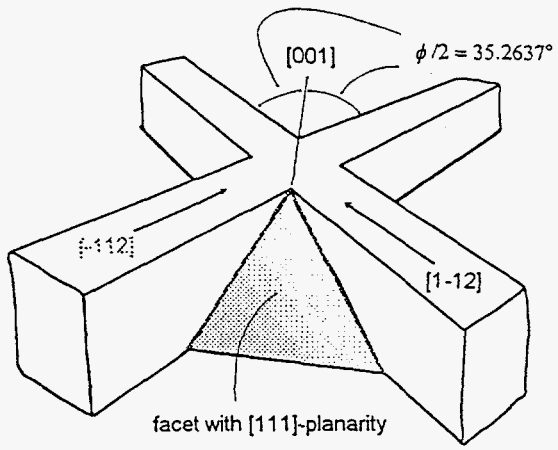


Figure 7. Unless processing steps supplementary to KOH etching are taken, the 70.526° acute inside corner of intersecting features develops a (111)-plane facet which extends to the substrate surface.

### 3.4 Interim statement of summary characteristics of KOH-etching of SOI silicon

The preceding sections have described the principles of replicating the equivalent of planar electrical test structures in monocrystalline silicon surface-layers of SOI wafers. The appropriate selection of the orientation of the starting SOI wafer, and the alignment of test structures' features relative to the crystallographic lattice, provide two architectural options for patterning test structures having features with planar sidewalls. In the VSW option, the allowed features have vertical† sidewalls, but may not intersect orthogonally. In the SSW option, the allowed features may intersect orthogonally but have sidewalls with a slope of 54.737° relative to the substrate surface. In principle, the sidewall surfaces are flat and smooth to within the amount of the silicon lattice constant which is 0.543 nm. Whereas there is much evidence in the literature to suggest that the subject test structures will have sidewall surface finishes with this desirable property, the case yet remains to be proven. If it is, then both the VSW and SSW options offer the possibility of fabricating features with a unique combination of important properties: namely,

- no ambiguity of edge location
- known sidewall slopes
- lattice-traceable reference metrology
- no sidewall roughness

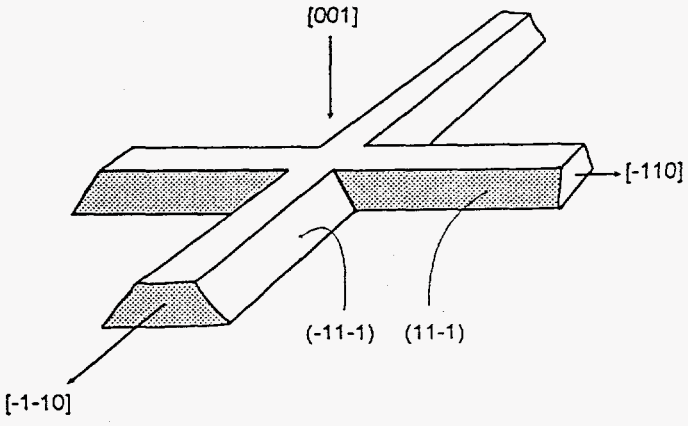


Figure 8. Orthognally-intersecting features, replicated on a {100} surface, with their lengths aligned with <110> crystallographic vectors.

† In the context of this paper, "vertical" means "normal to the substrate surface."

- usable by any known linewidth measurement technique
- uniformity of composition.

The above-listed properties ensure the applicability of a standard definition of linewidth, the essential prerequisite for the certification of a physical linewidth metrology standard. The following sections describes the two SOI-based test structures including provisions which are advantageously incorporated into the test structure design and fabrication to maximize its usefulness for reference-material technology.

## 4. TEST-STRUCTURE DESIGN AND TEST-CHIP FABRICATION

### 4.1 Electrical linewidth test-structure design issues

Following a description of the severe limitations of the designs of existing standard linewidth-cells§ for the subject application, this section reviews four recently-introduced electrical linewidth test-structure design issues which have been incorporated into both the VSW and the SSW options. They result in geometrical characteristics which are not generally familiar to the electrical linewidth metrology community. The first two, short reference-length segments and multiple reference-length segments respectively, apply also to structures that are patterned in other than monocrystalline materials but are particularly advantageous in the subject application. The second two issues, buried-barrier isolation assurance and outside-corner etch-stop tabs, apply exclusively to SOI applications.

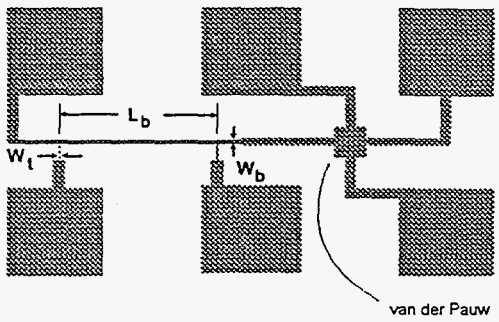


Figure 9. Standard electrical cell for the extraction of sheet resistance and average linewidth, $W_b$, of a length $L_b$ of the reference segment.

#### 4.1.1 Standard Electrical Linewidth Cells

Figure 8 shows the widely-used design of a standard electrical cell for the extraction of sheet resistance and average linewidth, $W_b$, of a length, $L_b$, of the feature identified as its reference segment. The reference segment is part of the extended feature called the bridge. The published designed rules for the standard cell specify that the reference length should be the larger of 80 μm and $15 \cdot W_L$ where $W_L$ is the width of the reference segment.[4] In addition, the design specifies that the Kelvin-voltage tap widths $W_t$ should be less than the reference-segment width $W_b$ , for lengths $L_b$ between 80 μm and 100 μm, and should be less than $1.2 * W_b$ otherwise.

Accordingly, for instances of the cell where the reference segment has submicrometer widths, according to the referenced standard,

- $L_b$ should be equal to, or exceed, 80 μm
- the tap width $W_t$ should have a width less than or equal to the submicrometer reference-segment width $W_b$.

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§ In much of the literature on electrical linewidth metrology, the unit patterns from which linewidth is extracted by probing are commonly referred to as "test structures." However, SEMI International Standards refers to such unit patterns as "cells."

These rules are to ensure that the reference segment has essentially the same electrical and physical lengths.‡ Whereas they are widely observed in practice, they pose certain difficulties for submicrometer applications. The first difficulty is a tendency for electrical failure of the continuity of the voltage taps where they connect to the bridge when the structure is fabricated at the limits of the process window. Provisions enabling the use of arbitrarily wide taps would remove this first difficulty. A second difficulty is that the effective electrical width of the voltage-tap attachments, in practice, is greater than the extended tap's physical width, as a consequence of inside-corner rounding deriving from the limitations of the lithographic replication process. Thus, the true extent of the effective reference-length shortening by voltage-tap width is generally not known. Consequently, whether the intent of the minimum reference-length rule is being satisfied is not known either. Provisions enabling the use of shorter reference lengths would address this second difficulty. In all cases, the traceability of the units in which $W_b$ is expressed derives from the traceability of the reference length identified as $L_b$ in Figure 8.

### 4.1.2 Short reference-length cells with cross-over voltage taps

Fortunately, there exists a proven technique which essentially eliminates the need for the design-rule restrictions generally relating to the specifications for a long reference length with narrow voltage taps as described above. It does this at the expense of minimal extra voltage sampling through one or more additional pads and is quite important for the unique application being described here.[13] The principle of the technique is effectively to measure the extent of reference-length shortening, δL, by a pair of voltage taps having the same arbitrarily-large, widths which do not necessarily have to match the reference-segment width. The value of L, used in conjunction with V/I measurements to provide the electrical linewidth, is adjusted by the measured value of δL. The need of the bridge-length and tap-width restrictions specified for the standard cell in section 4.1.1 above are thereby eliminated to the advantage of the stated mission.

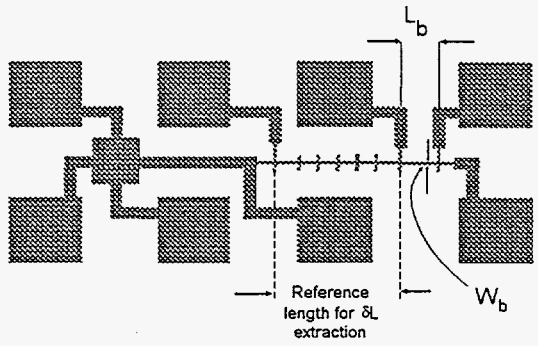


Figure 10. Linewidth cell incorporating provisions for δL measurement and having cross-over voltage-tap attachments.

The basic test-structure layout, which incorporates provisions for δL measurement, is shown in Figure 10. This version may be usefully compared with the standard version shown previously in Figure 8. The cross-over voltage-tap attachments in Figure 10 are recommended in preference to the standard T-type attachments shown in Figure 8.[14] They have been found to render the δL estimates less vulnerable to variations of inside-corner rounding which may derive from fabrication anomalies. Details of the measurement procedure are discussed further in the descriptions of the VSW and SSW test-structure versions in sections 4.2.1 and 4.2.2 below.

As a reminder, the revised electrical linewidth test structure shown in Figure 10 for submicrometer applications is applicable to planar patterned

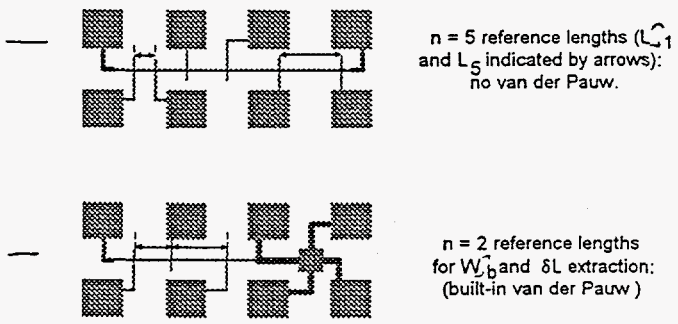


Figure 11. Two variations of a linewidth structure having multiple reference-length segments.

‡ The electrical length of the reference segment is the length of a feature having no attached voltage taps, but otherwise the same physical properties and geometrical cross section as the reference segment, and having an electrical resistance which is the same as the V/I of the reference-length segment measured using the voltage taps.

conducting films regardless of the material used.

4.1.3 Multiple reference-length segments

In the cases of the standard electrical cell shown in Figure 8, and the enhancement shown in Figure 10, the sheet resistance $R_S$ is derived separately from V/I measurements extracted from the van-der-Pauw cross and the reference-length segment. The value of $R_S$ is then used in conjunction with the V/I of the reference-length segment to provide the latter's electrical linewidth, $W_L$.[15] However, the added requirement for an estimate of the value of the voltage-tap induced reference-length-shortening parameter requires the extraction of three unknown parameters $W_L$, $\delta L$, and $R_S$, from a single structure instead of just the usual sheet resistance and linewidth. The way that has been selected to accomplish this in the present work is to connect $n \geq 2$ reference-length segments in series, each reference-length having a different value $L_i$. Two variations of a linewidth structure having multiple reference-length segments are shown in [redacted], Figure 11. One has a built-in van der Pauw box/cross and n=2 reference-length segments, and the other has n=5 reference-length segments but no van der Pauw. Both these structures can be electrically inspected with a 2 × 4 pad set, which is convenient for 2 × 16 and 2 × 32 probe-card configurations.

Whereas n=2 reference-length segments are, in principle, sufficient to allow the extractions of $W_L$ and $R_S$, the multiple-reference length option facilitates identifying the existence of patterning defects which might otherwise render the estimates of these parameters unreliable. When the patterning simply produces random variations in the V/I measurements, the values of $\delta L$ and $W_L$ are given by:

$$W_L = \frac{R_s \cdot \left[ \left( \sum_{i=1}^{n} L_i \right)^2 - 3 \cdot \sum_{i=1}^{n} L_i^2 \right]}{\sum_{i=1}^{n} L_i \cdot \sum_{i=1}^{n} R_i - 3 \cdot \sum_{i=1}^{n} L_i \cdot R_i} \qquad (1)$$

and

$$\delta L = \frac{\sum_{i=1}^{n} L_i \cdot \sum_{i=1}^{n} L_i \cdot R_i - 3 \cdot \sum_{i=1}^{n} L_i^2 \cdot \sum_{i=1}^{n} R_i}{\sum_{i=1}^{n} L_i \cdot \sum_{i=1}^{n} R_i - 3 \cdot \sum_{i=1}^{n} L_i \cdot R_i}. \qquad (2)$$

These equations represent the statististical estimates obtained from the least-squares fit of $R_i$ to a linear function of $L_i - \delta L$.

4.1.4 Oxide barrier isolation assurance

An unknown in the current work is the possibility of leakage from the test structure through the barrier-oxide to the silicon-substrate "ground" by faults relating to barrier-oxide electrical failure.¶ If more than one leakage path exists for a particular eight-pad structure, then it is highly probable that the resulting shunt currents affect the V/I readings. Consequently, the corresponding linewidth estimate will most likely be incorrect.

The approach to managing the unknown extent of this potential problem that was adopted was to provide a means of signaling whether a particular structure was being affected by leakage failure and thereby whether or not the corresponding linewidth estimate should be discarded. A minimum of one pad of each 2 × 16 set was attached

¶ In spite of the fact that CMOS-SOI is a relatively mature technology, the subject application of SOI is using unconventional wafer orientations and processing which could possibly lead to previously unencountered sources of failure.

exclusively to ground, or rather to a "ground plane."†† The ground plane consists of most of the residual surface silicon not assigned to test-structure patterning. All components of the ground plane are electrically interconnected and are isolated by patterning from the test structures. An affirmative test for electrical continuity between the ground-plane pad and any other test pad of a 2 × 16 set signals the likelihood that a structure being tested is affected by a barrier-oxide fault and that the corresponding estimate of $W_L$ should be discarded. The rationale for this approach is that, until the prevalence of barrier oxide failure is determined from further experience, if the oxide barrier below a single structure does experience ground-plane failure, then it is very likely that failures will also have occurred in the barrier oxide below the ground plane. This is because the ground plane has several orders of magnitude more area than any one eight-pad test structure.

Whereas a definitive test of leakage by forcing contact to the substrate silicon would generally be a safer test, the return on extra effort to provide such a facility is considered insufficient until more knowledge of the extent of the problem, if it exists at all, is established.

4.1.5 Corner-compensation techniques

The practice of a layout technique called corner compensation is uniquely necessary for the formation of planar electrical test structures on SOI. The reason is that patterns are formed by an etching process that is resisted exclusively by {111} lattice planes. For example, if a planar rectangular frame of residual material is patterned in monocrystalline material in the fabrication of the SSW option described in Section 3.1.4, the inside "concave" corners are perfectly formed, as indicated in Figure 12. On the other hand, due to the absence of intersecting (111) planes, which ordinarily contain material removal, at the outside "convex" corners, these corners are generally irregularly eroded as the etching initiates.

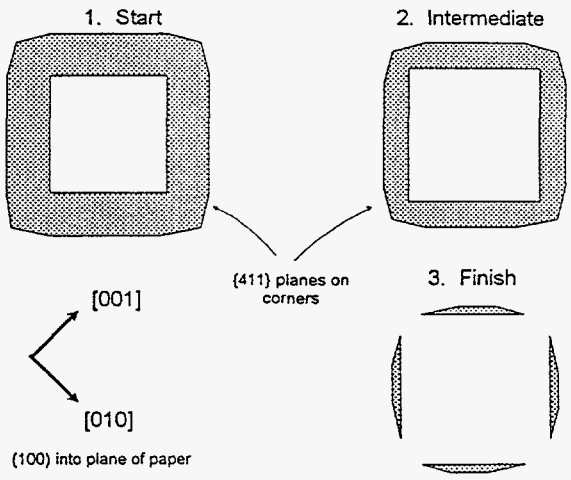


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Figure 12. A rectangular frame having perfectly formed inside corners but outside corners that are irregularly eroded as the etching initiates.

However, so-called corner-compensation techniques can be implemented to protect the desired patterning.[16] In the KOH-silicon system, these techniques are based on the observed tendency of {411} planes also to etch relatively slowly, but faster than {111} planes. The irregular initial etching sooner or later results in the formation of convex corners characterized by {411}-plane erosion as illustrated in the drawing contained in Figure 13.

13

Figure 13. The tendency of {411} planes also to etch relatively slowly sooner or later results in the formation of convex corners characterized by {411}-plane erosion in the SSW implementation. Narrow electrical connections having right-angle turns can be destroyed by the etch as it penetrates in <411> directions as illustrated on the right. Note the retention of crystallographically perfect inside-corner orthogonality.

†† This description applies to the use of the popular 2 × 16 probe-card arrangement which was employed in this work.

Whereas the resultant "rounded" outside corners of large rectangles of material, such as test pads in the present application, may be inconsequential, narrow electrical connections having right-angle turns can be destroyed by the defining etch as it penetrates in <411> directions as illustrated on the right in Figure 13. This optical micrograph derived from our early exploration of overetch effects and attempts to pattern a conventional test-structure layout, with <110> major-axis orientation, in a SIMOX material film having (100) orientation.

Corner-compensation techniques described in reference 16 include the utilization of convex corner extension by tabs, which delay the impact of preferential {411} etching on the required residual pattern. Examples of how the geometries of van-der-Pauw boxes and interconnect turns are modifed to provide pattern protection in the present work are illustrated in Figure 14 for both the VSO and SSW cases.

## 4.2 Test-structure layout

A schematic representation of two variations, distinguished by the presence or absence of a van-der-Pauw box, of characteristics of the basic test structure used for the VSW options, is shown in Figure 15. The two variations facilitate the comparison of linewidth extractions from two-reference-segment structures with those from three-reference-segment structures, in anticipation of a second design iteration.§§

The 2 × 4 padset of a single structure allows the end-to-end placement of four structures for the convenient utilization of a 2 × 16 probe card. However, implementation of structure placements, and the architectures of outside-corner-protector tabs, on the VSW and SSW test chips are necessarily quite different.

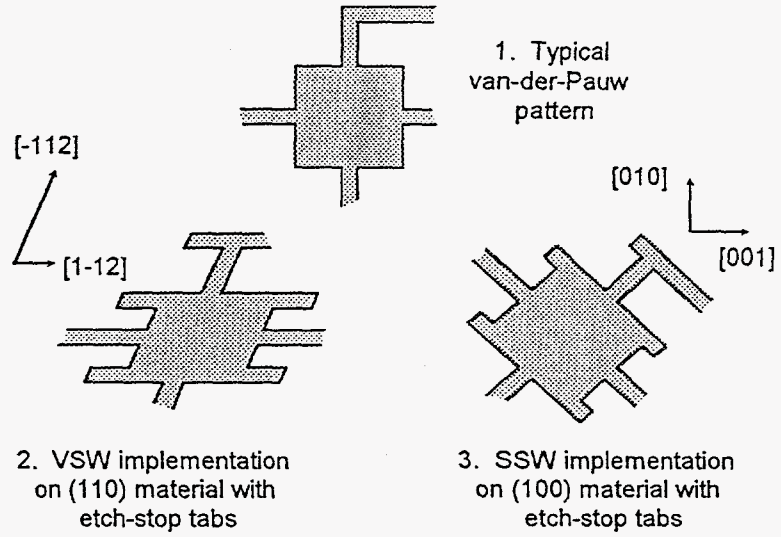


Figure 14. Examples of how the geometries of van-der-Pauw boxes and interconnect turns are modified to provide pattern protection against the KOH etch for both the VSO and SSW cases.

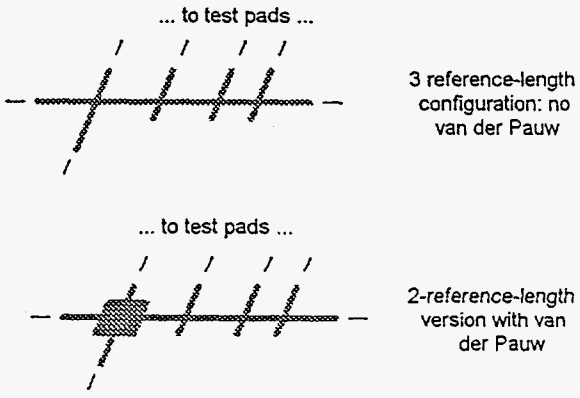


Figure 15. A schematic representation of two variations, distinguished by the presence or absence of a van-der Pauw box, of the basic test structure actually used for the VSW implementation.

They are described separately in later sections 4.2.1 and ~~3~~ 4.2.2

### 4.2.1 Vertical-sidewall (110) VSW version

The design of the basic test structure shown in Figure 15, configured expressly for the case of replication in SOI having a (110) orientation, that is, for the VSW implementation, is shown in Figure 16. Feature edges on the mask characteristically extend in the directions of the[-112] and [1-12] lattice vectors corresponding to the terminations of sidewall {111} planes at the (110) surface. This procedure prevents feature erasure by the KOH etch during pattern transfer from an *in-situ* mask, as described in Section 3.1. In Figure

§§ These versions correspond to cases for n=2 and n=5, respectively, in the equations in sections 4.1.2, 4.1.3.

Figure 16. The basic test structure, shown schematically in Figure 15, configured expressly for the case of replication in SOI material having a (110) orientation.

16, the test-structure bridge is intersected by cross-over taps per the discussion in Section 4.1.2, one intersection serving also for optional van-der-Pauw sheet-resistance extraction as described in Section 4.1.3. The convex corners have etch-stop tab corner-compensation as described in Section 4.1.5. The orientations shown in Figure 16 are consistent with the plane of the paper being a (110) plane, the [110] vector being directed into the paper. Alignment of the principal axes of the structure with the lattice vectors consistent with the scheme in Figure 16 assures perfectly vertical, atomically planar, sidewalls of the reference-length segments and voltage taps.

In test-chip layout, the rectangular ground plane in which the structure is laterally embedded, and which was introduced and described previously in section 4.1.4, is identified in Figure 16. It is electrically connected to the ground-plane sections similarly disposed around other instances of the basic test structure constituting the composite test chip. One pad of each 2 × 4 padset is connected to this ground plane to facilitate buried-oxide-barrier isolation assurance by means described in section 4.1.4. A secondary motivation for providing the ground plane is to conduct away as much electron-beam-induced charging of the exposed oxide layer as possible, for the usual reasons.

Design rules common to all instances of the structure include pad center-to-center spacings of 160 μm. In Figure 16, the wider lines connected to the pads have a width of 10 μm. The nominal lateral proximity of the ground plane to test-structure features is 5 μm. The proximity of the ground plane to the reference length segments is extended to 10 μm to meet requirements of optical inspection.

The reference-segment lengths $L_1$, $L_2$, and $L_3$ in Figure 16 are 8.1 μm, 16.3 μm, and 24.5 μm, respectively.

Various instances of the test structure on the test chip are characterized by different reference-length segment widths $W_b$ and drawn tap widths $W_t$. The twelve combinations listed in Table 1 are those employed, the individual selections recognizing that the wider the tap width, the greater the opportunity for patterning defects to cause undesirable variations of the tap-attachment reference-segment length-shortening parameter-values $\delta L$. Conversely, the narrower the drawn widths, the greater the possibility of encountering CD-related process-window limits and losing connection integrity altogether.

Table 1. The twelve combinations of reference-segment and tap widths used in the VSW implementation.

| Reference-segment drawn width, $W_b$ (μm) | Voltage-tap drawn width $W_t$ (μm) | Reference-segment drawn width $W_b$ (μm) | Voltage-tap drawn width $W_t$ (μm) |
|---|---|---|---|
| 0.25 | 1.00 | 1.50 | 1.50 |
| 0.35 | 1.00 | 1.75 | 1.75 |
| 0.50 | 1.00 | 2.00 | 2.00 |
| 0.75 | 1.00 | 2.25 | 2.00 |
| 1.00 | 1.00 | 2.50 | 2.00 |
| 1.25 | 1.25 | 3.00 | 2.00 |

Figure 17 shows how the individual test structures are arranged on the VSW test chip for probing with a 2 × 16 probe card with minimal probe-head travel. This figure also shows the abutting ground-planes. With the same reference feature orientation relative to the lattice as shown previously in Figure 16, the probe-card is aligned in the [001] direction and travels in either the [-110] or the [1-10] direction.

Figure 17. Arrangment of individual test structures on the VSW test chip well-suited for testing with a 2 × 16 probe card with minimal probe-head travel.

In all, a total of 144 test-structure instances are located within a 15 mm × 15 mm field on the substrate surface. Besides having the different design-rule combinations shown in Table 1, the various instances are also differentiated by their having, or by not having, the van-der-Pauw box and by having, or by not having, the optical/e-beam transmission window shown in Figure 18. In general, the structures were located within the field so that those having the narrower design rules were towards its center. Experience has taught that the process window is a little wider in this region.[17] Regions of the test-chip real estate left unused are allocated to cross-section SEM and STEM inspection targets with their orthogonals designed to coincide with the <112> directions to facilitate optimum cleaving.

With regard to optical and transmission measurements of the width of the reference segments, Figure 18 shows schematically a cross section of a reference segment with neighboring silicon overlying and underlying the barrier layer. The underlying silicon is patterned by the same plane-selective etching as the test structure pattern. Only a selection of test structures has underlying silicon removed in order not to compromise the mechanical integrity of finished samples and to facilitate mask design.

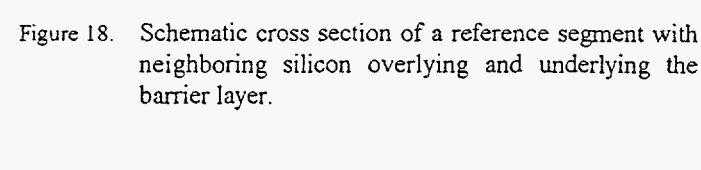

Figure 18. Schematic cross section of a reference segment with neighboring silicon overlying and underlying the barrier layer.

4.2.2 Sloping-sidewall (100) SSW version

The SSW version has several characteristics quite different from those of the VSW structure. First and foremost, the basic unit, characterized by single reference-length and voltage-tap widths, is connected out to a 2 ×16 pad set rather than to the unit 2 ×4 pad set of the VSW version. The scale drawing in Figure 19 shows the orientation of the principal geometric axes of the structure to correspond to <110> lattice vectors within the (100) plane, consistent with the descriptions in sections 3.3.2 and 3.4. Unlike the VSW version, it retains the more traditional provisions for δL-extraction from bridge segments crossed by multiple unterminated voltage taps. The value of δL is assessed by comparing the V/I values of such segments with that of the reference-length segment.

Figure 19. The principal geometric axes of the unit SSW version structure correspond to <1 10> lattice vectors within the (100) plane. The structure retains the more traditional provisions for δL-extraction from bridge segments crossed by multiple unterminated voltage-tap stubs.

The three sets of extended and one-side unterminated voltage taps are hybrid one-dimensional, optically- and electrically-readable, frame-in-frame overlay structures. They are incorporated into the structure because related work reported elsewhere has determined that the electrical-overlay values extracted from them are very sensitive to the consistency of the replication of inside-corner acuities.[18] These different characteristics are incorporated into the version to maximize the technical payback from the investment in the development of these new artifacts.

## 4.3 Wafer-processing and test-structure fabrication

### 4.3.1 Fabrication facilities

The process-technology and fabrication of the metrology linewidth structures is being carried out in the Microelectronics Development Laboratory (MDL) at Sandia National Laboratories. Although the primary work at this 30,000 square foot, class 1 fabrication facility is CMOS and radiation-hardened CMOS, it has been adapted for use in the development of a variety of micromechanical devices and control electronics for those devices using the technologies of surface and bulk silicon micromachining.

### 4.3.2 Applicable experience gained working with devices micromachined from bulk silicon

Historically, work with bulk micromachined devices such as pressure sensors and accelerometers indicate that very high quality surfaces can indeed be defined. This is accomplished by using a class of wet chemical etchants, in this case potassium hydroxide (KOH), which exhibit highly varying etch rates dependent on the exposed crystal surface orientation. For example, the etch rate ratio between the (100) and (111) planes of n-type silicon with a 6-molar solution of KOH at 85°C is over 100. By combining this crystal-plane selective etching and mono-crystalline thin films of silicon, extremely well-defined line cross-sections are anticipated. Important issues include the accurate determination of the etch directions relative to the wafer flat, compensation for convex corners, quality of the SOI

mono-crystalline film material, etchant mask quality, and complete removal of the mask material. The first two items are discussed in some detail below. The latter items are addressed briefly now.

4.3.3 Available SOI material suitability for MEMS-type processing

The quality of the SOI film by SIMOX, in these preliminary results, has proven suitable for the replication of long, continuous, linewidth features without any apparent defects on their sidewalls being decorated by the KOH etchant. Silicon nitride has proven to be the best *in-situ* etch mask material for use with KOH in defining the test features. This is consistent with the literature on the use of KOH for silicon etching. The phosphoric acid removal of the silicon nitride has not produced any deleterious effects while providing suitable removal of the silicon nitride film. The basic process described here addresses the additional issues of crystal direction and corner compensation.

4.3.4 Lithographic-step sequence

The general process which includes accurate determination of the crystallographic direction relative to the wafer flat requires four photolithographic masks. The first two masks are used to determine the proper crystal direction of the wafer surface and, then, alignment to this direction and to provide additional photolithographic features for subsequent masks. The pre-alignment steps use a whole-wafer contact aligner using a mask layer with a pair of rosette patterns which consist of rectangular boxes rotated in tenth degree increments from ±2 degrees. The pair of rosette patterns are along the horizontal centerline of the wafer near the wafer edges to maximize alignment accuracy. The anisotropic KOH etchant is used to etch pits into the silicon. Due to the crystal-plane-selective etch characteristics of the KOH, the pair of rectangular boxes aligned most closely to the proper direction has the most narrow final etch width. Then the second mask in the process, also a contact aligner mask, can be aligned to this pair of boxes. This second mask also contains the definition of alignment features to be used by a stepper aligner and alignment features for backside-wafer alignment if the substrate is to be removed from under the test structures. The reason for switching to a stepper aligner is that the desired features have linewidths under the resolution capability of a whole-wafer contact aligner. Although this is a tedious process, it assures proper alignment of the patterned features to the crystal lattice. This aids in eliminating the stair-step sidewalls which can occur with misaligned patterns.

4.3.5 KOH-etching process

The wafers are cleaned and coated with a 500-Å thick silicon nitride film to be used as the mask for the KOH etch. The silicon nitride is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at 850 °C. This method of depositing the silicon nitride mask film produces the best quality film for use with KOH etching. At this point, the SOI wafer is ready to be patterned with the linewidth test-structures. The pattern is defined in the silicon nitride hard mask using Reactive Ion Etching (RIE). The wafer is immersed in 6-molar KOH at 65°C for several minutes. This readily etches through the thickness of the SOI layer and provides additional etch time to the sidewalls of the features. This overetch of the sidewalls is being investigated as a means to assure that the sidewalls are as close as experimentally practical to single-crystal planes. The extent of overetching required for sidewall smoothing is traded against additional convex-corner compensation. These corners continue to etch back and eventually may lead to open-circuit lines as previously illustrated in Figure 13. One technique to allow greater over-etch times uses corner-compensation as described previously in section 4.1.5. Optimization of the over-etch time and suitability of corner compensation techniques are still being investigated.

After definition of the surface silicon by the KOH etch, the wafers must have the silicon-nitride hard mask removed. Boiling phosphoric acid at 165°C. for 5 m was used to accomplish this. At this point the wafers are ready to be electrically tested.

4.3.6 Material removal for optical and electron-beam transmission window

For those features to be inspected by optical or electron-beam transmission, substrate material is removed from beneath the linewidth-reference segments of a selection of structures. This is accomplished by continuing with the wafers from the above step and depositing another layer of thin (approximately 500-Å thickness) silicon nitride by LPCVD. The fourth contact-aligner mask is now aligned through the wafer to the frontside features and is patterned onto the backside of the wafer. The pattern is etched into the silicon nitride mask which subsequently acts as a hard mask for a KOH etch which etches all the way through the wafer, removing the substrate from beneath the selected frontside

linewidth-reference features. The result, for VSW structures, is reference-segment cross sections shown previously in Figure 18.

Whereas this type of processing is commonly used in the production of bulk silicon etched diaphragm pressure sensors, a major difference here is that the membrane films are much thinner (e.g., several 1000 Å) versus several micrometers as common to pressure sensor diaphragms. This consequently constrains the size of the membrane area and requires better backside-to-frontside alignment. Once the substrate areas are removed, the silicon nitride can once again be removed by a hot phosphoric acid etch, leaving the membranes and mono-crystal silicon linewidth-reference features intact for inspection by optical or electron transmission techniques.

## 5. EXAMPLE OF FABRICATION AND ELECTRICAL TESTING

As a proof-of-concept experiment for this procedure, several wafers of (100) SIMOX material were patterned using an existing mask set (NIST 19) which incorporated standard electrical linewidth test structures (such as in Figure 9) with nominal critical dimensions (CDS) of 1.0 and 2.0 μm. The final structures from these fabrications are not

Table 2. Measured Sheet Resistances and Linewidths

| | Sheet Resistance | | Measured Linewidth | | | |
|---|---|---|---|---|---|---|
| | Rs Ω/□ | Yield (Sample) | 1.0 μm ± σ | Yield (Sample) | 2.0 μm ± σ | Yield (Sample) |
| Sample 1 | 932 ± 36 | 76% (576) | 0.721 ± 0.069 | 75% (384) | 1.762 ± 0.045 | 75% (192) |
| Sample 2 | 1028 ± 34 | 89% (44) | 0.380 ± 0.023 | 93% (30) | 1.387 ± 0.027 | 100% (14) |
| Sample 3 | 1120 ± 38 | 65% (238) | 0.292 ± 0.027 | 62% (156) | 1.303 ± 0.056 | 78% (82) |

intended to be used for comparing different calibration techniques. There are two primary reasons: the first is that these structures do not incorporate features to protect against outside corner removal. The second is that the very long lengths of these lines (250 μm) make them particularly susceptible to rotational alignment errors - for these 250 μm long lines a rotational misalignment of 0.1° leads to an overetching of nearly 0.5 μm. In contrast, this same rotational misalignment for a 10 μm line would lead to only a 0.020 μm overetch. However, these test structures will provide a means for determining if the proposed fabrication procedure would provide test structures that could be calibrated by electrical, and other, means.

Three wafers were used in the proof-of-concept experiment. Each of these wafers was patterned and then scribed to allow for different etch procedures to be performed on each of the partial wafers.

The isolation between pairs of nominally unconnected features was measured on each of the wafer fragments and found to be extremely low on each (i.e., there was *no* measurable leakage). Several of the samples were overetched to the point that key features were missing completely on all sites. Of the possible samples, there were three from which results were derived. The results from these samples are shown in Table 2 along with the yield for each measurement. If the van der Pauw attached to a particular bridge did not function, the bridge resistance used to determine the sheet resistance was the average of other local van der Pauw crosses. The data were derived from two different wafers; the first sample was from a different wafer than the second and third. The data in Table 1 suggest that the linewidths on samples 2 and 3 were likely affected by angular misregistration of the mask relative to the desired crystal planes during the photolithography process - this amount of offset would be caused by angular misregistration of between 0.2° and 0.3° for these bridge resistors with a design length of 250 μm - as well as differing amounts of etch. Sample 3 also reflected an etch effect were the structures near a single corner, and the adjacent edges were etched substantially more than those elsewhere on the wafer. This explains the low yield of the 1.0 μm lines and the relatively high standard deviation of the 2.0 μm lines.

## 6. SUMMARY

The existence of methods divergence in CD metrology poses a serious challenge to the fabrication of reference materials for tasks such as instrument calibration and image-deconvolving algorithm development. A significant source of methods divergence is the unavailability of a standard definition of the linewidth of a feature having an arbitrary and/or unknown cross-sectional geometry and composition. On the other hand, the linewidth of features having known cross sections and material uniformity can readily have their linewidths specified. Consequently, their incorporation into CD-reference materials is an opportunity to relieve the challenge posed by methods divergence. This paper describes the fabrication of substrates uniquely possessing properties required for reference-material certification through the elimination of methods divergence, namely:

- atomically-smooth sidewalls
- definitive cross-sectional geometries
- material uniformity on an atomic scale.

In addition, the fabrication technique provides substrate properties having compatibility with the special requirements of

- electron-beam
- optical
- ion-beam

transmission metrologies.

Initial electrical test results and SEM inspections have been extremely promising, and more definitive measurement data are expected before the end of the year.

## 7. ACKNOWLEDGMENTS

The authors express their appreciation of manuscript reviews performed by Dr. Paul McWhorter of Sandia and Dr. E. Clayton Teague of NIST. Mary Gilliland of Sandia and Colleen H. Ellenwood of NIST are thanked for the extensive CAD work. J.C. Owen, III, performed the electrical measurements at NIST. E. Jane Wilkes, and Janet M. Rohrbaugh provided manuscript editing and related support. The authors gratefully acknowledge the support and encouragement of Dr. Karen Brown of SEMATECH.

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## DISCLAIMER

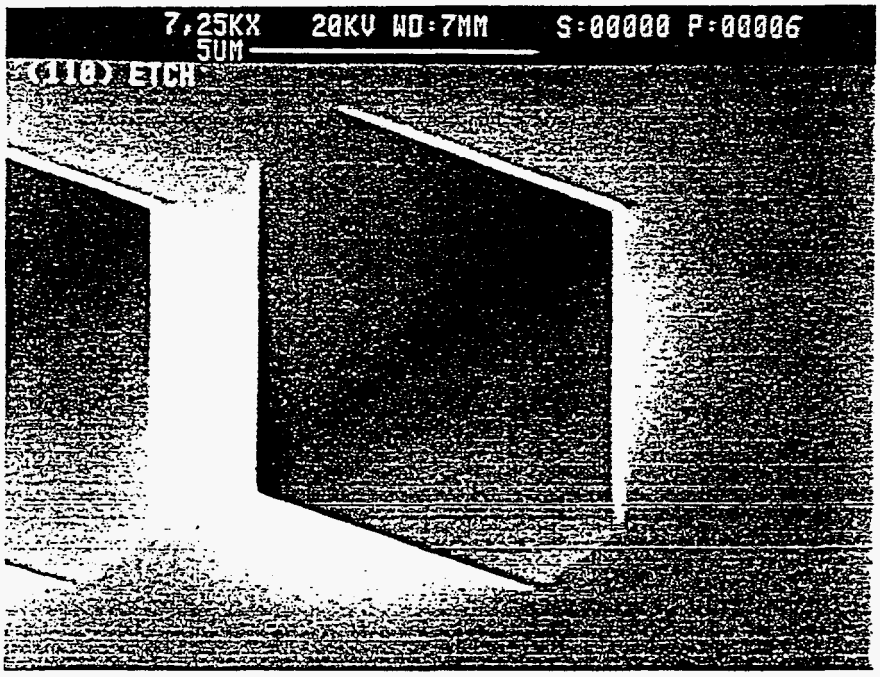



Fig 3

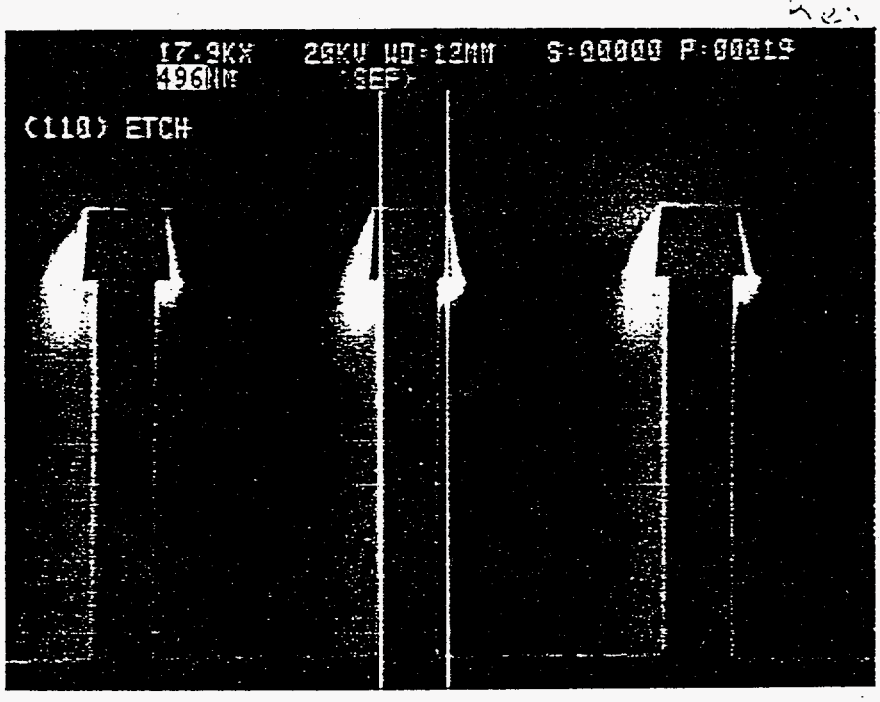
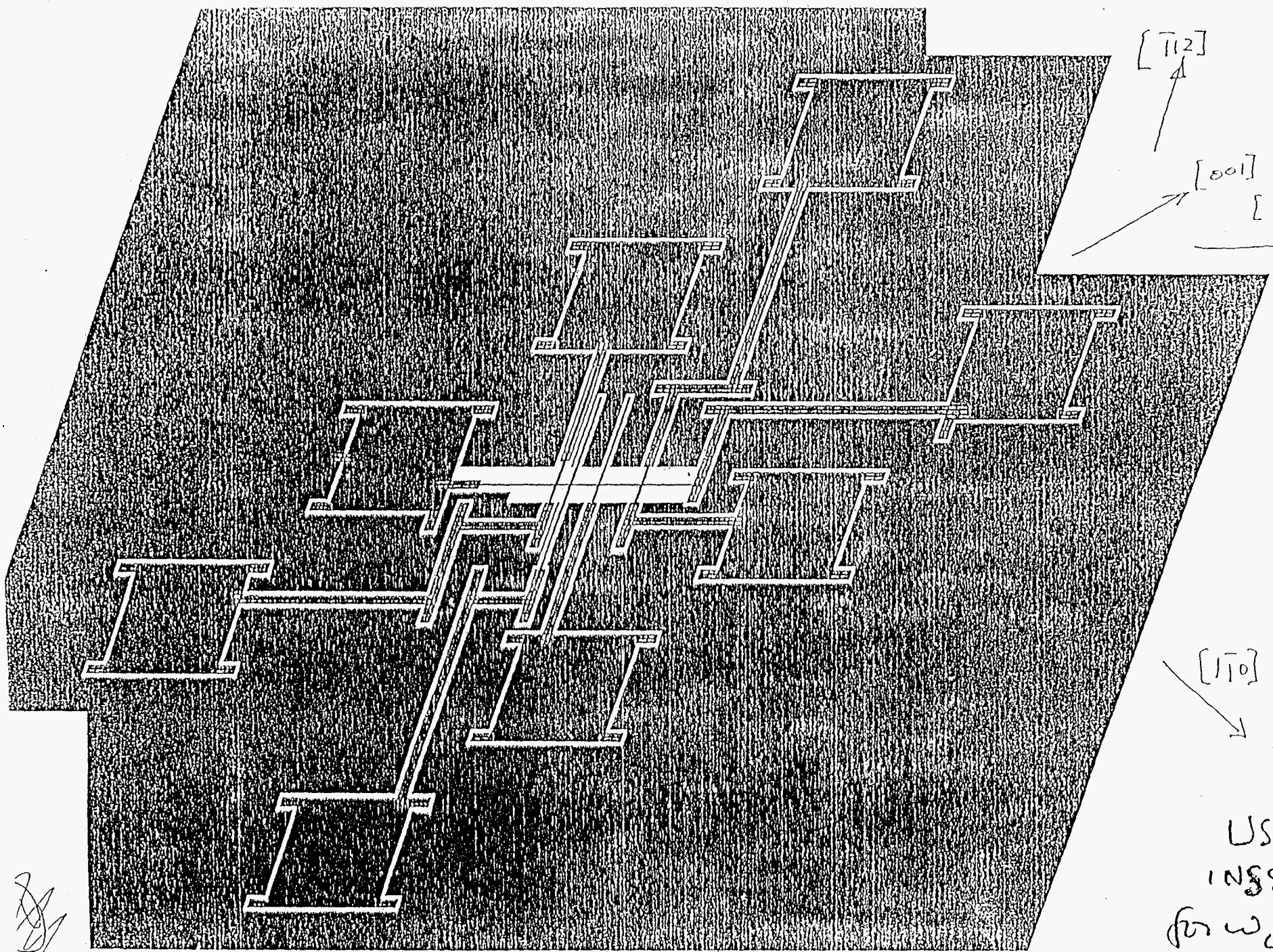



Fig 4




Plane of paper is $1\bar{1}0$ (110).

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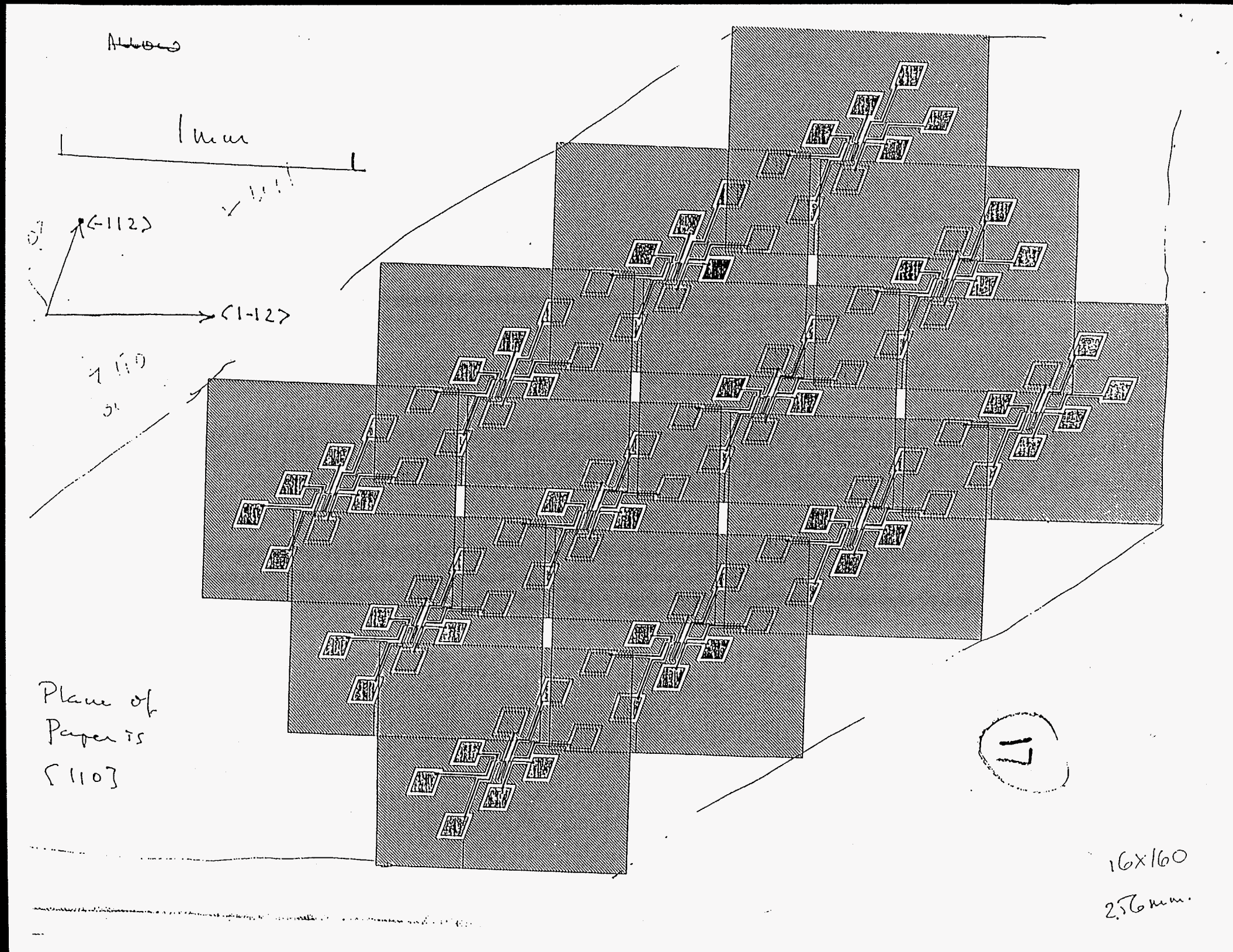
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Plane of Paper is [110]
16x160
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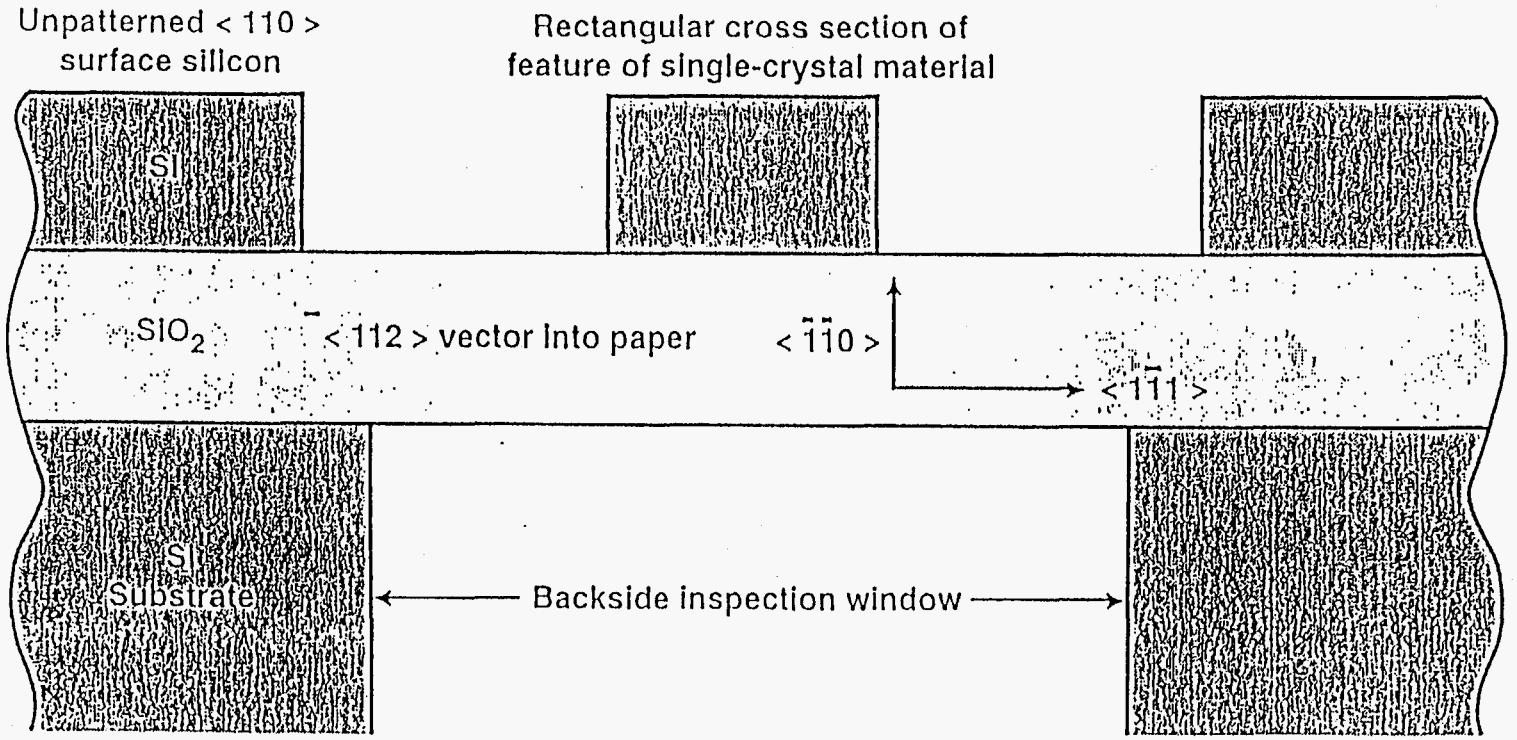
# SOI TEST STRUCTURE FOR LINEWIDTH MEASUREMENT BY ELECTRICAL, SPM, SEM, AND OPTICAL TRANSMISSION METHODS

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