INTERLINE TRANSFER CCD CAMERA

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INTERLINE TRANSFER CCD CAMERA

STATEMENT OF GOVERNMENT RIGHTS

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to charge coupled devices (CCDs) such as those used in camera equipment, and more particularly to an interline transfer CCD image sensing camera with multiple ports, high-speed readout for high framing rate. The camera is predominantly used as an image sensor in high ionization environment, particularly where events of relatively short duration are to be captured.

2. Description of the Related Art

CCDs have been found to be useful as optical sensing devices in camera equipment, and are used to capture visual images and to transform those images into electrical signals. A CCD includes an array of capacitors suitably designed so that they are coupled, and therefore, charges can be moved through the semiconductor substrate in a controlled manner.

When the CCD is used as an image sensor, the individual capacitor locations are arrayed in the form of a rectangle such that there is a plurality of rows, with each row consisting of a series of individual locations. The charge carrying substrates are isolated from the direct effects of exposure to light,
and are placed behind a photosensitive phosphor material.

The photodiodes are usually designed to respond, essentially, to the visual spectrum. However, the camera can be made to respond to wavelengths outside the visual spectrum by using a phosphor that is excited by the desired wavelength, but which emits light in the spectrum to which the photodiodes will respond. The opaque covering on the registers must be such that, while it is resistant to transmittal of photons, it will transfer charge from the photosensitive area to the register layer.

Available CCD sensors, based on how the image is generated and read out, are designated as full frame, frame transfer, or interline transfer type devices. Interline area sensors are generally used in high frame rate video cameras. The image transfer from photosites to opaque charge transport registers takes place simultaneously in interline transfer devices, and can take as little as 1 micro second. Frame transfer CCDs take much longer to shift the whole image into the opaque frame storage area. Full frame imagers do not have storage capability. Unless a light shutter (keeping the image integration and the read out cycles apart) is used, such devices may show a substantial image blur.

In one type of interline transfer type CCDs, there are two photodiodes, called photosites or "pixels", which are directly juxtaposed to each individual register location, with the photosites arranged as alternating "even" and "odd" photosites. After the photosites have been charged by exposure to light, and have transferred their charges to their
corresponding register locations, the registers are then "read out" by one or more charge coupled amplifiers, which produce an electrical output signal proportional to a sensed charge level.

In interline transfer CCDs, images are read out serially under the control of a sequence of clock signals. First, the charges contained in the even photosites are transferred to the registers. Then, the top "horizontal" register row is sequenced to the charge coupled amplifier, and the rows are shifted up one row at a time. The new top row is sequenced past the charge coupled amplifier. These steps are repeated until the entire register set is read out.

In another type of interline transfer type CCDs, the even and odd rows are read out at the same time, and one charge from each row is transferred to the serial readout register with each parallel clock.

Because the charge has been transferred from every other row of photosites to the vertical registers prior to the registers being read out, the reading out of the entire register set results in a sequence of signals which, combined, represent "every other row" of the image, which signals are temporarily stored in a memory.

The charges from the odd photosites are then transferred to the registers, and the registers are read out as described above, to produce a signal for the remaining rows, which signals are combined with the previously captured signals to produce an "interleaved" signal containing all the lines of the picture. Alternatively, the charges from both the even and the odd photosites can be transferred to the registers before the registers are first read out.
In certain applications, such as in test environments where strong ionizing radiation is generated, CCD cameras are used as instruments and measurement devices. These applications place special requirements on recording and imaging systems because of the effects of radiation and shock, especially when the CCD camera is placed in close proximity to the source of radiation.

Conventional high-bandwidth oscilloscopes or streak cameras are presently used as recording instruments for measuring high-bandwidth parameters. Streak cameras are used as recording instruments for spectroscopy (time/energy resolved radiation output), multichannel time-resolved recording and for time-resolved tomography.

The following representative patents reflect the state of the art in the field of imaging using interline architecture in CCD cameras:

Nagai et al., U.S. patent 4,742,395, discloses a high speed video camera having an objective lens and a CCD. The CCD is defined by a photosensor array for producing charge signals representing the image formed thereon by the lens, and a shift register for storing and moving the charge signals in a predetermined direction in response to drive pulses. The CCD has an interline architecture using a fast photogate pulse to replace the mechanical shutter.

Ikeda et al., U.S. patent 4,800,435, describes an image sensing device for a TV camera, and a method of driving a two-dimensional CCD image sensor in a shutter mode. The effective charge accumulation time in each light-sensing row in the imaging area is
reduced to eliminate fuzzy images produced when fast moving objects are picked up.

Kokubo, U.S. patent 4,984,002, describes a charge-coupled imager of interline transfer type, in which an electronic shutter is controlled by varying an effective charge accumulating time (exposure time). The accumulation is started in synchronism with a trigger signal, and the charge is accumulated only during a period of time determined by the shutter speed signal, whereby the accumulating time can be varied in such a manner that the starting of exposure time is made constant, while its ending is varied.

The following patent illustrates the state of the art of interline transfer type CCDs using multiple port readout devices:

Nelson, U.S. patent No. 5,060,245, teaches an interline transfer type image sensing devices, photo-generated charge is transferred from a collection mode into a charge coupled shift register. A CCD image sensing device with multiple outputs for higher framing rate, utilizes alternating shift register orientations and multiplexing of multiple shift registers.

The following patents illustrate the overflow protection and device clearing features in CCD cameras and sensors:

Kokubo, U.S. patent 4,984,002, which is described above.

Turko et al., U.S. patent 5,121,214, describes a method for eliminating artifacts in a video camera,
employing a CCD as an image sensor. This method includes the step of initializing the camera prior to normal read out, and includes a first dump cycle, for transferring radiation generated charge into the horizontal register, while the decaying image on the phosphor is integrated in the photosites. A second dump cycle period occurs after the phosphor image has decayed, for rapidly dumping unwanted smear charge which has generated in the vertical registers.

Suzuki, U.S. patent 4,805,024, describes a still image pick up camera having a solid state image pickup device comprising an image pickup area, a temporary storage area, and a horizontal shift register. The signal charges in the image pickup area are transferred to the temporary storage area by the transfer pulses which are given for a vertical blanking period. Clear pulses are given at a desired timing to enable the photo sensing interval in the image pickup area to be reduced and varied.

The following patent illustrates the high shutter speed feature in an interline transfer type CCD imaging device:

Takemura, U.S. patent 4,839,734 includes a solid-state imaging device having high-speed shutter function. Storage charges are held in a photosensitive section of a CCD, are simultaneously transferred to a high-speed transfer section, in response to a field shift pulse from a driver. The high speed transfer section then transfers the charges to a field memory, in units of lines, and at a high speed.
However, none of the foregoing references combines the features of imaging using interline architecture in CCD cameras, having multiple port readout devices, with overflow protection, and high speed clearing shuttering.

Therefore, there is clearly a need for a high speed readout CCD camera, which combines all the foregoing features, in addition to anti-blooming capability, and which is adaptable for imaging, spectrometer recording applications, and high-bandwidth parameter measurements, particularly in environments where strong ionizing radiation is generated.
SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a camera using a CCD, which produces high quality images, and which is particularly useful for recovering images produced from phosphorescent screens excited by strong ionizing radiation.

It is another object of the present invention to provide a camera using means for reducing the undesirable effects of ionization radiation, using interline transfer charge coupled devices, for fast electronic shuttering.

It is still another object of the present invention to provide a CCD chip with multiple port, and high speed readout, for short shutter times.

It is yet another object of the present invention to provide a CCD chip having anti-blooming capability for saturation control within and outside the imaging area.

It is still another object of the present invention to provide a CCD chip with vertical (orthogonal to the imaging area) overflow protection and fast device clearing, using substrate potentials.

Briefly, the above and further objects of the present invention are realized by an electronic video camera system having an interline transfer type CCD, as its image capturing element, wherein circuitry is provided to accomplish a sequence of events which quickly clears or dumps unwanted charges prior to the image being read out. This feature is particularly
important when it is desired to purge unwanted charges, which are created by strong ionizing radiation, from the charge transfer registers, prior to read out.

The camera system comprises an interline CCD sensing device, which includes an imaging area sensitive to impinging light, for generating charges corresponding to the intensity of the impinging light. Sixteen independent registers sequentially receive the interline data from the imaging area, corresponding to the generated charges.

Sixteen output amplifiers and ports sequentially transfer the interline data, one pixel at a time, in order to supply a desired image transfer speed. The imaging area is segmented into sixteen independent imaging segments, each of which corresponds to one register, one output amplifier, and one output port.

Each of the imaging segments includes an array of 128 rows and 128 columns of pixels. Each pixel includes a photogate area, an interline CCD channel area, and an anti-blooming area. The anti-blooming area is, in turn, divided into an anti-blooming barrier and an anti-blooming drain.

The development of the readout camera system incorporates a number of features, such as multiport fast readout, clear to substrate, anti-blooming drain, interline architecture fast clear, and high speed. The incorporation of all these features in the camera system provides a unique imaging system. With minimum design modifications, the circuit board which holds the imager, and the camera electronics, such as clock drivers, signal processors, analogue-to-digital
converters, data transmitter, and memory, which are modular, could be reconfigured for different imagers. This characteristic allows the use of the camera system for a variety of different applications.
BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features of the present invention and the manner of attaining them, will become apparent, and the invention itself will be best understood, by reference to the following description and the accompanying drawings, wherein:

Figure 1 is a block schematic diagram of a conventional CCD camera system;

Figure 2 is a more detailed schematic block diagram of a portion of a CCD camera system, which is constructed according to the present invention;

Figure 3 is a greatly enlarged block schematic diagram of a pixel architecture used in the CCD camera system of Figure 2, and forming part of a CCD architecture illustrated in Figure 4;

Figure 4 is a diagrammatic representation of a CCD architecture employed in the camera system of Figure 2;

Figure 5 is a simplified schematic top plan view of the CCD integrated circuit chip, according to the present invention;

Figure 6 is a schematic cross sectional view of the CCD integrated circuit chip of Figure 5 taken along line 6-6 thereof; and

Figure 7 is a schematic cross sectional view of the CCD integrated circuit chip of Figure 5 taken along line 7-7 thereof.
Referring now to the drawings and more particularly to Figure 1 thereof, there is illustrated a conventional CCD camera system 10. The camera system 10 includes an objective lens or fiber optic input 11, a CCD image sensor 12, a video signal processor 13, digital memory 14, and a timing and control circuit 15.

Light passes through the lens 11 and focuses the images onto the CCD 12, which converts these images into electrical signals. The passing light impinges onto an imaging area (photosensitive area) of the CCD 12. The imaging area includes a plurality of light-sensing elements which accumulate electrical charges of amounts corresponding to the intensity of irradiated lights for a predetermined period of time. The CCD 12 serves as a solid-state imaging device.

The video signal processor 13 reduces the noise level in these signals, and digitizes the resulting electrical signals, for storage, in a digital format, in the memory 14. The timing and control circuit 15 sets all the timings for the camera system 10.

Figure 2 illustrates a fast scanning, interline transfer CCD camera system 20, which is constructed according to the present invention, and which represents the preferred mode for carrying out the invention. As it will be described later in greater detail, the camera system 20 includes design improvements over the conventional camera system 10, and is equipped with a novel integrated circuitry design, for integrating multiple features, in an
The architecture of the CCD 12 integrates, on a single integrated circuit chip 50, features such as interline architecture, anti-blooming drains, fast clear to substrate, multiple output ports, and high speed readout. None of the conventional devices on the market, or the prior art references, is capable of, or discloses, the integration, on a single device (i.e., integrated circuit chip 50), all the foregoing features, due to the significant design challenges presented by such integration.

The predominant expected usage of the camera system 20 is for capturing images of relatively short duration such as in scientific research work, particularly for those created on phosphorescent screens exited by strong ionizing radiation, wherein an ability to reduce the undesirable effects of ionizing radiation and of high contrast images is most desirable. The preferred mode of the camera system 20 is primarily adapted for capturing single events, rather than a series of events, although the principles of the invention are applicable to either situation.

The camera system 20 is primarily intended for recording images from oscilloscopes, streak, and framing camera systems. The applications for which the millisecond readout camera system 20 is targeted, are generally high-bandwidth parameter measurements or detector imaging. The recording instruments for measuring these parameters are either high-bandwidth oscilloscopes or streak camera systems.
In the preferred embodiment, the camera system 20 is designed to record a 128 x 128 pixels, and to transport the image to a remote recording station, within approximately one millisecond (1 ms) of the experimental event. It should however be understood that the camera system 20 could record a different number of pixel images, for instance, 1024 x 256 pixels.

The camera system 20 has a dynamic range of greater than one thousand (1000), with adequate sensitivity to read single-electron excitations of a CRT phosphor, when amplified by a microchannel plate image intensifier.

Similarly to the camera system 10 of Figure 1, the camera system 20 of Figure 2, includes an objective lens or fiber optic input 21, a CCD image sensor 22, a video signal processor 23, digital memory 24, and a timing and control circuit 15. The camera system 20 is illustrated to further include a system controller 26 and a video monitor 27.

The camera system 20 further includes a command link (not shown), which controls the camera, connected to a fiber-optic transmission system (not shown). An image acquisition sequence can be commanded over this link or can be initiated by an external trigger. A remote control site (not shown) includes a specially designed memory to acquire the high data rate output by a fiber-optic transmission system. Recording and real-time displays are also provided at the control site.
The system controller 26 controls the setup of the camera system 20, and the digital memory 24, and further formats the signals for display on the video monitor 27. The system controller 26 receives the non-standard images from the CCD 22, and formats them into standard video signals, for display on the video monitor 27.

One of the main features of the camera system 20, which is illustrated in Figure 2, is the multi-port architecture, as shown by the sixteen (16) channels (collectively indicated by the numeral reference 28) which connect the CCD 22 to the video signal processor 23, and the sixteen (16) channels (collectively indicated by the numeral reference 29) which connect the video signal processor 23 to the digital memory 24.

Each of the CCD ports (P1 - P16) is connected to a separate channel 28 and 29, for further processing. While Figures 2 and 4 show only sixteen ports (P1 - P16) and sixteen channels 28, 29, it should become apparent to those skilled in the art, after reviewing the present description that a different number of ports and channels can alternatively be selected.

The CCD 22 includes a customized integrated circuit chip 50, which is schematically illustrated in Figures 5, 6 and 7. The CCD chip 50 is designed with 16 parallel output ports P1 through P16 (Figure 4), to supply the necessary image transfer speed. The CCD 22 is designed as an interline structure to allow fast clearing of the image and on-chip fast shuttering. The camera system 20 is designed to be modular and to allow CCD chips of various sizes to be used with minimal re-engineering.
The multiport architecture of the CCD 22 allows the data to be transferred from the CCD 12, at high speed, because of the "segmentation" of the imaging area 41 of the CCD 22 into a plurality of imaging segments. Figure 4 illustrates such a segmented architecture of the CCD 22, into sixteen (16) separate imaging segments A1 through A16. As a result of this segmentation, data is simultaneously transferred, one line at a time (interline architecture), from each one of the imaging segments A1 - A16, to the corresponding serial output registers R1 through R16.

While Figure 4 illustrates sixteen (16) serial output registers R1 - R16, it should be understood to those skilled in the art, that a different number of registers could be selected. Each imaging segment A1 - A16, corresponds to one serial output register R1 - R16. As a result, the transfer speed of the data is increased by a factor equal to the number of segments, i.e., 16, in the preferred embodiment.

It is within the scope of the invention to have a different correspondence between the imaging segments A1 - A16 and registers R1 - R16. For example, it would be possible to have one imaging area, i.e. A6, correspond and be connected to two or more registers, i.e., R6a and R6b, which are included in the register R6.

Each imaging segment A1 - A16 is sensitive to the impinging light, and includes a pixel array, such as an array of 128 by 128 pixels. Figure 3 is an enlarged block representation of a single exemplary pixel 40, which is 25 microns square, and which will be described later.
The data in the imaging segments A1 - A16 is transferred to the corresponding registers R1 - R16, and therefrom, to a plurality of corresponding output amplifiers. In the preferred embodiment shown in Figure 4, the CCD 12 includes sixteen (16) output amplifiers S1 through S16, each of which corresponds to one output register R1 - R16, and to one imaging segment A1 - A16. It should however be understood to those skilled in the art, that alternative designs for the CCD 12 could include other correspondence relationship between the imaging segments A1 - A16, the output registers R1 - R16, and output amplifiers S1 - S16.

Each output amplifier S1 - S16, reads the data in the output registers R1 - R16, serially, one pixel at a time. As a result, the read out speed of the CCD 22 is increased by a factor equal to the number of output amplifiers S1 - S16, which, in the preferred embodiment is sixteen (16). This is referred to as the high speed read out feature, due to the parallel and fast transfer of pixel data.

High speed operation of the CCD is achieved by using metal in conjunction with the conventional polysilicon, for the parallel clock interconnects between the pixels and the columns. By so doing, the effective resistance of the clock transmission lines is reduced, thereby reducing the RC time constant of the parallel clock transmission lines. This allows the device speed, in the preferred embodiment to range between 10 MHz to 40 MHz, with a preferred range of 15 MHz to 30 MHz, compared to conventional speed ranges of 20 KHz to 100 KHz.
Considering now the pixel design in connection with Figure 3, a single pixel according to the present invention generally includes three areas: A photogate area 42, an interline CCD channel area 44, and an anti-blooming area 46.

The photogate area 42 includes a plurality of light sensitive devices, such as photodiodes, which generate photo-charges, when light impinges on the photogate area 42. The photogate area 42 is about 22.5 microns long and 7 microns wide.

The charges generated in the photogate area 42 are transferred to the interline CCD channel 44, for subsequent transfer to the output registers R1 - R16. The interline CCD channel 44 is covered with an opaque aluminum shield 45, for isolation from the direct effects of exposure to light, in order to prevent smearing. The interface area 49 between the interline CCD channel area 44 and the photogate area 42 is negatively charged. The interline CCD channel area 44 is about 22.5 microns long and 9 microns wide.

The anti-blooming area 46 is divided into an anti-blooming barrier 47 and an anti-blooming drain 48. The anti-blooming barrier 47 is rendered negatively charged by appropriate ion implantation techniques that are well known in the art. The anti-blooming drain 48 is positively charged, and is connected to a power supply (not shown), so that it forms an electron sink for the electrons crossing the anti-blooming barrier 47.

When the photogate area 42 is saturated, the electrons exceeding the capacity of the photogate area 42, are drained into the drain 46 for preventing the
"blooming", or the leaking of the excess electrons to adjacent pixels. A negatively charged "virtual" barrier 49 is located at the interface between the photogate area 42 and the interline CCD channel 44. The barrier 49 is more negatively charged than the anti-blooming barrier 47, so that the excess electrons flow in the direction of the anti-blooming area 46 rather than in the direction of the interline CCD channel 44.

Referring now to Figures 5, 6 and 7 there is illustrated (not scale) an exemplary schematic top plan view and two sectional views of the CCD integrated circuit chip 50, with the arrow A showing the direction of the charge transfer. For illustration purpose, the chip 50 is shown to comprise several superposed layers. An n-type silicon layer 51 forms the substrate and is about 200 to 300 microns thick.

A p-type epitaxial layer 53 is about 6 to 12 microns thick and is formed on the substrate 51. A plurality of N-type barrier channels 54 are buried within the epitaxial layer 53, and form a plurality of P+ barriers.

A plurality of metal and polysilicon layers 55 is formed on the epitaxial layer 53, and acts as a gate structure. In the present illustration, a silicon oxide layer 55A is formed on the epitaxial layer 53, and defines a plurality of channel stops 56. A first and second polysilicon layers 55B and 55C respectively are formed on the silicon oxide layer 55A. A first and second metal layers 55D and 55E are formed on the polysilicon layers 55B and 55C.
The imaging area 41, the registers R1 - R16, the transistors S1 - S16, and the output ports P1 - P16 are formed by the epitaxial layer 53. When it is desired to clear the epitaxial layer 53, the positive potential of the substrate 51 is raised, so that the electrons are transferred from the epitaxial layer 53 to the substrate 51, thus achieving fast clear of the entire photogate area 42.

The features and operation of the CCD 22 will now be described in more detail. Reference is also made to the article entitled "Millisecond Readout CCD Camera", by the co-inventors of the present invention, which was published in "Proceeding of the Ultra-High Speed Photography, Videography and Photonics" (July 20-22, 1992), SPIE volume 757. The CCD 22 shown in Figure 4 indicates schematically the 16 serial readout registers and the location of the 16 readout ports. The array includes a total of 256 active rows and six additional light shielded rows, three on each side of the array. Because serial registers are located on both sides of the array, readout requires a total of 131 parallel shift operations. As shown, the 1024 pixel rows are transferred into 8 serial registers at each end of the array. As a result, each serial register includes 128 active pixels plus an additional transfer, for a total of 128 pixel locations per register.

To provide an electronic shutter capability, the interline transfer architecture is used. The interline transfer architecture and the anti-blooming capability require considerable silicon area and, as a result, about only 25.2% of the pixel photogate area functions as a light-acquisition detector.
Two-phase clocking is provided for both the parallel and serial shift operations to enhance rapid readout of the CCD. The implants required for two-phase operation will allow the CCD to be operated in the inverted mode, reducing device dark current to less than 1 na per cm\(^2\), at room temperature. While it is anticipated that most applications will involve very short integrations (1 ms or less), this feature will allow the CCD to be used in applications requiring integration times of several seconds without cooling the device.

The CCD has been designed for use with fiber coupling. As a result, bond pads are placed 30 mils outside the array, to provide space for fiber contact without breaking the bond wires. As a result, the CCD chip 50 has the following overall dimensions: 1.14 inch long and 0.40 inch wide.

In many of the applications anticipated for the CCD, the CCD will receive some overexposure just prior to image acquisition time. This overexposure will result in large numbers of electrons being induced into all device resistors, which must be rapidly cleared prior to acquiring the desired image. A CCD can be cleared of charge by rapid shifting operations. The 1024 x 256 array features a special capability that allows it to be rapidly and continuously cleared until image acquisition time.

In addition to the anti-blooming drain, the fabrication process develops a "vertical" anti-blooming drain that can be biased to sweep out all induced electrons. In operation, this action will proceed as follows. The device will be biased to produce this action until image acquisition time. At
image acquisition time, the bias condition will be removed and a cleared device will begin image integration.

As mentioned above, two-phase clocking is implemented for both the parallel and serial registers. This feature eases the clocking problem for high-speed readout, since only a single complementary clock is required to drive both phases.

In addition to this architectural choice, the CCD includes additional features to enhance high-speed operation.

The parallel gates of the CCD chip extend the full length dimension (1024 pixel) of the array. These polysilicon gates feature finite resistance and distributed capacitance. As such, they represent resistance-capacitance (RC) transmission lines. Even though these lines are driven from both ends of the array, transmission delays limit the rate at which charge can be transferred. To alleviate this problem, additional metallized connections are made to the parallel gates so the RC line effect is minimized.

The high-speed CCD readout includes output amplifiers which not only feature adequate bandwidth to support the readout rate, but also feature relatively high output gains (output volts per sensed electron). This output gain is achieved by fabricating a very small gate capacitance for the sensing out field effect transistor (FET). Cascaded FETs used as FET followers are required to achieve the required bandwidth and to provide some output drive capability. The design of the 1024 x 256 array includes three cascaded FETs with a designed output gain of 10 μV/electron.
The readout time for the CCD device is less than 1 ms. One main application of the CCD device is expected to feature an integration period of approximately 100 μs followed by a readout. Dark current will be negligible in such an application. Double-correlated sampling will be used on each channel.

Based on the noise density and a 20-MHz serial readout rate, a well-designed double-correlated sampling processor should yield an output noise of approximately 25 electrons rms. As a result, the dynamic range defined as the total full-well capacity divided by rms readout noise is 6000. This dynamic range calculation only includes readout noise and does not include other effects such as clocking noise from the conversion and data transmission system or the effects of quantizing noise from the conversion and data transmission system or the effects of quantizing noise from the analog-to-digital conversion process. As a result, an overall system dynamic range goal set at 1000 has been established.

All the clock signals required by the camera system are derived from the data transmission system clock and regenerated by a digital state machine, which provides the serial and parallel clocks and reset pulses required by the CCD. In addition, the state machine provides signals to synchronize the 16 channels of analog-to-digital (A/D) conversion and timing required to transfer A/D outputs to the data transmission link.

Clock drivers are required to provide the analog clocking required by the CCD. These drivers drive significant capacitance loads at the CCD at the rates
required by the readout time. They also have adjustable rails to allow optimization of CCD performance. In addition, a number of fixed potentials are required to operate the CCD. These fixed potentials are variable to optimize individual CCD performance.

Double-correlated signal processing is used in the system to (1) eliminate KTC noise, (2) reduce the effects of 1/f noise, (3) remove output amplifier offset voltages, and (4) limit output noise bandwidth.

Double-correlated sampling requires the implementation of delay, subtraction and filtering functions. The total analog signal processing system includes 16 identical channels, one for each output part of the CCD.

Because of the anticipated high dynamic range of the CCD, the signals from the double-correlated sampling processor will be converted to 10 bits. The conversion is accomplished using a commercially available 10-bit 60-MSPS converter, operational at 20 MHz, to maintain the effective bits of 9.5. Sixteen identical analog-to-digital converters are used.

The total data rate from all sixteen ports at a 20 Mpixels per port rate converted to 10 bits per output is substantial, approximately 3.2 Gbits per second. This amount of data will be transmitted over four fiber-optic links as follows. Four data channels will be combined and transmitted over a single optical fiber. The data transmission system is based on a gallium-arsenide technology to accommodate the very high data rates involved. The complete data transmission system includes circuitry to convert four
10-bit input channels into a single channel, the transmission system, the receiving system and circuitry to convert the received serial stream into four 10-bit received words.

The digital controller provides overall control and interfacing support for the camera and resides in a VXI mainframe and primarily provides the interface between the data acquisition memory and the image processing workstation. It additionally provides the common data bus between data acquisition memory and the video generation card for the pseudo-real time video.

In addition to storing the input data rate, the memory is designed to readout the data to the host in natural image order. That is, it first reads out row 1 in sequential pixel order, followed by row 2, row 3, etc., until the full image has been transferred. The memory has an eight-image depth. In addition to providing for data transfer to the host, the memory also interfaces with a video display card to provide a quasi-real time display capability since the input rate is much faster than the display.

The image processing system provides camera control, analysis, test, and calibration functions. The control includes acquiring and transferring data, real-time video, and file format conversion. The analysis portion includes image dynamic-range scaling, background subtraction, distortion, gain and defect correction, profiling, and MTF unfolding. The test and calibration portions provide the capability to evaluate and correct for such parameters as noise, defects, distortions, gain and offset errors, CTE, and background determination.
While specific embodiments of the CCD camera have been illustrated and described, in accordance with the present invention, modifications and changes of the apparatus, parameters, materials, etc. will become apparent to those skilled in the art, without departing from the scope of the invention.

What is claimed is:
INTERLINE TRANSFER CCD CAMERA

An interline CCD sensing device 22 for use in a camera system 20, includes an imaging area 41 sensitive to impinging light, for generating charges corresponding to the intensity of the impinging light. Sixteen independent registers R1 - R16 sequentially receive the interline data from the imaging area 41, corresponding to the generated charges. Sixteen output amplifiers S1 - S16 and sixteen ports P1 - P16 for sequentially transferring the interline data, one pixel at a time, in order to supply a desired image transfer speed. The imaging area 41 is segmented into sixteen independent imaging segments A1 - A16, each of which corresponds to one register, one output amplifier, and one output port. Each one of the imaging segments A1 - A16 includes an array of 128 rows and 128 columns of pixels 40. Each pixel 40 includes a photogate area 42, an interline CCD channel area 44, and an anti-blooming area 46. The anti-blooming area 46 is, in turn, divided into an anti-blooming barrier 47 and an anti-blooming drain 48.
FIGURE 2
FIGURE 3