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PROGRESS REPORT ON THE ARGONNE-OAK RIDGE DIGITAL COMPUTER

March 5, 1951

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Physics and Mathematics

ARGONNE NATIONAL LABORATORY
P. O. Box 5207
Chicago 80, Illinois

PROGRESS REPORT ON THE ARGONNE-OAK RIDGE
DIGITAL COMPUTER

March 5, 1951

by

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Physics Division

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PREFACE

The AVIDAC (Argonne Version of the Institute Digital Automatic Computer) is to be very nearly an exact copy of the computer being designed and built by the Electronic Computer Project of the Institute for Advanced Study under the direction of Prof. John von Neumann. This is in accord with a policy adopted by ANL at the outset in order to get a working machine as soon as possible. In a field as new as is that of the design and construction of high-speed machines of large capacity, it is to be expected that new developments will arise and improvements will suggest themselves while any particular machine is being built. Since such a computer is a tightly organized complex structure, it is generally not feasible to make such changes during construction, because they may not fit well in the over-all plan. Hence it seemed wise, in undertaking the construction of a second machine for ORNL, to have a breathing space in which to try out certain ideas of this kind and to review the design of the machine as a whole. Accordingly such a period has been provided for in ANL's contract with ORNL for the construction of the ORNL computer. The following report summarizes what has been done to date. It is an interim report, whose primary value is that it has forced those engaged in the work to give concrete expression to what they have been doing and thinking about up to this point.

The report has been prepared jointly by the Applied Mathematics Section and the Computer Engineering Section of the Physics Division. Since this report is being issued only two months after the date on which the contract took effect, it is necessary for the reader to understand that the proposed components, techniques in design and experimentation, schemes for logical synthesis, and even the underlying principles are tentative. Also as this report is primarily for internal distribution, many of the discussions are somewhat brief. It is our intention to issue such interim reports quarterly. A final report will be presented at the end of the development and research period (Phase One of the contract between ORNL and ANL).

In addition to those who helped in preparing this report as listed below,* Messrs. Al Crowley and Mal Burns of Central Shops contributed many practical constructional ideas. Mr. Emerson Mason did much of the detail design work on the magnetic tape drive. Carl Bergstrom, Warren Kelleher, Robert Dennis, James Woody, and Rudolph Klein all contributed in no small measure to progress in this project by their careful work in constructing and testing models and final equipment.

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J.C.C.
D.A.F. March 2, 1951

PROGRESS REPORT ON THE ARGONNE-OAK RIDGE DIGITAL COMPUTER

I. ARITHMETICAL OPERATIONS IN THE MACHINE

I.1. Introduction. In order to understand many of the considerations that enter into the design of the machine as a whole, particularly of the control mechanism, it is necessary to understand the manner in which the arithmetic unit performs arithmetical operations. Most readers are doubtless familiar with the general principles on which the usual desk calculating machines operate. This machine will be substantially of the same character, but there are at least three respects in which one is forced to be somewhat more precise in his understanding of the mathematics of the machine: (1) The machine uses the binary notation; i.e., numbers are represented by a positional notation in which each position may be occupied by either of two signs, rather than by any one of ten as in the decimal notation. Binary arithmetic is less familiar than decimal and also has certain unique features. (2) Since the machine is automatic, provision must be made for it to perform many operations that are often performed by the human operator of a desk machine; e.g., the treatment of signed quantities must be explicitly made automatic. (3) The usual desk machine has a travelling carriage that makes it possible to add a given number at any of a succession of decimal positions in the accumulator. In this machine the accumulator is fixed in position with reference to the adder, so that numbers must be shifted in the accumulator.

This section makes no pretense of being original. It is largely a paraphrase of portions of the excellent report of the Institute for Advanced Study.* The attempt has been made to summarize here such information concerning the functioning of the machine as an arithmetical organ as will be needed to understand later portions of the report.

One further remark should be made. The Arithmetic Unit has to perform various combinatorial and logical operations as well as arithmetical ones. These will be dealt with in a later report. We are here concerned with a minimal set of operations that must be the subject of explicit commands to the machine in order that it carry out arithmetical operations with efficiency. Even within these limitations there are decisions yet to be made as to what orders shall be built into the control, since certain desirable modifications of the operations dealt with here may turn out to be feasible at slight expense in design and equipment, while others may be deemed more costly than they are worth.

* Preliminary Discussion of the Logical Design of an Electronic Computing Instrument," by A. W. Burks, H. H. Goldstine, and J. Von Neumann, Institute for Advanced Study, June 28, 1946.

1.2. Machine Representation of Numbers. We shall use lower-case Latin characters, $a, b, \dots$, to denote real numbers. The absolute value of a number a will be denoted by a^* , and we shall write $a = a_s a^*$, where $a_s = +1$ if $a \geq 0$, $a_s = -1$ if $a < 0$. Let $a^* = a_{-p} \cdot 2^p + a_{-(p-1)} \cdot 2^{p-1} + \dots + a_{-1} \cdot 2^1 + a_0 \cdot 2^0 + a_1 \cdot 2^{-1} + \dots$, where each a_i has the value 0 or 1, so that $a_{-p} a_{-(p-1)} \dots a_{-1} a_0 a_1 a_2 \dots$ is a binary representation of a^* . We define as simply representable by the machine those numbers a such that a^* has a binary representation in which $a_i = 0$ for every $i \leq 0$ and for every $i > 39$. The simply representable numbers are then the $2^{40}-1$ integral multiples of 2^{-30} lying between -1 and $+1$. To each simply representable number we let correspond the number $1-a_s+a$, which is then one of the $2^{40}-1$ integral multiples of 2^{-39} that are ≥ 0 , $\neq 1$, and < 2 . This corresponding number can then be uniquely represented as a positive number of the form $\alpha = \alpha_0 \cdot \alpha_1 \dots \alpha_{39} = \alpha_0 \cdot 2^0 + \alpha_1 \cdot 2^{-1} + \dots + \alpha_{39} \cdot 2^{-39}$, where each α_i may have the value 0 or 1, except that the case $\alpha_0 = 1, \alpha_1 = \dots = \alpha_{39} = 0$ is excluded. The number α thus determined from a (more exactly, the 40-digit binary representation of α thus determined from a) will be called the word for a in the machine, and it is this ordered set of 40 digits that will constitute the machine representation of a . We shall write $\alpha = w(a)$. Conversely, any ordered set of 40 binary digits in one of the registers or storage positions of the machine will be called a word. If it is to be interpreted as a number it is either a bad word, namely $1.0 \dots 0$, which has no uniquely determined meaning, or one of the $2^{40}-1$ good words, $\alpha_0 \cdot \alpha_1 \dots \alpha_{39}$ whose meaning is the uniquely determined simply representable number a such that $\alpha = w(a)$. We shall write $a = m(\alpha)$.

We see immediately that $\alpha_0 = 0$ or 1 according as $a_s = +1$ or -1 (provided α is good), since for simply representable numbers $0 \leq a < 1$ is equivalent to $a_s = +1$ and hence to $\alpha = a = 0.a_1 \dots a_{39}$, while $-1 < a < 0$ is equivalent to $a_s = -1$ and hence to $\alpha = 2+a$, that is to $1 < \alpha < 2$, that is to $\alpha = 1.a_1 \dots a_{39}$. Thus α_0 may properly be called the sign digit of α . We shall call $\alpha_1, \dots, \alpha_{39}$ the magnitude digits of α , and shall write $\alpha^* = 0.a_1 \dots a_{39}$ and $\alpha = \alpha_0 + \alpha^*$. The following relations between simply representable numbers and good words are useful:

$$\begin{aligned} \alpha_0 &= (1-a_s)/2, & a_s &= 1-2\alpha_0 = (-1)^{\alpha_0}, \\ \alpha^* &= (1-a_s)/2 + a, & a^* &= (1-2\alpha_0)(\alpha^*-\alpha_0) = a_s(\alpha-2\alpha_0), \\ \alpha &= 1-a_s+a = 2\alpha_0+a, & a &= \alpha^*-\alpha_0 = \alpha-2\alpha_0, \end{aligned}$$

$$\alpha \equiv a, \text{ mod } 2.$$

The fact that $\alpha \equiv a, \text{ mod } 2$, and that no two distinct simply representable numbers, and no two distinct good words, can be congruent mod 2, has the following effect on the interpretation of the arithmetical operations of the machine: Let $a, b, \dots$ be any real numbers that are congruent mod 2 to $1.0 \dots 0$ or to simply representable numbers and hence to words $\alpha, \beta, \dots$ respectively. Let $f(a, b, \dots)$ be any function of these numbers that is itself simply representable. If ϕ is a word in the machine that is congruent to $f \text{ mod } 2$, then $\phi = w(f)$. This has the consequence that if any set of operations in the machine results in the word ϕ , then these machine operations have resulted in the computation of $f(a, b, \dots)$, even though $a, b, \dots$ may not themselves be simply representable, and even though the bad word $1.0 \dots 0$ may occur in the machine in the course of the operations.

1.3. Addition. Let $a \equiv \alpha$ and $b \equiv \beta, \text{ mod } 2$, where α and β are any words, good or bad, and let $a+b$ be simply representable. Then $\alpha + \beta \equiv a+b, \text{ mod } 2$, and there is a unique good word $\gamma \equiv c = a+b$. (Since all congruences that we shall use are with respect to the modulus 2, we shall henceforth omit explicit reference to the modulus.) If we add α and β in the ordinary way, we obtain a result that may be expressed thus:

$$\begin{array}{r} \alpha_0 \cdot \alpha_1 \dots \alpha_{39} \\ \beta_0 \cdot \beta_1 \dots \beta_{39} \\ \hline \gamma_{-1} \gamma_0 \cdot \gamma_1 \dots \gamma_{39} \end{array} ,$$

where $\gamma_{-1} = 1$ or 0 depending on whether there is or is not a carry from the 0 place. In any case, however, $\gamma_{-1} \gamma_0 \cdot \gamma_1 \dots \gamma_{39} = \gamma_{-1} \cdot 2^1 + \gamma_0 \cdot \gamma_1 \dots \gamma_{39} \equiv \gamma_0 \cdot \gamma_1 \dots \gamma_{39} \equiv a+b$, so $\gamma_0 \cdot \gamma_1 \dots \gamma_{39} = \gamma = w(a+b)$. Thus the desired sum is obtained in the machine by performing addition of the corresponding words in the ordinary way except that any carry generated in the leftmost (sign) position is neglected. We shall denote this operation by $\oplus$, and write $\gamma = \alpha \oplus \beta \equiv \alpha + \beta$.

Thus far it appears that we must provide registers in the machine for the storage of the (word for the) augend, α , for the addend, β , and a mechanism for the addition of two 40-digit numbers without provision for carry to the left of the sign digit. Further, we must either provide a third storage position for the result, or provide for replacing one of the given summands, say the augend, by the sum after the sum has been formed. The latter expedient is adopted. The augend is assumed stored in the Accumulator Register A before the addition operation is commanded, the addend is assumed to be at some known "address" (storage location) in the memory. When the order is given to add the number at the given address to the number in the accumulator, the number in the memory is first transferred to the Storage Register S, the machine sum of the contents of A and S

is formed in the adder, called the plusser, P, and the resultant sum is then transferred to A, displacing the previous augend. Since the operation of the plusser will take a certain amount of time, including carry time, during which the contents of A and S must be fixed so as not to affect the result, and since, to insure complete unambiguity of the result, the augend should remain in A while the sum is being introduced into A, a temporary memory for the result of the addition must be provided. For this, and other reasons to be given when we come to consider multiplication by powers of 2, the accumulator is actually a double register. One of these is called the lower (or permanent) register, A_L , and from it information is transferred to the plusser. The sum is received by the other register, the upper (or temporary) register A^U , without disturbing A_L . Thus when sufficient time has elapsed for the sum to have been formed in the plusser, the sum is transferred to A^U and the connection from P to A^U is broken. The contents of A^U may then be transferred to A_L and the connection from A^U to A_L broken. The connection between A_L and P need not be broken, and in fact is not broken at any time.

I.4. Change of Sign and Its Applications. Let $\alpha, = w(a)$, be a good word, and let $b = -a$. Then b and a are both simply representable. If $a \neq 0$ then $b_S = -a_S$ and $b = b_S b^* = (-a_S) a^*$, so $\beta = 1 - b_S + b = 1 + a_S - a = 2 - (1 - a_S + a) = 2 - \alpha$. If $a = 0$, then $b = 0$ and $\beta = \alpha = -\alpha \equiv 2 - \alpha$. Since $\alpha \neq 1, 2 - \alpha \neq 1$. Hence β is a good word in any case, and is always the unique word congruent to $2 - \alpha$.

Now let $\bar{\alpha}_i = 1 - \alpha_i$ for each digit of α . We call $\bar{\alpha}_i$ the 1-complement of α_i . The complete set of 1-complements of the digits of α forms a word that we denote by $\bar{\alpha}, = \bar{\alpha}_0 \bar{\alpha}_1 \cdots \bar{\alpha}_{39}$, and call the 1's-complement of α . (Note that $\bar{\alpha}$ may be formed from α simply by changing the value of each of the digits of α to the other of its two possible values.) Since $\alpha_i + \bar{\alpha}_i = 1$, then $\alpha + \bar{\alpha} = 1 \cdot 2^0 + 1 \cdot 2^{-1} + \cdots + 1 \cdot 2^{-39}$. Hence $2 - \alpha = \bar{\alpha} + 2^{-39} \equiv \bar{\alpha} \oplus 2^{-39} = \beta$.

Subtraction may now be performed as follows: Let $a \equiv \alpha$ and $b \equiv \beta$, where α and β are any words, and let $a - b$ be simply representable. Then $a - b \equiv \alpha - \beta \equiv \alpha + 2 - \beta \equiv \alpha + \bar{\beta} + 2^{-39} = \gamma = w(a - b)$. We shall write $\gamma = \alpha \ominus \beta$. To carry out this operation in the machine we assume that α is in A_L and β is brought into S from the memory, M. A double set of exits from S to P is provided. One of these provides for the direct transfer of information from S to P, as in addition. The other provides that the information in S shall be complemented as it goes into P, that is, each digit in S is transformed into its 1-complement as it goes into P, so that P receives $\bar{\beta}$. Also, when the complement paths are used, the extra 2^{-39} that must be added to form $\alpha \ominus \beta$ is inserted as a carry into position 39 of P (a carry that is superfluous for addition). Thus P actually forms $\alpha \oplus \bar{\beta} \oplus 2^{-39}$, i.e. $\alpha \ominus \beta$.

The flow of information from S to P is controlled by gates, direct and complement, and β or $\bar{\beta}+2^{-39}$ will be transmitted to P depending on which set of gates is open. If both are closed, no information is transmitted. We must require that at least one set is closed.

The gates from S to P may be controlled for a different purpose. If we wish to add the absolute value of b to a, we may open the direct or complement gates according as the sign digit of β , that is the contents of S^0 , is 0 or 1. If we wish to subtract the absolute value of b from a, the direct or complement gates will be opened according as the contents of S^0 is 1 or 0.

So far every operation described has combined the information in S with that in A_L . If we wish to disregard the information in A_L , we must either have gates between A_L and P or provide means of "clearing" A_L to 0 before the sum in P is transferred to A^U . The latter course is adopted. If each of the operations described so far is preceded by clearing A^U to 0, we have four new operations, which result in the storage in A_L of the word for b, or for -b, or for $|b|$, or for $-|b|$, respectively.

1.5. Multiplication by Powers of 2. Let p be a positive integer such that $1 \leq p \leq 39$. Let a be a number such that both a and $2^{-p}a$ are simply representable. From $a^* = 0 \cdot 2^0 + a_1 \cdot 2^{-1} + \dots + a_{39} \cdot 2^{-39}$ we have $(2^{-p}a)^* = 0 \cdot 2^0 + 0 \cdot 2^{-1} + \dots + 0 \cdot 2^{-p} + a_1 \cdot 2^{-(p+1)} + \dots + a_{39-p} \cdot 2^{-39} + a_{40-p} \cdot 2^{-40} + \dots + a_{39} \cdot 2^{-(39+p)}$, which requires that $a_{40-p} = \dots = a_{39} = 0$ if $2^{-p}a$ is to be simply representable. Since $(2^{-p}a)_s = a_s$ we have $w(2^{-p}a) = 1 - a_s + 2^{-p}a = (1 - a_s)(1 - 2^{-p}) + (1 - a_s + a)2^{-p} = 2\alpha_0(1 - 2^{-p}) + \alpha 2^{-p}$. Now $2(1 - 2^{-p}) = 1 + 2^{-1} + \dots + 2^{-(p-1)}$, so $w(2^{-p}a) = \alpha_0 \cdot \alpha_0 \dots \alpha_0 \alpha_0 \alpha_1 \dots \alpha_{39-p}$. Thus the word for $2^{-p}a$ is derivable from the word for a (assuming both a and $2^{-p}a$ simply representable) by performing p times the operation of shifting the contents of A to the right while retaining the sign digit.

The basic shifting operation could be performed by closing both gates from S to P, transferring the contents of A_L through P to A^U , and then transferring the contents of each position A^i of A^U down and to the right to the position A_{i+1} of A_L . However, since this would require that addition time in P be allowed for, even though no real addition occurs, a separate set of paths from the A_i of A_L directly up to the A^i of A^U is provided. If in the transfer down from A^U to A_L the contents of A_0 is left intact the repetition of the sign digit is taken care of.

If we wish to multiply by 2^p it is easy to see that we must have $w(2^p a) = 2\alpha_0(1 - 2^p) + \alpha 2^p \equiv \alpha 2^p$, since $\alpha_0(1 - 2^p)$ is an integer, which may be accomplished by p repetitions of the operation of shifting the contents of A_L to the left and inserting a 0 in A_{39} . At each stage the contents of A_0 , which was previously in A_1 , must be a_s , since the sign is not changed by

multiplication by 2. Therefore if the result of p such shifts to the left is to be $w(2^p a)$, we must have had $\alpha_0 = \alpha_1 = \dots = \alpha_p$, which is equivalent to requiring that $a_1 = a_2 = \dots = a_p = 0$, which is obviously necessary if $2^p a^*$ is to be less than 1. The basic shifting operation to the left can be accomplished by transferring the contents of A_L up to A^U , and then providing paths by which the contents of each A^i in A^U is shifted down to the left to A_{i-1} in A_L . During the transfer down to the left the contents of A_{39} must be replaced by 0.

In multiplication by 2^p the requirement that $a_1 = \dots = a_p = 0$ is made to insure that $2^p a$ be of the proper size to be simply representable. Failure to observe the limitation will cause the machine to produce spurious results that are incorrect in the leading significant figures, and possibly in sign also. In multiplication by 2^{-p} , however, the requirement that $a_{40-p} = \dots = a_{39} = 0$ is made only to insure the precision of the result in the last significant figures. If the limitation is not observed, the result will only be in error in the 2^{-39} position, which is often tolerable. This raises the problem of rounding off the result.

At least three courses are open: (1) The result is not rounded off at all, which produces a biased error whose magnitude is $< 2^{-39}$ and whose sign is always opposite to that of the quantity approximated. (2) At the end of the shifting process the last digit is always replaced by a 1. This produces an unbiased error, that is, one whose sign is as likely to be positive as negative, regardless of the sign of the original quantity, but its magnitude is $\leq 2^{-39}$. (3) Before the last shift occurs a 1 may be added in what is then the 39th place but is to become the 40th place, and the resulting number is then shifted. This gives an unbiased error of magnitude $\leq 2^{-40}$, and is therefore the most desirable procedure in theory. In practice, however, this requires that the shifting process be interrupted at the last stage and replaced by sending the contents of A_p through P , at the same time inserting a carry in the 39 position of P , transferring the resulting contents of P to A^U and then shifting it down right into A_L . Clearly it is less desirable, though still possible, from an engineering point of view.

The operations described in this section have shown that both A_L and A^U must have multiple exits, suitably controlled by gates. A_L must have exits to P and to A^U . A^U must have exits to A_L along three paths, directly down, to the right and to the left. The exit directly down may be eliminated as it is in the IAS machine by providing that information that is to be transferred directly down from A^U to A_L follow a zigzag path, say by going down right to A_L , directly up to A^U and then down left to A_L . This has the double disadvantage of being longer and of requiring an extra position at the right end of both A_L and A^U to insure that the right hand digit not be lost. When symmetrical toggles are used this procedure has certain engineering advantages, but these considerations do not apply to the asymmetrical toggle that is planned for the Oak Ridge machine.

1.6. Multiplication of Simply Representable Numbers. With respect to precision our numbers are 39-digit numbers since the sign digit does not affect the magnitude of the number. The product of two 39-digit binary proper fractions is a 78-digit binary proper fraction which is not then generally simply representable. It will simplify the discussion of multiplication to extend our notion of representability as follows: A number a will be said to be representable (simply or multiply) if its absolute value a^* is less than 1 and it can be represented as a binary fraction with a finite number of terms; i.e., if a^* can be written in the form $a^* = 0.a_1 \cdots a_n$ for some finite integer n . The word for a representable number a will then be defined as $\alpha, = w(a), = 1 - a_s + a$.

Let a and b be simply representable, let $ab = c$ (which is representable), and let $w(a) = \alpha, w(b) = \beta, w(c) = \gamma$. From $a = \alpha^* - \alpha_0$ and $b = \beta^* - \beta_0$ we have $\gamma \equiv ab = (\alpha^* - \alpha_0)(\beta^* - \beta_0) = \alpha^* \beta^* - \alpha^* \beta_0 - \alpha_0 \beta^* + \alpha_0 \beta_0$. Since $\alpha_0 \beta_0$ is an integer $\alpha_0 \beta_0 \equiv -\alpha_0 \beta_0$. Hence $\gamma \equiv \alpha^* \beta^* - \alpha_0 \beta^* - \beta_0 (\alpha_0 + \alpha^*) = \alpha^* \beta^* - \alpha_0 \beta^* - \beta_0 \alpha$
 $\equiv \alpha^* \beta^* \ominus \alpha_0 \beta^* \ominus \beta_0 \alpha$. Thus when a and b are both positive their product may be obtained in the machine as the product of the magnitude parts of their words, but if either factor is negative this result must be corrected by subtracting β^* or α respectively. Since these terms are not symmetric in the two factors, we shall call a the multiplicand, b the multiplier, $-\alpha_0 \beta^*$ the multiplicand correction, and $-\beta_0 \alpha$ the multiplier correction.

The multiplicand correction can be broken into two parts, one of which may be carried out while $\alpha^* \beta^*$ is being formed. For $\alpha^* \beta^* \ominus \alpha_0 \beta^* \equiv \alpha^* \beta^* \oplus \alpha_0 (\bar{\beta}^* + 2^{-39})$. Since $\beta^* = 0.\beta_1 \cdots \beta_{39}$, $\bar{\beta}^* = 1.\bar{\beta}_1 \cdots \bar{\beta}_{39}$. Hence $\alpha^* \beta^* - \alpha_0 \beta^* \equiv \alpha^* \cdot 0.\beta_1 \cdots \beta_{39} + \alpha_0 \cdot 0.\bar{\beta}_1 \cdots \bar{\beta}_{39} + \alpha_0 (1 + 2^{-39}) \equiv$
 $\sum_{i=1}^{39} (\alpha^* \beta_i + \alpha_0 \bar{\beta}_i) 2^{-i} + \alpha_0 (1 + 2^{-39})$. Regardless of the value of α_0 , for each i just one of the terms $\alpha^* \beta_i, \alpha_0 \bar{\beta}_i$ can be different from 0, since either $\beta_i = 0$ or $\bar{\beta}_i = 0$. Hence only one of these terms need be formed, namely $\alpha^* \beta_i$ if $\beta_i = 1, \alpha_0 \bar{\beta}_i$ if $\beta_i = 0$. Hence we may express γ in the form $\gamma =$
 $\sum_{i=1}^{39} \delta_i 2^{-i} + \alpha_0 (1 + 2^{-39}) - \beta_0 \alpha$, where $\delta_i = \alpha^* \beta_i = \alpha^*$ if $\beta_i = 1, \delta_i = \alpha_0 \bar{\beta}_i = \alpha_0$ if $\beta_i = 0$.

To apply this procedure to the machine in a fairly simple fashion one more modification is required. As the formula stands the summands $\delta_i 2^{-i}$ must be added by forming δ_i , shifting it i places to the right, and adding to the previous sum. This would require that the output of the plusser be capable of being added in at any of 39 different positions. Also, unless the plusser is capable of adding 78 digits, the accumulation of round-off error will be large. Instead we may make provision for shifting the contents of A as follows: Define $\epsilon_i = 0$ for $i = 0, \epsilon_i = (\epsilon_{i-1} + \delta_{40-i}) 2^{-1}$ for $1 \leq i \leq 39$. Then

$\epsilon_{39} = \delta_{39}2^{-39} + \dots + \delta_1 2^{-1}$. ϵ_0 is formed by clearing A. When ϵ_{i-1} has been formed for any i such that $1 \leq i < 39$, ϵ_i may be formed by adding ϵ_{i-1} and δ_{40-i} in P, admitting the sum to A^t and multiplying it by 2^{-1} by transferring it down right to A_p . In this process the least significant part of the product is formed first. As the successive contents of A^U are shifted to the right, the digits that are lost are in places in which no further additions are to be made, so there is no accumulation of round-off error.

The procedure just described requires that the successive partial products be stored in A, and suggests that the multiplicand be stored in S, with provision for separate treatment of α_0 and α^* , that is of the contents of S^0 and of $S^1 \dots S^{39}$. Clearly we must also provide for the storage of the multiplier, which we do by providing a third storage register, Q, the Quotient Register. Q could be a single register like S, but by making it a double register with shifting facilities like A we gain two advantages: First, to form the successive ϵ_i 's we must sense the successive β_{40-i} 's in Q. If at each step we arrange to shift the contents of Q to the right as the sum from P is shifted right in A, the digit to be sensed in Q will always be in the same position, at Q_{39} . The second advantage is that as β is shifted out of Q we may shift the digits dropped from A into Q so that all 78 digits of the product can be preserved. This greatly simplifies multiple-precision operations (that is computations in which more than 39-digit precision is desired). Accordingly, we assume that Q is a double register like A, except that so far we shall not specify the precise arrangements for transferring information into and out of it and between A_L and A^U except insofar as it must clearly be possible to introduce the multiplier from the memory, transfer the last 39 digits of the product to the memory, and perform right shifts coupling A and Q.

Before we go on to consider the final corrections and rounding off, a possible refinement in the formation of the ϵ_i 's may be noted. If $\beta_i = 1$ we must add the contents of $S^1 \dots S^{39}$ to the contents of A through P. If $\beta_i = 0$ the addition of the contents of S to the contents of A may be performed more quickly by not going through P (which requires waiting the full addition time, whether there are carries or not). For if ϵ_{i-1} has sign-digit 0 we may arrange to transfer the contents of $A_1 \dots A_{39}$ up to $A^1 \dots A^{39}$ and at the same time admit the contents of S^0 to A^0 . A^t will then contain $2\epsilon_i$, which may then be transferred down right to A_p as ϵ_i . But the contents of A_0 is always 0 during these 39 steps, of whichever sort, since initially A_p is cleared to 0 and at each later stage the sum $2\epsilon_i$, however formed, is shifted to the right, leaving A_0 untouched. (This assumes that in a right shift A_0 is left intact as it is in a multiplication by 2^{-1} .) In this way, whenever $\beta_i = 0$, an addition time is replaced by the shorter time required for a shift.

If a round-off is desired, the second and more accurate method described in the previous section can be employed without much difficulty. If the 39th step is required to be an addition, regardless of the value of β_1 , a carry can be inserted at the right end of the plusser, so that $2\epsilon_{39} + 2^{-39}$ is formed in P. The ensuing shift puts the first 39 magnitude digits of $\epsilon_{39} + 2^{-39}$ into A_p , which is the desired rounded off result.

The multiplier correction can be made immediately after the 39th step is completed by obliterating the distinction between S^0 and the remaining positions of S and signalling the subtraction of α (the contents of S) from the contents of A_p . The result is, of course, not shifted. The multiplicand correction, adding $\alpha_0(1+2^{-39})$, can then be formed by admitting only $\alpha_0 (=1)$ to P from S, impulsing a carry at the right end of P, and returning the result through A^t to A_p without shifting.

1.7 Division. If a and b are simply representable numbers with $b^* < a^*$, the quotient of b by a will not in general be even representable, much less simply representable. We shall therefore attempt to define a simply representable quotient c by a relation of the form $b = ac + 2^{-39}r$, where some restriction on the size of r is imposed. c is then some approximation to the desired quotient. Instead of defining c directly in this manner, we shall define it by means of the operations, of the type commonly performed in numerical division, that generate it.

Define $r_i = b$ for $i = 0$, $r_i = 2(r_{i-1} - c_{i-1}c_s a)$ for $1 \leq i \leq 39$, where $c_s = a_s b_s$ and $c_{i-1} = 1$ or 0 according as the signs of b and $r_{i-1} - c_s a$ are like or unlike. From this definition these consequences follow: (1) r_i always has the same sign as b. (2) $r_i^* \leq 2a^*$. (3) $b = ac' + 2^{-39}r_{39}$, where c' has algebraic sign c_s and absolute value $0.c_1 \dots c_{38}$.

The first two properties may be proved concurrently by mathematical induction. They clearly hold for $i = 0$. Assume them for $i = k-1$, where $1 \leq k \leq 39$. Then $r_{k-1} - c_s a = b_s(r_{k-1}^* - a_s a) = b_s(r_{k-1}^* - a^*)$. (a) Assume $b_s = +1$. If the sign of $r_{k-1} - c_s a$ is the same as that of b, then $r_{k-1}^* - a^* \geq 0$, so that $0 \leq r_{k-1}^* - a^* \leq 2a^* - a^* = a^*$, $c_{k-1} = 1$, $r_k = 2(r_{k-1} - c_s a) = 2(r_{k-1}^* - a^*) \geq 0$, and finally $r_k^* = r_k \leq 2a^*$. If the sign of $r_{k-1} - c_s a$ is opposite to that of b, then $r_{k-1}^* - a^* < 0$, $c_{k-1} = 0$, $r_k = 2r_{k-1}$; consequently r_k has the same sign as r_{k-1} , which is like that of b, and $r_k^* = 2r_{k-1}^* < 2a^*$. (b) Assume $b_s = -1$. If the sign of $r_{k-1} - c_s a$ is also -1 then $r_{k-1}^* - a^* > 0$, but not $= 0$ since we have agreed to consider 0 positive. Also $c_{k-1} = 1$. Hence $r_k = 2(r_{k-1} - c_s a) = -2(r_{k-1}^* - a^*) < 0$ so r_k has the sign of b, and $r_k^* = -r_k \leq 2a^*$. If $r_{k-1} - c_s a$ is positive, so that $c_{k-1} = 0$ and $r_k = 2r_{k-1}$, then r_k is negative and $r_{k-1}^* - a^* \leq 0$, so that $r_k^* = 2r_{k-1}^* \leq 2a^*$. The induction is complete.

(N.B. Were it not that for simplicity in the machine we require 0 to be positive, our definitions could have been worded so that r_k^* would always be $< 2a^*$.)

To demonstrate the third property multiply the i^{th} defining equation through by 2^{-i} and rearrange, so that one has $2^{-(i-1)}r_{i-1} - 2^{-i}r_i = 2^{-(i-1)}c_{i-1} \cdot c_s a$. If we sum these relations from 1 to 39, all the terms on the left cancel except $2^0 r_0$ (which = b) and $-2^{-39} r_{39}$. If we factor out $c_s a$ from the sum on the right and express the remaining factor in binary notation we have the relation $b - 2^{-39} r_{39} = a \cdot c_s \cdot c_0 \cdot c_1 \cdots c_{38}$. Since $r_0^* = b^* < a^*$, $c_0 = 0$. Hence c_s is the sign and $0.c_1 \cdots c_{38}$ is the absolute value of c' , and $b - 2^{-39} r_{39} = ac'$.

To define the quotient finally we add $2^{-39} ac_s$ to both sides of the last equation. We then have $b - 2^{-39} (r_{39} - c_s a) = ac$, where $c = c_s \cdot 0.c_1 \cdots c_{38} 1$. We may also write this as $b = ac + 2^{-39} r$, where $r = r_{39} - c_s a$. Then $r = b_s (r_{39}^* - a^*)$ and $-a^* \leq r_{39}^* - a^* \leq a^*$, so $r^* \leq a^*$. Thus c is a simply representable approximation to b/a that is uniquely defined, is unbiased, and has an absolute error $\leq 2^{-39}$ in magnitude. While this round-off is equivalent to the less accurate round-off described earlier, we may safely assume that division will be much less frequent than multiplication so that the larger error will be tolerable.

We must next consider how division is to be performed in the machine. In forming the quotient we wish, of course, to form the word for the quotient directly. If $c_s = +1$ there is no problem since $w(c) = c$. If $c_s = -1$ we must form $\bar{c} + 2^{-39}$. Owing to the rounding off $c_{39} = 1$, so $\bar{c}_{39} = 0$ and $\bar{c}_{39} + 1 = 1$, and hence no carries are introduced by the addition of 2^{-39} . Thus we can obtain $w(c)$ when c is negative simply by taking the 1-complement of each quotient digit as it is determined through the 39 steps required to determine c_0 through c_{38} , and then inserting 1 for γ_{39} .

Clearly the dividend b must be put in A initially and the divisor a in S . An initial sign comparison (that is, a comparison of the contents of S and A_0 after the dividend and divisor are in place but before the actual division operations start) will determine whether we uniformly attempt to subtract the divisor from the contents of A ($c_s = 1$) or uniformly attempt to add ($c_s = -1$). This amounts simply to determining whether we admit the contents of S to P through the complement gates or through the direct gates, respectively. This decision is made for every step of the division. If we assume that r_{i-1} has been stored in A_0 and that we are ready to determine γ_{i-1} and r_i , then $r_{i-1} - c_s a$ is already being formed in P . When the addition time has elapsed it has been formed and we can inspect its sign. As we shall see in a moment, the contents of A_0 may not represent the sign of

r_{i-1} , that is, the sign of b . We can, however, compare with the sign of a , which is fixed. Since $c_s = a_s b_s$, $b_s = c_s a_s$. Hence we shall take $c_{i-1} = 1$ or 0; that is, we shall form r_i from the contents of P (which represents $r_{i-1} - c_s a$) or from the contents of A_0 (which represents r_{i-1}) according as the sign of the contents of P agrees or disagrees with $c_s a_s$. This can be arranged before the division operations start by making the consequence of the sign comparison between P_0 and S_0 depend on c_s : If $c_s = +1$ we shall transfer information into A^U from P or up to A^U from A_P according as the contents of S^0 and P_0 are like or unlike. If $c_s = -1$ the operations will be reversed.

According as we transfer in from P or up from A_L we shall have $c_{i-1} = 1$ or 0. However, $\gamma_{i-1} = c_{i-1}$ or $\bar{c}_{i-1}$ according as $c_s = +1$ or -1 . Hence $\gamma_{i-1} = c_{i-1} = 1$ when $c_s = +1$ and S^0 and P_0 are alike, and $\gamma_{i-1} = \bar{c}_{i-1} = 1$ when $c_s = -1$ and S^0 and P_0 are alike. Thus γ_{i-1} depends solely on S^0 and P_0 , without regard to c_s .

When A^U has received the contents of P or A_L , its contents represent $2^{-1}r_i$, whose absolute value, as we have seen, is $\leq a^* < 1$. The contents of A^U is transferred down left to A_L , which multiplies it by 2, to give r_i . Let us examine this in more detail, since it may be that $r_i^* > 1$, so that r_i is not simply representable. r_0 is simply representable by hypothesis, so the initial contents of A are congruent to r_0 . At the beginning of the i^{th} step assume that the word in A_L is congruent to r_{i-1} . If c_{i-1} is 0 this means that $r_{i-1}^* \leq a^* < 1$, so r_{i-1} is simply representable and A_L contains $w(r_{i-1})$. If c_{i-1} is 1, this means that $r_{i-1} - c_s a$ has absolute value $\leq a^* < 1$, so P contains $w(r_{i-1} - c_s a)$ since the words on which it operated were congruent to r_{i-1} and a . Hence in any case A^U receives $w(r_i/2)$, which we may denote by $w(S)$, $= \sigma_0 + \sigma^*$. When the contents of A^U are transferred down left to A_L , A_L then contains $2(\sigma_s + \sigma^*) + \epsilon 2^{-39} - 2\sigma_s$ since the digit σ_s is shifted out at the left end and a digit ϵ appears at the right. We can require that $\epsilon = 0$. Then the contents of A_L are $2\sigma^*$, $2\sigma^* \equiv 2\sigma^* - 2\sigma_s = 2(\sigma^* - \sigma_s) = 2s = r_i$, so the contents of A_L are congruent to r_i . Thus even though the words in A_L do not necessarily represent the quantities r_i , the resulting quotient is correct.

We have not yet provided for the storage of the quotient. While the transfer in or up to A^U is taking place we may insert γ_{i-1} into Q^{39} . When the transfer down left to A_L takes place we may similarly arrange to have a transfer down left from Q^U to Q_L take place, so that γ_{i-1} is then in Q_{38} , and at the same time arrange to have Q_{39} clear to 1, or alternatively, have Q_{39} initially set at 1 and not cleared thereafter. At the end of the last step,

39-i steps later, γ_{i-1} will be in $Q_{38-(39-i)}$, that is, in Q_{i-1} , and Q_{39} will be occupied by 1. Hence Q_L will contain the desired quotient.

Since Q and A may be coupled in left shifts as well as in right, we could allow the dividend to have 78 significant figures by putting $\beta_0.\beta_1\cdots\beta_{39}$ in A_L and $\beta_{40}\cdots\beta_{78}$ in positions 0 through 38 of Q_L . If we then make provision for Q^0 to transfer to A_{39} on a left shift, the extra digits of the dividend will be shifted into A as they are needed while the quotient digits are being shifted into Q . This device could be used not only for double precision computations but also for single precision division by an integer. In the latter case the simply representable number b could be multiplied by 2^{-39} (with the provision that A^{39} empties into Q_0 on the right shift) so that all the magnitude digits of $w(2^{-39}b)$ would be in Q . If the integer a ($<2^{39}$) is replaced by 2^{-39} , which is simply representable, the quotient of $2^{-39}b$ by $2^{-39}a$ could be formed directly.

II. GENERAL DISCUSSION OF DESIGN PRINCIPLES

II.1. Brief Synopsis of Boolean Algebra. At the suggestion of Dr. Householder the techniques of Boolean Algebra have been tried and found very useful in expounding and testing the logical aspects of the design of the machine. Accordingly we shall make use of these methods in the report and shall here give a brief outline of the basic theory.

A system B of entities $a, b, \cdots$ will be called a Boolean Algebra if the entities are subject to a two-termed operation "and" (" a and b " denoted by " ab "), a two-termed operation "or" (" a or b " denoted by " avb ") and a one-termed operation "not" ("not a " denoted by " a' "), and if the system has the following properties:

1) Each of the operations "and" and "or" is

(1.1) universal: that is, if a and b are in the system, so are ab and avb .

(1.2) idempotent:

$$aa = a,$$

$$ava = a.$$

(1.3) commutative:

$$ab = ba,$$

$$avb = bva.$$

(1.4) associative:

$$a(bc) = (ab)c,$$

$$av(bvc) = (avb)vc.$$

(1.5) distributive with respect to the other:

$$a(bvc) = abvac, \quad av(bc) = (avb)(avc).$$

(2) The system contains distinct entities 0 and i that are

(2.1) null elements for "and" and "or," respectively:

$$0a = 0, \quad iva = i.$$

(2.2) identity elements for "or" and "and," respectively:

$$ia = a, \quad ova = a.$$

(3) The operation "not" is

(3.1) involutoric:

$$(a')' = a.$$

(3.2) complementary with respect to the null of each of the operations "and" and "or":

$$aa' = 0, \quad ava' = i.$$

(3.3) dually distributive with respect to "and" and "or":

$$(ab)' = a'vb', \quad (avb)' = a'b'.$$

One can readily define inductively the extension of "and" and "or" to more than two terms, using the notations $a_1a_2\cdots a_n$ and $a_1va_2v\cdots va_n$ in an obvious way analogous to many-termed products and sums. The analogy of "and" relations to products and "or" relations to sums extends further, to the treatment of signs of aggregation in many-termed relations; e.g., $(ab)vc$ may be written $abvc$.

It is readily shown that 0 and i are unique and that $0' = i$. In addition to (1)-(3) the principal tools used in the manipulation of expressions in Boolean Algebra are:

(4) The law of absorption: $a(avb) = avab = a$.

(5) The law of duality: Any identity is transformed into an identity by interchange of "and" and "or."

(6) The law of consistency: $ab = a$ if and only if $avb = b$.

(7) If $ab = ac$ and $avb = avc$, then $b = c$. (From this follows the uniqueness of the complement of any entity.)

In what follows we shall ordinarily denote o and i by 0 and 1 , respectively.

II.2. Basic Vacuum-Tube Circuits and Their Logical Presentation.

We have here collected a set of vacuum-tube circuits that may be regarded as basic in the design of electronic equipment. From these elements may be built up mechanisms of as great complexity as may be desired in order to achieve specific ends. Along with each circuit is given its logical interpretation in terms of Boolean algebra and the number of vacuum tubes used, as illustrated in the first diagram. These diagrams facilitate passage between the logical block diagram and the electronic circuit diagram in designing and checking more complex components.

Before we can give a Boolean representation of the circuits to follow, we must define the meaning of the elements "0" and "1." Most of the circuits described herein are operated at only two different states (what we may call a high voltage and a low voltage) except, of course, during transitions between states. It is largely arbitrary whether we select the "0" or "1" to represent the high voltage (and vice versa for the low voltage), but the following consideration shows that one choice is more convenient than the other.

In analyzing the operation of a given control circuit (for example, one designed to control multiplication), we normally concentrate attention on those states of the circuit which accomplish the desired operation (in this case, multiplication). Let us call them the "active states." Clearly, the distinction between "active state" and "inactive state" can only be drawn roughly, and in some cases is inapplicable. Nevertheless, it is more convenient to use Boolean algebra in tracing through the action of a circuit if "1" is assigned to the "active state." Now it turns out that in most of the circuits employed in this machine, action is accomplished by a low voltage, so we therefore assign "1" to represent a low voltage and "0" the corresponding high voltage. If it is desired to represent the "actual state" of any given wire, this can be done by drawing a vertical arrow near that wire with the head up if action is accomplished by a high voltage, and with the head down if action is accomplished by a low voltage.

II.3 Engineering Design Principles.

After a decision on a type of computer has been made, engineering design principles should be formulated to meet the requirements of memory capacity, speed, and reliability.

First, consider reliability. Reliability is achieved by use of:
 (1) minimum number of components, (2) reliable components, (3) tolerances greater than component variation requires, and (4) built-in checking systems

FIGURE II.1

BASIC VACUUM-TUBE CIRCUITS AND THEIR LOGICAL PRESENTATION

1 $\equiv$ negative action $\equiv a$ 0 $\equiv$ positive action $\equiv a'$

TOGGLES

Symmetric (negative action)

Asymmetric (positive action)

GATES

$$(a_1 \vee \dots \vee a_n) \equiv c$$

$$(a_1 \cdot \dots \cdot a_n) \equiv c$$

' not

$$a \equiv b'$$

$$a \equiv b'$$

$$(a_1 \cdot \dots \cdot a_n) \neq (a_1' \vee \dots \vee a_n')$$

$$\equiv b$$

$$(a' \cdot b) \equiv c$$

$$(a_1 \cdot \dots \cdot a_n)' \cdot b \equiv c$$

$$(a_1' \vee \dots \vee a_n') \cdot b \equiv c$$

FIGURE II.1 (Contd.)

BASIC VACUUM-TUBE CIRCUITS AND THEIR LOGICAL PRESENTATION

that detect and localize errors. Item (1) requires rigorous logical design, and items (2) and (3) require careful engineering. However, item (4), the checking system, always requires additional internal memory space and auxiliary checking equipment. It is not clear where the optimum balance between the desirable amount of checking and equipment lies. For this reason, checking will not be considered in the following discussion.

Second, consider speed and memory capacity: Since it is our purpose to construct a large-scale general-purpose computer, we shall aim to achieve maximum speed and memory capacity but not at the expense of a large amount of accessory components. On this basis we have chosen to design a parallel static computer. Static implies an attempt to avoid the use of capacitance, delay times, etc., for information storage. We shall justify this decision when we discuss the arithmetic and control unit.

In order to obtain an internal memory capacity of at least 1000 words and an access time better than 20 microseconds, we have tentatively decided to use the Williams memory system, operating in parallel fashion.

At the present time, there are three other systems that have been demonstrated. These are the Selectron System, Magnetic Drums, and Mercury Delay lines. The Selectron System, built around the RCA selectron tube, is a fast system but has limited capacity. The Mercury Delay line is best suited to a serial system, but even in this application access time is long. The Magnetic Drum can be built with large capacity, but its access time is also long.

Direct coupling will be employed extensively throughout the machine. Direct coupling is desirable in the present case, because most of the machine will be asynchronous. Also, D.C. voltage shifting and coupling condenser blocking problems due to grid current will not be present. Furthermore, a close examination of the circuits shown in the latter sections will show that direct coupling will not affect the reliability or increase the voltage levels required.

Of course, A.C. coupling problems can be overcome by the use of diode restoration and diode clamping circuits, but these require additional components.

Employment of crystal diode as circuit components must be considered with the following reservations:

1. When considering the complexity of the machine we will not count crystal diodes as passive elements such as resistors but will count them as vacuum diodes. We do not feel that one can say that computing machines employing crystal diodes are either more or less reliable than those without them. A judgment depends on each particular circumstance and on how the crystal diodes are used.

2. A crystal diode will be used only at places where speed or space is required and on condition that the failure of its adjacent components or voltage will not affect its life.
3. The crystal diode should be easily accessible for replacement. Finally, our aim is not only to choose reliable components but also to keep the number of component types to a minimum in order to facilitate servicing.

III. THE ARITHMETIC UNIT

The Arithmetic Unit of the ORNL Computer will consist of three Registers and a Plusser. This section will consider the proposed Registers. They are the Storage, Accumulator, and Quotient Registers; and will be represented by S, A, and Q, respectively.

The Storage Register, S will consist of one bank of forty toggles. The toggles of this Register are represented by $S^n, n=0,1,\dots,39$. This Register serves as an intermediate stage between the Memory and Plusser.

The Accumulator Register, A will be constructed in the following manner. It will consist of two banks, an upper and a lower, of forty toggles each. The toggles of the upper bank are represented by $A^n, n=0,1,\dots,39$, and the toggles of the lower bank by $A_n, n=0,1,\dots,39$, respectively. The five forms of gating in A are:

Form		Symbol
1) "in" gating	$P_n \rightarrow A^n$	$G_{in}(A) *$
2) "up" gating	$A_n \rightarrow A^n$	$G_{up}(A)$
3) "down" gating	$A^n \rightarrow A_n$	$G_{dn}(A)$
4) "right down" gating	$A^n \rightarrow A_{n+1}$	$G_{rt}(A)$
5) "left down" gating	$A^n \rightarrow A_{n-1}$	$G_{lt}(a)$

* P_n represents the nth position in the Plusser.

The Quotient Register Q will be similar to the Accumulator Register. It is to consist of two banks of toggles represented by $Q^n, n=0,1,\dots,39,40$, and $Q_n, n=0,1,\dots,39$. The four forms of gating in Q are:

Form		Symbol
1) "in" gating	$M_n \rightarrow Q^{n+1}$	$G_{in}(Q)^*$
2) "up" gating	$Q_n \rightarrow Q^n$	$G_{up}(Q)$
3) "right down" gating	$Q^n \rightarrow Q_{n+1}$	$G_{rt}(Q)$
4) "left down" gating	$Q^n \rightarrow Q_{n-1}$	$G_{lt}(Q)$

When both Registers are used together, the connections between them are:

- 1) in a right shift $A^{39} \rightarrow Q_0$
- 2) in a left shift $Q^0 \rightarrow A_{39}$

The above sketch shows the gating lines.

The A and Q Registers will be used as follows:

- 1) For additive operations, only A will be used, with operations $G_{in}(A)$ and $G_{dn}(A)$.
- 2) To place a multiplier in Q, only Q will be used, with the operations $G_{in}(Q)$ and $G_{lt}(Q)$.
- 3) To carry out a multiplication after the multiplier is in Q, the two Registers are operated in tandem with a right shift in the following manner.

* M_n denotes the location of the n^{th} bit in the memory.

If Q_{39} contains "1" $G_{in}(A) \& G_{up}(Q)$ followed by $G_{rt}(A \& Q)$

If Q_{39} contains "0" $G_{up}(A \& Q)$ followed by $G_{rt}(A \& Q)$

- 4) To carry out a division after the dividend is in A and Q, the two Registers are operated in tandem with a left shift in the following manner.

If no overdraft $G_{in}(A) \& G_{up}(Q)$ followed by $G_{lt}(A \& Q)$

If overdraft $G_{up}(A \& Q)$ followed by $G_{lt}(A \& Q)$

The appropriate quotient bit is inserted in Q_{39} at the end of each trial subtraction. To facilitate round-off of the quotient, a phantom Q_{40} position containing "1" is programmed with the division order. This causes Q_{39} to contain "1" after each left shift. After the last shift no quotient bit enters Q_{39} , hence the round-off is accomplished.

- 5) To multiply a number by 2^n , n =integer, a shift of both Registers is programmed. If n is positive, a shift of the form $G_{up}(A \& Q)$ followed by $G_{lt}(A \& Q)$ is programmed. If n is negative, A_0 is not cleared, and a shift of the form $G_{up}(A \& Q)$ followed by $G_{rt}(A \& Q)$ is programmed. When n is negative, the round-off of the shifted number can be done by either of two ways, as described in I.5.
- 6) Permutation shifts (i.e., shifts to replace the first and/or last bits of a word by zeros) are programmed in the same manner as multiplicative shifts, but A_0 is cleared to "zero" in a right shift, and Q must be cleared to "zero" by a separate order prior to a left shift.

III.2 Description of A Basic Binary Cell -- The Asymmetrical Toggle. To explain the asymmetrical toggle proposed for the ORNL Computer, it is necessary to describe the two stable states of the toggle, the means of switching from one state to the other, and methods of obtaining a suitable output.

A simplified schematic diagram, Figure III.1 of the toggle is as follows: The toggle itself consists of two triodes T_1 and T_2 having elements P_1, G_1, K_1 , and P_2, G_2, K_2 , respectively. The cathodes of the two triodes are tied together and have a common resistor R_k going to B-. G_1 is tied to ground. The current through the cathode when T_1 is conducting is

$I_k = \frac{B-}{R_k} \cdot R_1, R_2, R_3$, and B^+ are chosen so that $G_2 = -20v$ if the current through T_1 is I_k and $G_2 = +20v$ if the current through T_1 is 0. The cathodes of the two triodes will follow the higher of the two grid potentials; i.e., the

FIG. III.1

FIG. III.2

FIG. III.3

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tube possessing the higher grid potential will conduct, and the other tube will be cut off. Therefore, if T_1 is conducting it will remain conducting since it causes G_2 to be lower than G_1 . Conversely, if T_1 is cut off it will remain cut off since it causes G_2 to be higher than G_1 .

The toggle will be used to represent "0" when T_1 is conducting and "1" when T_1 is cut off.

Two methods of changing the information in the toggle are as follows:

- 1) The toggle initially contains "1"; that is, T_1 is cut off, and T_2 conducts. The toggle may be changed by raising the potential of G_1 above that of G_2 , causing T_1 to conduct. This lowers the potential of G_2 below ground. When G_1 is lowered back to ground, T_1 will still continue to conduct since ground potential is still above the new potential of G_2 .
- 2) The toggle initially represents zero; that is, T_1 conducts, and T_2 is cut off. If the cathode is raised above the potential of G_1 , T_1 becomes cut off. This will cause G_2 to rise above ground potential, and, hence, when the cathode is allowed to go down, it will only go down as far as the potential of G_2 . T_1 will continue to be cut off.

The circuits as shown on following pages are used to accomplish the transfers illustrated in the two cases:

- 1) In Figure III.2, cathode follower control of G_1 .
If no signal appears on G_3 (i.e., G_3 is not of positive potential), then K_3 and G_1 follow G_4 and remain at zero potential. If a positive signal appears on G_3 , then K_3 and G_1 will follow G_3 . The nominal signal will be +30 volts.
- 2) In Figure III.3, cathode follower control of K_1 and K_2 .
 - (a) If P_I is positive, then the cathodes follow the highest of the three grids. If G_I goes sufficiently positive, the cathodes will follow G_1 .
 - (b) If P_I is negative, G_I will have no effect on cathodes aside from grid current flow. (The grid current is limited by grid resistance R_I .)

The signal put on G_3 , as described in Figure III.2, will be called a clear pulse. It clears the toggle to zero, thus making the toggle receptive to a transfer illustrated in Figure III.3. Information that is to be presented to the toggle will be represented by a positive potential at P_I if it is "1" and a negative potential if it is "0." This information will be able to enter the toggle only during the time G_I is positive and only if the toggle has first

been cleared to zero. When P_I is positive, the toggle will change to "1"; otherwise it will remain at "0."

The experimental toggle shown in Figure III.4 was built and tested. In Figure III.4, G_2 was either +20 or -20 volts, and G_0 +100 or -20 volts. These potentials represent "1" and "0," respectively. The toggle was found to require a 00.12- μ s clear pulse and a 0.2- μ s gate pulse (these are minimum time figures). The 10- μ f condenser served to neutralize the input capacitance at G_2 . The resolution time of the output of the circuit at K_0 was 1.0 μ sec.

The following methods may be used to pulse the toggle:

- 1) A "clear" signal on G_1 will make the left side of the toggle conducting. Then a "gating" signal placed on the cathode may follow the clear signal, flip the toggle, and make the right side conducting. Figure III.5 illustrates the pulses recommended for this operation.
- 2) In Figure III.6 the clear and gate pulses occur at the same time, but the gate pulse is longer than the clear pulse by at least 0.2 μ sec. Since the clear signal is higher than the gate signal, the effect of the former will override the latter during the common period. Because the gate signal lasts longer than the clear, the gating action is the same as described in 1 a.
- 3) In Figure III.7, the gating signal and clear signal are arranged in such a way that they always occur concurrently. The gate signal is always higher than the clear signal in amplitude. Thus, if P_I is positive, the gating signal will override the clear signal, and if P_I is negative, the clear will override the gate.

The use of cathode outputs and grid inputs permits multiple interconnections of toggles owing to low output and high input impedances. A possible register design making use of the asymmetrical toggles is shown in Figure III.8. The "P" gating pulses and "C1" clear pulses originate in the dynamic programmer. The operation of the dynamic programmer and its relation to the arithmetic registers are explained in Section III.4.

III.3 A Fast Carry Logical Adder

The speed of operation of the machine as a whole rests on the speed of three operations: 1) access to any specific position in the memory, 2) transfer of information from one position to another, and 3) addition. The design of the machine as a whole as a parallel rather than serial machine provides the most favorable framework for obtaining high speed in all these operations. The use of electrostatic storage (The Williams Memory Tube) achieves satisfactory speed of accessibility. The introduction

FIG. III. 4

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FIG. III.5

FIG. III.7

FIG. III.6

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AUTHOR	CHU
DATE	6-5-51
D.C.V.

TUBES:
TOGGLES 12AT7. CATHODE FOLLOWERS FROM
TOGGLES 12AU7. INPUT GATES 5687

ACCUMULATOR REGISTER FOR
ORNL COMPUTER

FIG. III. B

RD.	AMS-103-0
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of the asymmetrical toggle gives promise of substantial economy of time in transfer operations. There remains the problem of designing a reliable adder of higher speed than the present one. Such an adder is described in this section.

The present adder is a Kirchoff Law type of adder (Figure III.9) in which two of the inputs, the resident digit and the incident digit, switch precisely determined amounts of current through a resistor, while the carry input determines the supply level to the resistor. With binary numbers this results in four possible output voltages. To be specific, with no carry the supply voltage is 211, the summing resistor is 10,000 ohms, and each incident or resident digit "1" switches 5 ma through this resistor. With carry the supply voltage is 161. So we see that the various possible output levels are as follows:

(Carry Input)		(Resident Digit)		(Incident Digit)		(From Summing Resistor)		
CIN	VOLTS	R ↑	CURRENT	I ↑	CURRENT	E OUT	UNIT OUT	CARRY OUT
no	211	no	0	no	0	211	0	no
no	211	yes	5 ma.	no	0	161	1	no
no	211	no	0	yes	5 ma.	161	1	no
no	211	yes	5 ma.	yes	5 ma.	111	0	yes
yes	161	no	0	no	0	161	1	no
yes	161	yes	5 ma.	no	0	111	0	yes
yes	161	no	0	yes	5 ma.	111	0	yes
yes	161	yes	5 ma.	yes	5 ma.	61	1	yes

Combinations of the three inputs produce four output voltage levels, which must be interpreted as "0" or "1," that is, two levels. Also each of the output levels must be measured to determine if a carry has resulted. The interpretation of the carry takes place in the adder, while interpretation of the sum information takes place in another unit--the Digit Resolver. Eight tubes per digit are required in the adder and the digit resolver together.

The speed of addition in any adder is almost entirely a function of the carry time. In the present adder the carry time is about 8 μ seconds.

One of the disadvantages of the Princeton Kirchoff Law type adder is the number of supply voltage levels required. Thirteen d.c. voltage levels are used in the adder and digit resolver. The large number is due to the need for interpreting the adder output voltages, which is done electronically by examining the output voltage to see if it is higher or lower than a certain reference voltage and then switching the proper voltages to the "carry" line and the "sum" line.

FIGURE III.9
KIRCHOFF ADDER

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Effort toward improvement can be made in several directions. First, attention should be given to reducing the number of supply voltages--which will not only simplify the adder but will greatly simplify the machine's power supply. The latter will make practical the use of sources of supply other than batteries--the elimination of batteries is in itself desirable. Second, the carry time should be reduced as far as possible, since this reduces the time of all arithmetic operations in the machine. Third, the number of tubes should be reduced in order to increase the over-all reliability of the machine and reduce the cost of equipment.

Our efforts have been directed toward developing a logical adder since all of these advantages can be realized in such an adder. Consider the addition of two binary numbers, such as

$$\begin{array}{r}
 1\ 0\ 0\ 1\ 1\ 0\ 1\ 1\ 0\ 1\ 1 \\
 0\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0 \\
 \hline
 1\ 1\ 1\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 1
 \end{array}$$

Starting from the right we notice that carry is produced by the second pair of digits (a pair of "1's") and continues until we reach the ninth pair of digits, where two zeros appear. So if we sense the pairs of digits and produce a carry until two "0's" appear and then stop the carry, we have satisfied the carry requirements in addition.

Diagrammatically, a single stage appears as follows:

This gate is arranged so that "carry" will continue through it, or can be started by two "1's," but will only be stopped by two zeros. If we look at this diagram closely, we see that we have all the information here to produce the "sum" also.

C-IN	R	I	SUM	C-OUT
1	0	0	1	0
1	1	0	0	1
1	0	1	0	1
1	1	1	1	1
0	0	0	0	0
0	1	0	1	0
0	0	1	1	0
0	1	1	0	1

If we have two "1's" or two zeros in R and I, that is, if R and I are alike, we put the C-in number in the sum. If R and I are unlike, we invert C-in and put it in the sum column.

The circuit for accomplishing this for one pair of digits is shown in the attached sketch III.10. The circuit arrangement has been tried for a single stage and operates satisfactorily. There is a reduction in signal level along the carry line which will have to be made up by inserting an amplifier at approximately every 10 stages.

Calculations indicate that the speed of the carry will be less than 2μ seconds for 40 stages; so the total addition time should be less than 4μ seconds.

The number of supply lines has been reduced to three for this single stage. When amplifiers are added we don't anticipate using more than 5 supply lines in all.

The number of tubes per stage is 6 as compared to 8 for the present adder. Reduction of the number of tubes has the advantage of improved reliability.

To make further checks we intend to build a ten-stage adder which will permit measuring the carry time and will also allow us to measure the attenuation in the carry line more accurately.

The reliability and freedom from critical components is good in this adder, but further examinations of the components must be made to be certain that $\pm 10\%$ variations in resistors and $1/3$ aging of tubes can occur without disturbing operation.

III.4. The Arithmetic Control

III.4.1. Introduction

The logical design of the arithmetic control for the Oak Ridge Computer has been prepared, and this section attempts to explain the operational aspects of this automatic control. Before considering the operation of the various units of the control, the following general description should provide a foundation for understanding the operational analysis:

A. Static Programmer: Operates as a static system whose function is to position its associated gates as dictated by the function table and A^0 , S^0 , Q_{39} and P_0 if required by the arithmetic operation. After the orders have been read into the function table and A^0 , S^0 , Q_{39} and P_0 are set, the output voltages of the static programmer ("G" Lines) through various gates serve to route the pulses ("P" pulses) generated by the dynamic programmer to program the arithmetic organ.

FIGURE III.10

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LOGICAL BINARY ADDER
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In Figure III.11 parts of the static programmer are identified as follows:

1. T_1, T_2, T_3 and T_4 = Toggles from the function table.
2. A_0 = Sign digit of A_L .
3. S^0 = Sign digit of S^U .
4. $Q_{39} = 2^{-39}$ digit of Q_L .
5. P_0 = Sign digit of the plusser.

B. Dynamic Programmer: Toggles D_1, D_2 , and D_3 (Figure III.11) and the associated gates ("H" gates) generate the action pulses, depending upon how the gates have been set by the "G" voltages. These action pulses serve to cause the data in the registers of the arithmetic organ to be operated upon to perform the dictated mathematical operation. Furthermore, the $\bar{P}$ pulses are used in the final part of the multiplication operation to provide the necessary corrections. Pulses P_{in} or P_{up} and Cl_{up} are coincident on the time axis and are generated in the first part of the cycle. Pulses P_{rt}, P_{dn} or P_{lt} and Cl_L are coincident on the time axis for the second part of the cycle. In the analysis, the first part of the cycle will be designated as n.1, and the second part n.2; n designates the setting of the shift counter. For each cycle of operation four pulses are derived from the dynamic programmer. The first two pulses will be either P_{in} or P_{up} and Cl_u , and the second two pulses will be either P_{rt}, P_{dn} or P_{lt} and Cl_L .

C. Shift Counter: The shift counter is designated by $K_{n,j}$; n can be from 0 to 39 and is used to indicate the particular set value of the counter; j can be either 1 or 2 and is used to indicate period 1 or 2 of the dynamic programmer.

D. Multiplication Corrections: Circuitry required to carry out the multiplication end corrections. In Fig. III, 11 parts necessary to produce the multiplication end corrections are identified as follows:

1. Q^{38} contains digit 39 of the multiplier in Q^u .
2. Toggles I, II, III, IV are toggles from which K_{39}^*, K_{40}^* and K_{41}^* are decoded. Round-off for multiplication, division, and 2^{-n} shifts are controlled by K_{39} . Multiplication end corrections are controlled by K_{40} and K_{41} .

E. Arithmetic Organ: The arithmetic organ performs the mathematical operations upon the data placed in the various registers upon command from the static and dynamic programmer. In Figure III.11 parts of this unit are identified as follows:

1. A^u = upper bank of the accumulator register.
2. A_L = lower bank of the accumulator register.
3. S^u = upper bank of the memory (storage) register.

*39th, 40th, and 41st steps of the multiplication operation.

4. C.G. = complementary gates.
5. P = plusser

III.4.2. Static Programmer

The function table toggles are set to various combinations to produce twelve orders. These orders are listed (Figure III.11) in the chart adjacent to the function table toggles with the appropriate toggle setting for each order. Each of the function table toggles in general controls the following part of the orders: T_1 controls the presence or absence of a clear; T_2 determines when shift counter is used; T_3 determines whether the data that passes through the complementing gates is complemented, or directly transferred; and T_4 selects the absolute magnitude of the number or the number itself. The combination of T_1 and T_2 will control the G_{rt} , G_{lt} , and G_{cl} output.

The gate voltages of the static programmer are controlled from four sources:

- (a) The function table toggles.
- (b) The asymmetrical toggles A^0 , S^0 , Q_{39} , and P_0 .
- (c) Voltage outputs of other gates.
- (d) a , b , $\overline{Gd}$, β , γ , voltage lines from the gates and toggles of the multiplication correction section.

Each of the above sources plays a particular part in setting up for the execution of the machine orders. The asymmetrical toggles A^0 , Q_{39} , and P_0 have no part in setting the gates of the static programmer for the clear, hold, and single shift orders. S^0 does contribute since it must be referred to for setting the gates for the magnitude orders. Q_{39} is used only during multiplication to determine the gate settings for the programming of G_{in} , G_{up} , $G_{s0} \rightarrow A^0$ and $G_{A^0} \rightarrow A^0$. A^0 , S^0 , and P_0 control gates during the division operation so as to determine G_{comp} , $Q=1$, G_{in} , and G_{up} . a , b , $\overline{Gd}$, β , and γ , remain constant during all the orders except for multiplication. The static programming is altered during the multiplication process by changing a , b , $\overline{Gd}$, β , and γ , at the appropriate time. This changes the routing of the dynamic pulses to permit the additional operations required to make the multiplication corrections. Gate "G" functions only on a division operation so as to transfer the reverse of the sign digit of A^0 to T_3 to allow an initial comparison of the divisor sign digit and the dividend sign digit. This comparison establishes the G_{comp} output. At the same time a comparison of S^0 and P_0 will produce a G voltage output at $Q=1$. The G_{comp} output and $Q=1$ are fed to a simple adder (C^s , D^s , E^s , F^s) to determine whether G_{in} or G_{up} is programmed. Once the complement gates are set by the initial comparison they do not change throughout the division process. P_0 thereafter does change, and the comparison of S^0 and P_0 will determine $Q=1$. If the adder senses an overdraft, the partial remainder in

P is rejected, and G_u is programmed. Otherwise, the partial remainder is accepted, and G_{in} is programmed. The complementary gates are set for direct transfer during the multiplication operation by attaching the multiplication line to gate Y. The $Q=1$ output is incapacitated for all operations except for division by attaching the divide line through an inverter to gate Z. The G line voltages control the accumulator, and the Q registers are a slave of the accumulator. Section III.1 of this report explains the related actions of the accumulator and the Q registers.

III.4.3. Dynamic Programmer

The static state of the programmer prior to starting is one that establishes the "P" voltage levels at approximately -10 volts and the clear voltage levels at approximately 0 volts. When the start signal changes toggle D_1 (Figure III.1) from 0 to 1, a P_{in} or P_{up} positive pulse (approximately +40 volts) is generated, depending upon which one is programmed by the static programmer. At the same time Cl_u (positive pulse approximately +30 volts) changes D_2 and D_3 from 0 to 1. After P_{in} or P_{up} has returned to its quiescent level of approximately -10 volts, the second pair of pulses P_{lt} , P_{rt} , or P_{dn} depending upon the static programmer, and Cl_L are generated. Cl_L will change toggle D_2 and D_3 back to 0, and another cycle can begin if P_{rt} , P_{lt} or P_{dn} has returned to its quiescent voltage level. The above cycle will continue until toggle D_1 is changed back to 0 by the stop signal. The stop signal is generated by Cl_u . During multiplication after the stop signal is generated, $\bar{P}_{dn}$ will be the final pulse generated, and it is used to reset toggles I and II of the multiplication corrections section.

III.4.4. Carry Delay for The Dynamic Programmer

During the multiplication and division operations some of the processes require more time for completion than others. For multiplication Q_{39} indicates whether the multiplicand will be transferred from S^u through P into A or the partial remainder be shifted up and down to the right with the insertion of the proper sign digit. If the multiplicand passes through P, it will be added to the contents of A_L (partial remainder). This gives rise to a series of carries dependent upon the character of the multiplicand in S^u and the partial remainder in A_L ; whereas for a transfer up and down to the right in the accumulator there are no carries instigated. Thus, the pulses from the dynamic programmer must be programmed properly to allow enough time between dynamic pulses, as necessary, to permit the carry operations to be completed. During division, the divisor and the dividend or partial remainder will be added in P for each of the division processes. This causes carries to occur continuously throughout the division operation. For any clear orders involving the use of the complement and for all hold orders, carries will arise. Clear orders not involving the complement will not produce carries.

Figure III.12 is a logical diagram of the carry delay to be incorporated in the dynamic programmer. Pulses $\bar{P}_{rt}$, P_{lt} , and $\bar{P}_{dn}$ are the same as those illustrated in Figure III.1 (Dynamic Programmer). These pulses will be at a positive value during n.1 and then become negative during n.2. Toggle D_1 and gate H_4 of Figure III.12 represent the same toggle D_1 and gate H_4 shown in Figure III.1. B_1 is a one-shot multivibrator which is triggered by a negative input pulse to produce a positive output pulse with a duration of sufficient length to permit the carries to be completed before n.1 starts. The delay for the various operations will be controlled as follows:

(a) Multiplication: If $Q_{39} = 1$, a delay must be inserted; if $Q_{39} = 0$, the delay is not necessary. Therefore, when $Q_{39} = 1$, gate F is opened by Q_{39} , X line from the static programmer and $\bar{P}_{rt}$. The output of gates F and E causes the one-shot multivibrator to produce a positive pulse. The n.1 pulse of the dynamic programmer cannot be generated until the positive pulse of the multivibrator has returned to a negative value. If $Q_{39} = 0$, gate F will remain closed, and the multivibrator is not triggered; thus n.1 will begin after n.2 as usual. Gates C and A cannot affect the multivibrator during multiplication since the divide line voltage and the hold line voltage are positive.

(b) Division: The start signal changes D_1 to 1 and also triggers B_1 via gates D, C, and E, introducing a delay before n.1; thereafter B_1 is triggered by $\bar{P}_{lt}$ to produce the delay before n.1. This procedure causes a delay throughout the entire division operation. Gates F and A remain closed during division and do not affect B_1 .

(c) Clear Orders: Gates A, C, and F are closed; thus the delay is not inserted for any clear order.

(d) Hold Orders: The start signal and the hold line open gate A, which triggers B_1 . This produces a delay before n.1 for each of the hold orders. Gates F and C remain closed.

III.4.5. Shift Control Counter

The internal mechanism of the shift control counter is adequately described in section V.2 of this report. Therefore, this section is only concerned with the integration of the counter with the arithmetic control, the utilizing of the counter information, and a means of triggering the counter.

At the start of any operation requiring a definite number, n, of repeated steps it is necessary to insert n into the shift control counter as a limit. This can be done by either presetting the counter to "0" and recognizing the number, n, as a stop signal or by setting the counter to $m - n$ (m is the module of the counter) and recognizing the appearance of "0" as a

FIG. III.12

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stop signal. The choice between these two methods depends on the relative complexity of variable setting and variable input circuits.

In an operation using the counter it will be pulsed by the Cl_u and Cl_l lines of the dynamic programmer. Appropriate gating techniques will cause the counter to be one-half cycle ahead of the register; this will allow an adequate resolving time for the control.

III.4.6. Multiplication Round-off and Correction Controls

Referring to Figure III.11, toggles Q^{38} , I, II, III, and IV effect the programming only near the end of the multiplication operation. When the multiplication process reaches $K_{38.2}$, gate C_4 opens, causing toggle I to change to 1. This introduces a carry insert to the data in P. Changing toggle I causes gate C_5 to open; γ closes gate J and opens gate N of the static programmer; G_{in} is made active, and G_{up} is inactive regardless of the contents of Q_{39} . If $Q^{38} = 0$, toggle III is changed to 1 at 38.2; gates C_{12} and C_{13} are opened, which closes gate S^* between S^u and the complementary gates. The shift counter then changes to K_{39} at n.1. Toggle II is changed to 1 when $\bar{P}_{rt}$ and K_{39} open gate C_3 , and if toggle III has not previously been changed by Q^{38} , it is changed when gate C_3 opens. Now that toggles II and III have both been changed to 1, S^T opens gate S^* , and the complement output of the corrections section programs complementation. γ is changed since gate C_5 is closed when toggle II changes to 1; thus Q_{39} resumes control of G_{in} and G_{up} . The complement output of gate C_{14} and Cl_u changes toggle IV to 1. " a " closes gate U of the Static Programmer, inactivating G_{rt} ; and $\bar{G}_d$ opens gate W, activating G_{dn} . Now the static programming is complete to allow for the multiplier correction. After the multiplier correction has been made, $\bar{P}_{dn}$ opens gate C_7 and gate B_5 , toggle III is reset, and S^0 is transferred into Q_{39} to determine if multiplicand correction is to be made. Resetting toggle III closes S^* , and the static programming is complete to allow for the multiplicand correction. After toggle III has been reset and the multiplicand correction is made at n.2, Cl_u opens gate C_9 which stops the shift counter and resets D_1 . $\bar{P}_{dn}$ then opens gate H_5 , and toggles I and II are reset. Toggle IV is reset by the start signal when another operation begins.

III.4.7. Analysis of the Arithmetic Orders

The logical analysis of the orders for the computer is contained in Tables III.1, III.2, and III.3. Table III.1 lists ten of the orders, and the relevant components associated with the programming of the orders have their respective conditions tabulated. Table III.2 treats multiplication, and Table III.3 treats division. It is assumed for each of the orders that all of the operands are in their proper location before the operation that is programmed starts.

TABLE III.1

Order		G_{in}	G_{lt}	G_{rt}	G_{cl}	G_{dn}	Comp.	A_P^u	$A_{A^u}^L$
C + N	n.1	0	1	1	0	0	C'	0	1
	n.2	0	1	1	0	0	C'	1	0
C - N	n.1	0	1	1	0	0	C	0	1
	n.2	0	1	1	0	0	C	1	0
C + M	n.1	0	1	1	0	0	2*	0	1
	n.2	0	1	1	0	0	2*	1	0
C - M	n.1	0	1	1	0	0	3*	0	1
	n.2	0	1	1	0	0	3*	1	0
H + N	n.1	0	1	1	1	0	C'	0	1
	n.2	0	1	1	1	0	C'	1	0
H - N	n.1	0	1	1	1	0	C	0	1
	n.2	0	1	1	1	0	C	1	0
H + M	n.1	0	1	1	1	0	2*	0	1
	n.2	0	1	1	1	0	2*	1	0
H - M	n.1	0	1	1	1	0	3*	0	1
	n.2	0	1	1	1	0	3*	1	0
S_{rt}	n.1	1	1	0	1	1	-	1	1
	n.2	1	1	0	1	1	-	1	0
S_{lt}	n.1	1	0	1	1	1	-	1	1
	n.2	1	0	1	1	1	-	1	0

Code for Table III.1

0 means open

1 means closed

C means complement

C' means direct (not complement)

2* 3* ... etc = refer to notes.

2* if $S^0 = 0$, comp. gates are set for direct transferif $S^0 = 1$, comp. gates are set for complementing3* if $S^0 = 0$, comp. gates are set for complementingif $S^0 = 1$, comp. gates are set for direct transfer

Table III.2

STATIC PROGRAMMER						MULTIPLICATION CORRECTIONS										ARITHMETIC ORGAN						
	C_1G	G_{rt}	G_{dn}	G_{up}	G_{in}	α	B	γ	a	b	$\overline{Gd}$	I	II	III	IV	<div> $\begin{matrix} P \\ \uparrow \\ S \end{matrix}$ </div> 1-39	<div> $\begin{matrix} A^0 \\ \uparrow \\ S^0 \end{matrix}$ </div> S^0	<div> $\begin{matrix} A_0 \\ \downarrow \\ A^0 \end{matrix}$ </div> A^0	<div> $\begin{matrix} C_0 \\ \uparrow \\ S^0 \end{matrix}$ </div> S^0	Q^{38}	Q_{39}	K
n.1	C'	0	1	2*	2*	-	-	+	-	+	+	0	0	0	0	0	3*	3*	1	+	S^t	+
n.2	C'	0	1	2*	2*	-	-	+	-	+	+	0	0	0	0	0	3*	3*	1	S^t	+	n
The above procedure is same for $K_0 - K_{37}$.																						
38.1	C'	0	1	2*	2*	-	-	+	-	+	+	0	0	0	0	0	3*	3*	0	+	S^t	+
38.2	C'	0	1	+	+	+	-	+	-	+	+	+	0	4*	0	4*	3*	3*	0	S_t	+	38
39.1	C'	0	1	1	0	+	-	-	-	+	+	1	0	5*	0	5*	3*	3*	0	+	S_t	+
39.2	+	0	1	+	+	+	+	+	-	+	+	1	+	6*	0	6*	+	+	+	S_t	+	39
40.1	C	+	+	2*	2*	+	+	+	+	-	+	1	1	1	+	0	1	0	1	+	S^t	+
40.2	+	1	0	2*	2*	+	+	+	+	-	-	1	1	+	1	+	1	0	1	S^t	+	40
4.1	C'	1	0	2*	2*	+	+	+	+	-	-	1	1	0	1	1	1	0	1	+	S^t	+
4.2	C'	1	0	2*	2*	+	+	+	+	-	-	1	1	0	1	1	1	0	1	S^t	+	41

Code For Table III.2

0 means open

1 means close

2*, 3* etc. - refer to notes

2* = If $Q_{39} = 0$, G_{up} is programmedIf $Q_{39} = 1$, G_{in} is programmed3* = If $Q_{39} = 0$, gate A^S is open permitting a sign digit transfer, and gate V^* is closed to prevent A_0 transfer up into A^0 .If $Q_{39} = 1$, gate A^S is closed and gate V^* is closed.4* = If $Q^{38} = 0$ then + ; if $Q^{38} = 1$, then no change.

5* = Static state of 4*

6* = If not changed at 4* then +.

For toggles I, II, III and IV, 0 and 1 mean the state of the toggle.

 S^t - Static state

+ - Changing state

C - Complement

 C' - Direct transfer

TABLE III.3

K ₃₉	T ₃	G _{lt}	C.G	Q=1	G _{in}	G _{up}	P to A ⁰	A _L to A ^u	A ^u to A _L	
---/	1.1	1*	0	2*	3*	4*	4*	5*	5*	1
1	1.2	1*	0	2*	3*	4*	4*	1	1	0
---/	n.1	--	0	6*	3*	4*	4*	5*	5*	1
n	n.2	--	0	6*	3*	4*	4*	1	1	0

Code for Table III.3

0 means open

1 means closed

1*, 2*, 3* ... n* = refer to notes

---/ - means changing state

1* - opposite state of A^0 transferred to T_3 for the initial comparison of A^0 and S^0 .

2*.1 - S^0 and A^0 agree -- C.G., comp. (pos.)

2*.2 - S^0 and A^0 disagree -- C.G., direct (neg.)

3*.1 - S^0 and P_0 agree -- $Q=1$, open (pos.)

3*.2 - S^0 and P_0 disagree -- $Q=1$, closed (neg.)

4*.1 - 2*.1 + 3*.1 - G_{in} , open (neg.); G_{up} , closed (pos.)

4*.2 - 2*.1 + 3*.2 - G_{in} , closed (pos.); G_{up} , open (neg.)

4*.3 - 2*.2 + 3*.1 - G_{in} , closed (pos.); G_{up} , open (neg.)

4*.4 - 2*.2 + 3*.2 - G_{in} , open (neg.); G_{up} , closed (pos.)

5* - depends on 4*, G_{in} transfers data from P to A^0 ; G_{up} transfers data from A_L to A^u .

6* - after C.G. is determined at K_1 by the comparison of S^0 and A^0 , C.G. remains in that condition throughout the division operation.

During the programming of the orders listed in Tables III.1 and III.3, there are several voltage inputs to various gates of the static programmer that remain constant. These voltage inputs are active only during the multiplication process and are derived from the multiplication corrections section of Figure III.1. They are as follows: β (No. 4 input of gate H); γ (No. 5 input of gate N and No. 3 of gate J); "b" (No. 2 of gate X); "a" (No. 3 of gate U); and $\overline{Gd}$ (No. 2 of gate W). Furthermore, the following gates of the arithmetic organ will maintain the following condition during the programming of the orders in Table III.1: Gate T^* between S^0 and C_0 will be open; gate S^* between S^u and C.G. will be open; gate A^s between S^0 and A^0 will be open; gate A^s between S^0 and A^0 will be closed; gate V^* between A^0 and A_0 will be open; and gate U^* between A^u and A_L will be closed.

Taking the first order of Table III.1, the following analysis may be made: Clear and add a number from S^u into A_L is the order set in the function table. The gates of the static programmer are then set to produce output voltages on the "G" Lines. If the voltage sign (+ or -) on a particular line agrees with the arrow direction shown on that line, then that output is considered active. After the gates of the static programmer are set, the dynamic programmer starts. 1.1 is the first dynamic pulse, it causes data from S^u to pass from P into A^u . 2.2 is the second dynamic pulse, and it causes the data that was placed in A^u by 1.1 to be shifted down into A_L . Similarly, each of the other orders may be followed in the above manner.

IV. DESCRIPTION OF AN EXPERIMENT ON WILLIAMS MEMORY TUBE

IV.1. Introduction. Since the successful operation of electrostatic storage on the cathode-ray tube is dependent on the screen material having a secondary emission ratio greater than unity in the region of operation, it is essential that this material deposit be homogeneous and contain no particles of foreign material, or at least no foreign material which has dissimilar emission characteristics.

The purpose of this section is to discuss the effects of these impure spots upon storage in their immediate vicinity, as well as a practical method of determining the spots location and their quantitative detrimental effect. No attempt will be made to explain the exact nature of an impurity spot, since this is not known; and it suffices for present purposes to state that in the primary electron energy region where the normal screen surface has a secondary emission ratio of greater than unity, an impurity spot is one where the ratio is less than unity. (Figure IV.1 shows the results of some preliminary investigation into impurity types.)

FIGURE IV. 1
SECONDARY EMISSION RATIO
OF GLASS & PHOSPHOR

FIGURE IV. 2
POTENTIAL DISTRIBUTION
THROUGH IMPURITY

AVERAGE IMPURITY PULSE
FIGURE IV. 3

DOUBLE DOT FOR
TESTING IMPURITY
FIGURE IV. 4

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IV.2 Effect of Impurity Spots. Basically, in the region where the emission ratio is greater than unity, the beam, as it moves across the screen, leaves a positive charge in its wake because of more secondary electrons escaping from the screen than primary electrons arriving. Some of these secondary electrons, however, that have low energies and velocity components opposite to that of the lateral direction of the beam will fall behind the beam, tending to neutralize the positive charge which had previously been left. Since the energy of the majority of the secondary electrons is quite low, the lateral distance which they will travel before returning to the screen is small, being on the order of two millimeters or less. It is logical to assume, then, that the extent to which a given remanent positive charge will be neutralized by the secondary electrons coming from the source moving away from the remanent charge will be proportional to the speed of the source. In the present case this means proportionality to the lateral velocity of the electron beam. Thus, if the beam is moving slowly enough and if no interference to the escape of these secondary electrons of low energy exists after the beam has been turned on, there should be no great net change of charge on the surface of the tube. However, if a point exists on the screen which has an emission ratio of less than unity, it will accumulate electrons and in time will acquire a sizeable negative potential. As the beam crosses this point, the secondaries which normally would fall behind, neutralizing the positive charge it has left in its wake, may be prevented from doing so by this potential barrier which now exists between the beam and the positive charge. Thus, immediately preceding each impurity, there may exist a less neutralized region (Figure IV.2). If the beam is moved swiftly enough and returns to this point before this positive charge has leaked, a negative pulse will occur at the pickup plate owing to the anticipation pulse effect discussed by Williams.¹ As the beam now passes over this impurity and reaches the surface which again possesses a greater than unity emission ratio, it will establish a positive potential at that point, and a positive pulse will be seen at the output.

¹The anticipation pulse may be explained briefly as follows: As the beam moves along an equipotential region of greater than unity emission ratio, the time integral of secondaries leaving the screen, primaries arriving, and low-velocity secondaries falling back on the screen, is zero. Thus, no change in screen charge occurs, and no output pulse is seen. If the beam now approaches a region of residual positive charge, some of the secondaries having velocity components along the beam path will be accelerated toward this positive charge, the time integral will momentarily have a negative value, and a negative pulse will be seen at the output. This pulse, which anticipates a positive charge ahead of the beam, is called an anticipation pulse.

The wave form of the impurity pulse is shown in Figure IV.3 and corresponds with the potential distribution along the beam path (Figure IV.2) as shown. The negative pulse (1,2) is the resultant of:

- (a) a negative pulse formed by bringing the beam into a region 1 (Figure IV.2), where a previous equilibrium had been established (anticipation pulse),
- (b) a negative pulse formed by moving the beam into a region 2 having less than unity emission ratio, and
- (c) a positive pulse if the region 1 was partially neutralized by the beam moving away from it.

It should be noted at this point that the negative anticipation pulse of region 1, described in (a) above, may or may not exist, depending upon whether or not the positive charge ahead of the impurity exists. The magnitude of this charge is equal to $Q_1 - \sum_{t_1}^{t_2} e(t)$, where Q_1 is the original positive charge, t_1 is the time when the charge was established, t_2 is the time when the beam next returns to the spot, and e is the absolute magnitude of the charge on those electrons which fall on the spot in the time interval $t_2 - t_1$, assuming that these electrons have insufficient energy to remove a secondary. Thus, depending upon $\sum_{t_1}^{t_2} e(t)$, the charge the beam sees after returning to the point immediately ahead of the impurity will vary from Q_1 to zero or less, and the anticipation pulse may or may not exist. The negative pulse due to region 2 will exist in any case.

The positive pulse (region 3) is due to the beam establishing a new trail of charge as it passes into a good region beyond the impurity.

The peak to peak amplitude of the impurity pulse, then, is a function of the negative potential established at 2, and may be used to approximate the extent to which the impurity will retard the storage of information at that particular point.

The manner in which an impurity affects the storage of information may be shown by the following experiment:

If the beam is moved repeatedly between A and B (Figure IV.4), which represents two spots on the cathode-ray screen approximately 1.4 spot diameters apart (the beam remains on each spot approximately 3 microseconds and then is turned off while moving from one spot to the other), two positive pulses will be observed at the output of the video amplifier. This indicates that secondaries from spot A at least partially neutralize the positive equilibrium left at B and vice versa. These positive pulses correspond to dashes in the practical memory system. If now B be located

over an impurity, the positive pulse due to B will decrease and, in the case of a bad impurity, will go in a negative direction owing to the instantaneous increase in negative potential there. This negative charge existing at B will cause the beam to diverge in the manner shown in Figure IV.5. The combined effect of reduction of primary impact energy and angle of impact will cause those primary electrons falling on the positive equilibrium on A to neutralize it, rather than to emit secondaries from it. This neutralization will be more complete, i.e., the spot A will be brought closer to zero potential than it normally would have been owing to the secondary refill process, and a larger than normal positive pulse will result when A is examined.

IV.3. Mapping of Impurity Spots

To perform the initial mapping or location of the impurity spots upon the cathode-ray tubes, the beam was caused to scan the entire surface of the tube following the equations $x = \sin \omega t$ and $Y = \sin \omega' t$, where ω equals $2\pi \times 200 \frac{C}{S}$ and $\omega' = 2\pi(200 \pm .125) \frac{C}{S}$. A second cathode-ray tube or slave tube had its deflection plates connected in parallel with those of the tube under test (master tube), and its Z axis was caused to be turned on only upon receipt of the previously described negative impurity pulse from the amplifier associated with the master tube. Thus it is seen that a pattern of dots will appear on the slave tube exactly corresponding to the position of the impurities on the master tube. A reticle was placed over the slave tube, and photographs were taken of this tube with full lens opening (F7.7) on Kodak Super Pancro Press type B film for 120 seconds. Beam current density was adjusted to 10 microamperes, and accelerating potential to 2KV. Two sample photographs, one showing a tube containing many impurities and one showing a tube relatively free from impurities, are enclosed in the report. It will be noticed on the photograph of the tube containing a large number of impurities, that some spots seem to have two crossed lines passing through the center of the impurity. This condition indicates a particularly bad spot, and one explanation of the crossed lines is as follows. If the impurity acquires a charge sufficient to deflect the beam around its periphery rather than allowing it to pass through its center, the regions about a line normal to the beam path and passing through the center of the impurity will be scanned by a trace which is moving somewhat more swiftly than the trace preceding and following the impurity. Since the time required to establish a positive charge in a good region is less than the time taken to refill or neutralize it, it is conceivable that a positive potential exists for a short distance along the lines normal to the beam path through the impurity (Figure IV.6). If this condition does exist, whenever the beam, in its later excursions, passes through a point on this positive distribution, a negative anticipation pulse will be seen, turning on the beam of the slave tube. The locus of all of these slave tube turn-ons will then be the lines shown in Figure IV.7.

RELATIVE AMP
+
| 0
|

FIGURE IV. 5
BEAM DISPERSION CAUSED BY IMPURITY

Photographic map of a cathode-ray tube unusable as an electrostatic storage tube. The heavy crossed white lines as well as the intense white dots indicate impurities of area large enough to prevent storage at those points.
(See text, IV.2 and IV.3)

Photographic map of a cathode-ray tube suitable for use as an electrostatic storage tube. The area of the impurities indicated by the faint white dots was found to be insufficient to hinder storage at those points.

FIGURE IV. 6
POSITIVE CHARGE ESTABLISHED AROUND LARGE IMPURITY BY
DISPERSION OF SCANNING BEAM.

FIGURE IV. 7
LOCUS OF SLAVE TUBE. TURNONS AROUND LARGE IMPURITY

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Because of the difficulty in comparing the relative intensity of the spots appearing on the photographs, the photographs may be used only as an indication as to position of the impurity and not as a method of quantitatively determining the spots' effect upon storage at that point.

IV.4. Quantitative Determination of the Effect of Spots upon Storage

Since now a map of the position of the impurity spot has been obtained, it is necessary only to position the beam at this spot and attempt to write a dash there in order to determine the spot's effect upon storage. This was accomplished in the following manner. A horizontal line is placed upon the tube and manually is moved vertically in the vicinity of a known impurity spot. When the line passes through an impurity, a signal will appear as described in section IV.2. By vertically positioning the line until the amplitude of the signal is at a maximum, the spot is known to be located somewhere along the line. Two dots similar to the dots A and B described in section IV.2 are then moved horizontally along the ordinate thus established until a reduction in one of the positive pulses is noted. The ratio of the amplitude of this reduced pulse to the amplitude of a good pulse in comparison with a previously determined minimum ratio gives a precise indication as to the suitability of this particular spot for storage. Since the present memory system employs an accelerating potential of 1200 volts, the quantitative determinations were made at this voltage, and the steady-state beam current was adjusted to 2.2 microamperes.

IV.5. Equipment

The scanning described in section IV.3 was obtained in the following manner: A 200-cycle-per-second sine wave from a Hewlett Packard Oscillator was split into three sine components of equal amplitudes and separated in phase by 120° . This three-phase system was then applied to the stator of a Bendix Autosyn, giving a rotating magnetic field of angular velocity $\omega = 2\pi \times 200$ radians per second. If the rotor of the Autosyn is turned externally at a constant angular velocity, the signal appearing on the rotor will be of frequency $F = 200 \pm$ the frequency of rotation of the rotor in cycles per second. In practice the rotor was turned at 0.125 cycles. This signal suitably amplified was applied to the Y deflection plates of the tube under test and the slave tube, while the original 200 cycles per second from the Hewlett Packard was applied to the X deflection plates (Figure IV.8.)

The resultant of these two signals forms a constantly degenerating ellipse, the over-all pattern appearing as a square, the diagonal of which is proportional to the peak amplitude of the sine waves.

The amplifier used to detect the signals appearing at the pickup plate had a band pass of 1.5 mc and a gain of 1.9×10^4 . Diagrams of the apparatus used appear in Figure IV.9.

FOR $\alpha = \beta = \gamma = 60^\circ$

$db = be = ed$

THEN $ab = \frac{ac}{2}$ OR $X_C = R_1$

AND $ad = \frac{ac}{2} (1 - \tan \frac{\theta}{2}) = ec$

OR $R_2 = R_4 = \frac{R_2 + R_3 + R_4}{2} (1 - \tan 30^\circ)$

NO.	PWG-103-X
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FIGURE IV.9
APPARATUS FOR MAPPING IMPURITIES

NO. PHG-103-W
DEPTS D-6
AUTHOR CNU
DATE 6-5-51
D.C.V.

IV.6. Experimental Results and Conclusions

Although the number of tubes tested to date is insufficient to formulate a statistical analysis of rejection probability, it does give sufficient information regarding the nature of impurity pulses encountered and their bearing on usability of the tube.

In the case of the normal negative to positive impurity pulse (Figure IV.3), the dash reduction ratio is a function of the peak to peak amplitude of the pulse (Figure IV.10). However, the intercepts of this curve were found to vary from tube to tube so that, except for the case of extremely large impurity pulses, this measurement alone cannot be relied on as a standard of tube performance, and the dash reduction ratio test must be performed.

Some unique pulses of the form, Figure IV.11, were encountered, and upon inspection of the tube were found to occur at points where an area of glass as large or larger than the spot area was not covered by phosphor. One explanation of this phenomenon is as follows. As the beam travels in a straight line across the face of the tube, it is continually establishing a positive equilibrium and reducing, by means of its trailing secondaries, the equilibrium which it left immediately in its wake. If now a spot of uncovered glass be placed in its path, it will acquire a negative potential sufficient to reduce its operating point to A, Figure IV.1. If the area of this spot be large, the number of electrons collected will form a point charge sufficient to disperse the beam somewhat, at the same time reducing its energy, the next time the beam passes through the impurity. When this occurs, some of the dispersed primaries will fall into the remnant positive charge normally left immediately ahead of the impurity. More electrons of reduced energy from the primary beam, under these conditions, will fall on the positive charge than would secondaries in the normal trail of charge, and the charge will be brought closer to zero potential than any other partially neutralized spot along the beam path. The next time the beam crossed this more thoroughly neutralized spot, a greater change in screen charge would be required to recharge it to equilibrium than would be required at any other spot along the line, and a positive pulse would result. The remaining negative and positive positions of the pulse (Figure IV.11) are obvious in light of the discussion in section IV.2. It follows that any large impurity would have the same effect, but a tentative investigation has shown that impurities consisting of particles of foreign material are generally much smaller in size than those consisting of absence of phosphor.

Curves of impurity pulse size versus accelerating potential indicate at least two types of impurities present (Figure IV.12). Curve A decreases rapidly with a decrease in accelerating potential and probably intersects the X axis around 800 volts, while curve B has a relatively small slope and probably extends to the origin. A undoubtedly represents an impurity

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AUTHOR CHU
DATE 6-5-51
REV.

FIGURE IV.10
DASH REDUCTION RATIO VS LINE SCAN IMPURITY PULSE

Figure IV.11
Unique Impurity Pulse

of the uncovered glass - or absence of phosphor - type, since glass has a unity emission ratio in the region of 900 volts. B is probably due to small particles of carbon imbedded in the phosphor, since carbon does not have an emission ratio greater than or equal to one in any primary energy region used. Upon dissecting a tube, the B particles can be seen with the naked eye, but it is not definitely ascertained that they are carbon. The A regions may be seen by cross-lighting the tube and looking at the screen through the uncovered regions between the end of the aquadag and the screen.

Testing of 57 tubes yielded 28 tubes usable for storage on the basis of a minimum dash reduction ratio of 0.75. Of the tubes rejected, 80% of the tubes had only one rejectable impurity, 10% had two impurities, and 10% had three rejectable impurities.

REFERENCES

1. Williams, F.C. and T. Kilbourn: "A Storage System for Use with Binary-Digital Computing Machines." Proceedings of the Institution of Electrical Engineers (London), Vol. 96, Part III, pp. 81-100 (March, 1949).

V. THE INTERNAL MEMORY CONTROL

V.1. Memory and Order Sequence Control. The function of this Control is to integrate the Arithmetic Control with the Memory. Specifically it sets the Memory to the appropriate position for read and write orders, cyclically goes through the Control orders, readjusts the Control position on Conditional and Unconditional Transfer orders, and permits Memory regeneration at other times.

This Control synchronizes the asynchronous Arithmetic Control with the synchronous Memory whenever they must interact.

The accompanying sketch (Figure V.1) is submitted as a preliminary design.

V.2. The Control Counter. Counters are an essential part of all digital computers. In the parallel type of computers some orders, such as multiplication and division, imply a certain number of shifts. The number of these shifts is recorded in a counter. When the prescribed number is reached, the operation is ended, and a signal is sent to the control so that the machine can continue to the next operation. The time required to record the count is added to the shifting time so that the speed of these operations is a function of the counter speed. Another application is in the Williams Memory System. This is an electrostatic storage system which requires regeneration of the stored charges at regular intervals. It is convenient, circuitwise, to do the reading or writing operations at the same rate as regeneration is done. Only one of these operations occurs at a time.

A shorter regeneration interval means greater reliability and shorter access time. Here again counters become important components in determining the speed of this system. Counters are a part of the device used to step the beam of the cathode-ray storage tube successively from point to point in regeneration or to a specific point in reading or writing. These operations, regeneration and action, are controlled by separate counters with a common set of toggles. This arrangement will be explained in detail later. Here we can point out that the speed with which the cathode-ray beam is stepped from point to point is a function of the counter speed. Therefore, the intervals at which regeneration of action takes place are shortened if a high-speed counter is used.

In general there are two ways in which the counters could be designed. One of these would use the conventional scaler, in which the condition of any toggle is dependent on the transition of the preceding toggle from one state to the other. In some cases this would require waiting until all the toggles changed state successively. Thus the maximum carry time would be the time of operation of a single toggle times the number of stages.

The other counter design utilizes the adding principle, in which "1" is added successively to the count existing in the counter. This scheme also implies a "carry" thru a chain of stages and the necessity of waiting until the carry is propagated thru the chain of stages. However, in this type of counter a chain of cathode followers can be used to propagate the carry. Since cathode followers have a low output impedance, the circuit response can be extremely fast: in a typical design, the maximum carry time per stage was about 0.05 microsecond. The time required to change the state of the toggles was about 0.5 microsecond.

MEMORY AND ORDER SEQUENCE CONTROL
LOGICAL DIAGRAM

FIG. V.1

NO. *PHG-103-E*
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This design, then, consists of a set of toggles (T_2 in Figure V.2) in which the result of the preceding count is held. Output connections are made from these toggles. A chain of gates (the carry line) examines each of these toggles and changes the state of the counting toggles (T_1 in Figure V.2) if required. This change of state occurs at the time of pulse P_2 . Then upon the command of pulse P_1 , the information is transferred to the T_2 toggles. The information is available at the T_2 toggles without a wait for possible carries to take place. The only waiting time is the time required to transfer toggles T_2 from one state to another.

In detail, the circuit operates as follows: Associated with each set of toggles T_1 and T_2 in Figure V.2 there is a set of transfer gates G_1 and G_2 . They are negative "and" gates. Initially, 2^0T_1 toggle is cleared to unity and all the other toggles are cleared to zero. The presence of a negative pulse on the P_1 line will energize all the direct transfer gates G_2 which will transfer all the contents of T_1 to T_2 . Thus toggle 2^0T_2 will register a unit. The presence of P_2 will always open the reverse transfer gates 2^0G_1 . Whether 2^nG_1 will open or not is dependent on the following: $2^{n-1}T_2$ must contain a unit, and $2^{n-1}G_0$ must be energized. Closer observation of the arrangement of G_0 gates will reveal that they are a full decoding function table of all the previous $2^{n-1}T_2$ stages. Since the functional purpose of the toggles 2^KT_2 is to store the contents of toggles 2^KT_1 and do the gating, they are named the storage toggles. The true count is carried out during the presence of P_2 . Therefore the toggles 2^KT_2 are the counting toggles.

Since the counter outputs are taken from the storage toggles, it is seen that counting is accomplished as soon as the P_1 line is energized.

The principle of this counter can be extended to the design of a dual counter. Such a counter is useful in controlling the deflection circuits in the Williams Memory System, where the beam position must obey the commands of either the regeneration counter or the control counter. The control counter counts the sequence of orders. In the dual counter, shown in Figure V.3, T_1 and T_1^1 are the two sets of counting toggles, and T_2 is the common set of storage toggles. Output connections are taken from T_2 . The contents of either T_1 (or T_1^1) can be transferred to T_2 after T_2 is cleared of all information. Then the information is transferred back to T_1 (or T_1^1) with the addition of a "1." Then T_2 can be cleared ready for the information from T_1^1 (or T_1 again).

Information can be transferred into T_2 without clearing by using a double gate, which results in a slight increase in speed. Double gates are indicated in Figure V.3 in both sets of transfer gates, that is, in the transfer gates from T_1 (or T_1^1) to T_2 and from T_2 to T_1 (or T_1^1).

ZERO CARRY TIME BINARY COUNTER

BLOCK DIAGRAM

FIG. V.2

NO. *PHG-103-D*
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DUAL COUNTER
FIG. V. 3

NO. PNG-103-C
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ALL TUBES 6J6 OR 5670

MEMORY COUNTER

FIG. I. 4

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MEMORY COUNTER
FIG. I.5

PHG-103-F3
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An experimental model of this counter has been built, and the resolving time is about $1/2$ microsecond. A dual counter using an asymmetrical toggle has been designed. It requires 7 tubes per stage. A model will be built, and the results reported in the next quarterly report.

VI. MAGNETIC TAPE AS THE AUXILIARY MEMORY

VI.1. Introduction. Considerable investigation has demonstrated that a parallel high-speed tape memory system is feasible. An experimental driving unit has been constructed that will move 100 feet of tape 50 inches per second in a reliable manner. Progress on head design has reached the stage where it is evident that 40 parallel channels can be accommodated without difficulty.

A description of the proposed memory system may be conveniently separated into three distinct parts, namely, the mechanical drive, the recording heads and associated equipment, and the control.

In what follows, certain basic design features are to be assumed. These are:

- (1) The tape speed is 50 inches per second.
- (2) There are 42 simultaneous channels of which 40 are for information and two for synchronization.
- (3) The tape width is 5 inches.
- (4) The digit density is 100 per inch per channel.
- (5) The digit rate is 5000 per second per channel.
- (6) The tape length is 200 feet of 0.002 inch thick tape or 100 feet of 0.004 inch thick tape.

The design of a tape unit suitable for actual computing use has been initiated. The basic features of this unit are the same as those of the experimental drive with the exception of tape width and length. The width on this model will be under 3 inches, and the driving mechanism will be powerful enough to handle 1200 feet of 0.006 inch thick tape.

The memory capacity inherent in 1200 feet of tape is of the order of 10^6 words.

VI.2. The Mechanical Drive. The starting-stopping characteristics of a high-speed tape drive should be as rapid as possible. For this reason, initial accelerations are applied to a low-inertia capstan and a very short section of tape on either side (Figure VI.1). The windup reels containing most of the tape are driven by much slower acting servomechanisms. The servomechanisms are powerful enough so that both reels will follow the capstan to within a few inches. They derive their control signals from the position of two dancing rollers.

Distortionless travel of a wide tape cannot be achieved unless a high degree of precision is maintained in the relative orientation of the rolling members. Four important conditions must be satisfied; namely, (1) the surface of the rolling members must be cylindrical, (2) the flanges on the rolling elements must lie in two parallel planes, (3) the axes of the rolling elements must be at right angles to the planes of the flanges, and (4) the tape must be straight and of a width equal to the distance between the flanges.

The construction of a truly cylindrical surface involves precision grinding operations. For this reason and because of the high strength/weight ratio, hardened steel was used in constructing the rolling elements. No recording difficulties attributable to the magnetic properties of steel windup reels, dancing rollers, etc., have been encountered. Figure VI.2 shows the construction of a typical rolling element exclusive of dancing rollers. The units were hardened after rough machining. The surfaces deviate from true cylindrical form by no more than 0.0001 inch.

The alignment of axes and flanges is controlled by two large flat support plates. These plates are 1/2 inch thick and made of cold rolled steel. These plates should be annealed and aged, although this was not done on the present drive. The tape and accompanying rollers are located between the plates, whereas the servomechanisms for driving the windup reels and the capstan driving unit are situated externally. The plates are supported one-to-another by means of eight heavy crosspieces at the four corners. Bearing holes and other guiding surfaces common to both support plates were machined while the plates were firmly clamped together. The flanges in the system are maintained at a constant distance from the support plates by means of spacing collars (Figure VI.2).

The axes of the rolling parts are at right angles to the support plate surfaces to within 0.0001 inch per inch. The flanges lie within 0.001 inch of parallel planes.

Dancing-roller construction is illustrated in Figure VI.3. These units lack flanges, and control of the orientation is limited. The dancing-roller end bearings travel in 6" long vertical slots, and the end play of the rollers is limited to about 1/8 inch. The slots are located in both support

FIGURE VI.1
TAPE DRIVING UNIT.

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FIGURE VII.2
ROLLING MEMBERS

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plates and are 0.001 inch wider than the end bearing diameter. No further restrictions on dancing-roller orientation (except those imposed by the tape) exist.

In order that ample guiding length on the tape edge be available, the flanges are everywhere $1/2$ inch deep. The inside corners of the flanges are rounded to prevent tearing. The flange depth allows the placement of nearly 200 feet of tape (0.0022 inch thick) on a windup reel without loss of guidance.

The dancing rollers are the points at which tension is introduced into the tape. This tension should be great enough to keep the tape from slipping on the capstan during acceleration. The tension should, however, be the minimum required, so that the flanges in the system may align the tape without bending, stretching, or tearing. Evidently, it is desirable to control the tension so that large forces are present during acceleration, and minimum amounts are present under steady-state running conditions. Application of such a force to the dancing rollers directly is difficult since they must be highly mobile devices.

The servomechanisms are separated into a main drive and differential drive servo. The tension force is applied to the dancing rollers through a differential roller and cables as illustrated in Figure VI.1. The tension and length of the connecting cables must be as nearly alike as possible. A turnbuckle is provided for equalizing cable lengths. Equality of cable tension is assured by introducing the force at the exact center of the differential roller. The main drive servo rotates both windup reels in the same direction at high speed and is controlled by the position of one dancing roller. The differential servo rotates the reels in opposite directions at a low relative speed and is controlled by the position of the differential roller. Since the ratio of winding depth to mean radius of the reels is kept as low as practical, the differential servo is essentially a low-speed, high-torque device, while the main drive servo is of the opposite nature. Assuming equal servomechanism power capabilities, the advantages to be gained from this system as compared to straightforward and distinct servo-mechanisms on each reel are threefold.

In the first place, since the differential servo is a relatively high-torque device, the position of the differential roller can be held quite closely to a nominal value. Furthermore, this roller may be loaded down with much more mass than is permissible on the dancing rollers, since the capstan will not see this mass during acceleration. Application of a controllable force to a roller of these characteristics is relatively easy.

Secondly, the inertial load on the main drive servo will be nearly independent of the tape position. Any change in the load of tape on one reel is compensated for by a nearly equal and opposite change in load on the

other reel; as a result, the servo is reliable and stable. The inertial load presented to the differential drive servo depends on tape position but, because of the large gearing ratios used in this servo, the tape load is an insignificant part of the whole. This servo, too, is reliable and stable.

In the third place, a high degree of efficiency is possible, particularly where the tape tension is large. The energy that one reel receives from an aiding tape tension is transferred mechanically to the other reel where it is used in overcoming an opposing tape tension. The saving in energy enables the main drive servo to utilize nearly all of its inherent power in starting and stopping the reels.

Both servomechanisms are constructed around 50-watt (1/15 hp) two-phase induction motors. The damping signals are taken from small induction generators directly coupled to the motor shafts. Differential transformers are used to generate the error signals.

The servo-amplifiers (Figure VI.4) are direct coupled from inputs to power amplifier grids. Direct coupling was used to avoid grid blocking following strong signals. The first stage functions as separate phase shifters for the error and damping signals. The signals are mixed and amplified, and balanced output is obtained in the second stage. The third and fourth stages are a balanced amplifier and driver, respectively. A slow-acting inverse feed-back circuit is employed in the third and fourth stages in order to make the average bias on the p.a. grids independent of drift.

The output stage is a pair of 807's running Class AB₂ and capable of 120 watts output to each motor. The output transformers are commercial power transformers chosen to provide the correct impedance match for maximum stall torque. The plate circuit is tuned to 60 c.p.s. for maximum plate efficiency.

The motor impedance rises sharply with increasing motor speed. It is therefore possible for excessive p.a. screen current to flow with large input signals. The screen dissipation is held to a safe value by clamping diodes and series dropping resistors.

Because two-phase induction motors tend to run at full speed with only one phase excited, provision has been made for removing all motor power in case of a lack of final plate supply voltage. In addition, the power is automatically removed in case the differential roller strays too far from its nominal position. Both cutout arrangements have helped immensely in avoiding tape snarls under abnormal circumstances.

Figure VI.5 shows the gearing system used between the servo motors and windup reels. The entire gear system is mounted on the outside of one of the support plates. The electronic apparatus associated with the

FIGURE VII.5
GEAR SYSTEM

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servomechanisms is in a separate standard relay rack and connects to the drive by means of electrical cables.

For the present, the capstan is driven in a very elementary fashion by means of a small reversible motor. Direction and speed are governed by a simple controlling unit on the relay rack. The reversing time of the motor is about one second. To avoid running past the end of the tape, automatic reversal has been provided. That is, a felt-lined wiper senses the amount of tape on one windup reel and causes the capstan motor to reverse if the tape height exceeds certain limits.

A fast-acting capstan drive unit is nearing completion. It is anticipated that this unit will be able to start or stop the capstan in less than 3 milliseconds. The corresponding tape movement is less than 1/10 inch per start or stop. The description of the unit will be postponed until satisfactory operation has been attained.

The force applied to the differential roller is presently being generated by a long spring of adjustable tension. No attempt to construct a force-controller unit (to work in conjunction with the capstan drive) will be made until the necessity of a controlled tape tension has been demonstrated.

A discussion of the mechanical characteristics of magnetic tape has so far been omitted. Currently, a state of indecision exists regarding the choice of a suitable tape. Tests now being performed will eventually settle the matter.

It has been pointed out that important features of the tape (insofar as proper mechanical action is concerned) are straightness of the edge and precision of the width. The wide plastic tapes thus far obtained seem to be straight enough to run true, provided the manufacturer understands the requirement. Small curvatures are present, but the tension used in the drive is sufficient to straighten the tape out. Typical tensions are of the order of one pound per inch of tape width. After several passes through the drive, the tape seems to be permanently straightened out. No metal tapes have been tried, and, thus far, paper tape has proven itself valueless for quite a different reason. The phenomenon of setting has also been observed operating in a disadvantageous fashion, i.e., permanent curvatures have been introduced into tapes that were improperly wound on storage reels.

The precision of tape width is of far more importance than curvature. There are three independent causes of tape width variation, namely, temperature changes, relative humidity changes, and the strains of tension. Clearly, a desirable tape should possess low temperature and humidity coefficients of expansion and a high modulus of elasticity. It is also evident that, given a tape of a certain character, the possible humidity and temperature variations should be minimized, and the tension used should be a minimum.

The same arguments apply to the manufacturing process. In particular, it would be convenient if the temperature, humidity, and tension present in the slitting process were the same as those present in the drive. However, by trial-and-error, it is possible to circumvent differences, provided the conditions are constant in both the manufacturer's and user's plants. It might be thought that the user could cut the tape to suit himself, but our experience indicates that tape cutting is not easy and is best left in the hands of the manufacturer. Our manufacturers are currently co-operating in an attempt to establish precision widths. Progress to date indicates that precisions of 0.1% or better will be attained. Samples of tape as close as 0.05% to the desired width have been received.

One definite conclusion that can be drawn from observations to date is that the tape will drift until a flange is touched. The drift ultimately takes place no matter how much precision is inherent in the initial passage of the tape through the drive. The drift is small, probably not exceeding 0.001 inch per passage under good conditions, but it is present nevertheless. Therefore, a satisfactory tape must be one which the flanges can guide without harmful effects.

The force per unit length that a flange exerts while guiding a tape may be assumed to be proportional to the tension, curvature of rolling surface, and coefficient of friction between tape and rolling surface. The force per unit length that a tape edge will withstand without undue bending is proportional to the modulus of elasticity and the cube of the tape thickness. The amount of bending that can be tolerated without tearing or permanent stretching is proportional to the elastic strain limit of the material. It is apparent that a desirable tape, in addition to possessing a high modulus of elasticity, should possess a large elastic strain limit (resiliency) and relatively large thickness. As for the coefficient of friction, the requirement that the tape shall not slip on the capstan during acceleration overshadows the advantage of a low friction coefficient for guiding purposes. The exception concerns the windup reels where tape may be stored for considerable periods of time. Here, it is highly desirable to have a tape which will slip easily into place. The pertinent coefficient of friction is that of the tape on itself, and, unfortunately, the values for paper and plastic run rather high.

One other good reason for using a tape of high resiliency is its ability to withstand the shock of rapid accelerations. The shock arises from the inertial load of the dancing rollers. We are contemplating accelerations of a magnitude such that the total instantaneous tension in the tape can reach 50% or so of tensile strength (or yield strength, as the case may be). This applies to the thinnest tapes used. The condition is proportionally less severe for thicker tapes. On a weight-for-weight basis, the plastic tapes are far superior in shock absorbing powers to either paper or metal tapes. Direct tests using forces of short duration have been applied to the plastic

tapes, and the indications are that a 50% shock load is not harmful. It should be pointed out that the load was uniformly distributed, and the edges of the tape contained no tears.

The mass per unit length, or more properly the density, is an important feature of the tape. For the sake of reducing the necessary servomechanism power capability, the tape should be as light as possible. This reason alone has forced abandonment of any attempt to use metal tapes. The specific gravity of plastic or paper tapes (average of base and oxide coating) is around 1.2-1.3.

Thus far, we have preferred the plastic tapes to the paper tapes. However, the plastic tapes possess one extreme disadvantage, i.e., a huge humidity coefficient of expansion. For this reason, investigation of paper tapes is still continuing, although it is already apparent that a satisfactory paper tape will have to be at least twice as thick (and consequently twice as heavy) as the equivalent plastic tape. One is reduced to choosing between large servomechanism power capabilities or a humidity controlling apparatus. The fact that the paper tapes must be substantially thicker than the plastic tapes arises from the great difference in resiliency of the two materials. The paper tapes seem to be incapable of withstanding even a minute bend in the neighborhood of a flange without tearing and subsequent failure. The standard 0.0022 inch thick size passed through the drive once and then tore itself apart at the edges, whereas the same thickness of plastic tape is capable of several repeated travels without harmful effects. It has been established that a plastic tape of at least 0.004 inch thickness is strong enough to be trustworthy under any conditions. We contemplate the use of tape of 0.005 inch thickness (0.0062 including the magnetic coating).

Paper tape of 0.004 to 0.006 inch thickness is being procured for further testing, but the performance is not expected to match that of the 0.004-inch plastic tape.

The humidity problem may be handled by a suitable air-conditioning unit. Control of the humidity should be such that the relative humidity deviates not more than 5% from nominal, and further, the nominal value should be no greater than 60%. Temperature control to within 10°F of nominal is adequate, and the air-conditioning system for the entire computer will do better than this. We plan to isolate the tape drive (drives) and tape storage reels in as small a space as practical and use an over-sized air-conditioning unit for precise humidity control.

VI.3. Recording Processes and Head Design. There are two reliable ways in which binary digital information may be stored on a magnetic tape. One method is to record pulses whose polarity is governed by the presence of a 0 or 1. This method is commonly called "return-to-zero" recording, since regions of zero magnetization lie between the successive magnets

forming the pulses. The other method, called "non-return-to-zero," consists of maintaining a continual state of magnetic saturation on the tape, the polarity of the magnetization distinguishing between 0's and 1's.

Although the return-to-zero type of storage is somewhat more reliable than the other, the convenient erasing feature of the non-return-to-zero system makes it particularly attractive. The act of writing a new non-return-to-zero record automatically removes any old records present. Separate erasure is necessary in the pulse system. In addition, continuous storage requires simpler electronic facilities than does the return-to-zero type of storage.

A characteristic of the non-return-to-zero storage method is that flux lines enter or leave the tape surface at places where a 0 changes to a 1 or where a 1 changes to a 0. Hence, when a record is read out, pulses are present only if a change in the recorded digit occurs. Furthermore, the pulses are simple ones whose polarity may be used to indicate whether the change was 1-to-0 or 0-to-1. The indication is independent of the direction of tape motion, since a tape reversal inverts both the pulse polarity and the assertions 0-to-1 and 1-to-0.

Separating the pulses on a polarity basis is circuit-wise a very simple operation. If the separated pulses are used to trigger the opposite sides of a flip-flop, the flip-flop will at all times serve to indicate the state of magnetization in the tape and hence the digit stored.

To create a record of the non-return-to-zero type, a continuous current capable of saturating the tape is maintained in the head coils, and a second flip-flop used to establish the polarity of the current.

The two flip-flops, called the reading and writing toggles, are the points through which information passes to and from the tape memory system. The passage of this information must be controlled by gates of a synchronous nature. These gates should be actuated by the tape itself if precise interpretation and placement of the magnetic patterns is to be obtained. The tape must contain, therefore, at least one synchronizing channel. For simplicity in the tape control circuits, two such channels are required.

Figure VI.6 is a block diagram of the reading/writing equipment associated with one channel. One stage of the accumulator is shown to indicate the origin and/or destination of stored information. Figure VI.7 illustrates a possible circuit layout meeting the requirements of the block diagram. It will be noticed that provision is made for operating several distinct head assemblies from the same electronic circuits. This allows the use of a multiplicity of tape units without the need for a proportionate amount of equipment. It is evident that by applying the proper voltages to

FIGURE VI.6
READ/WRITE EQUIPMENT

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what are called the operation lines, any one of several heads may be utilized without disturbing the remainder. Figures VI.6 and VI.7 apply to the 40 digit channels only.

The circuit diagram shows a single-ended coil, i.e., no center tap exists. There are three excellent reasons for using a single-ended design as opposed to push-pull. In the first place, only one driving tube is necessary. Secondly, since the push-pull circuit normally returns the center tap to ground, twice as much signal voltage is available from a coil of limited volume. And lastly, the center tap is a nuisance feature in head construction.

It must not be thought that the rms current flow in a single-ended driving tube is twice the rms current in the push-pull circuit. Since twice the number of turns are available on the single-ended coil as opposed to a split coil, the required single-ended coil current is $1/2$ that of the other. The 50% efficient single-ended coil driving tube may therefore be called upon to conduct the same amount of current as that in either tube of the balanced circuit. Since any of the tubes described could be "on" continuously, the heat dissipation requirements are equal.

We omit a description of recording head construction because difficulties in mechanical fabrication are yet to be overcome. On the other hand, tests on a few experimental models enable a prediction of the following characteristics at a tape speed of 50 in./sec.

- (1) The track width is 0.100 inches,
- (2) The magnetic material is unlaminated high silicon steel (commonly called audio iron).
- (3) The recording gap is about 0.001 inch long.
- (4) Saturation excitation is about 10 ampere-turns.
- (5) Output voltages are 15 microvolts per turn peak-to-peak.
- (6) Output pulse lengths are about 100 microseconds.
- (7) Output pulse rise times are of the order of 50 microseconds.

Reliable triggering of the reading toggles will be assured if, under the worst possible conditions, the amplitude of the trigger signals is greater than the largest spurious signals. It may be assumed that perfect recording fields are always presented to the tape during writing operations since the fields used are sufficient to saturate the tape. Therefore, spurious signals and amplitude variations in the reading pulses will arise from imperfections

in the reading process and the tape itself. Let the quantity S denote the amplitude of a readout pulse under ideal conditions. N will denote the amplitude of spurious or noise signals, and let L be the greatest fractional loss to be expected in a readout pulse. The requirement that the weakest possible trigger pulse be greater than the largest spurious signal may be written

$$S(1-L) - N > N \quad \text{or} \quad N < \frac{S(1-L)}{2}$$

Hence the effective noise level must be less than $1/2$ of the weakest expected reading pulses. This is equivalent to a 6db signal/noise ratio for weak signals.

The order of magnitude of tape area used in the memory system is 50 ft². There is no reason to expect that such an area of tape will be free from pinholes in the oxide coating. The effect of a pinhole as large as the track width is to force the recorded flux lines away from the surface in the neighborhood of the hole. The amount of flux locally leaving and re-entering the tape could be as large as $1/2$ the amount leaving or entering at the location of a normal field reversal.

While pinholes as large in extent as a track width ($1/10$ inch, for example) are not to be expected, the possibility of their existence in the tape must be considered. It is clear that the presence of large pinholes is apt to make the local signal/noise ratio as low as 6db. If reliable triggering is to be obtained, the pinholes must be avoided by not using the affected region for storage, or by developing coatings that are hole-free. The presence of a single incorrect trigger pulse would make the entire memory system useless.

On certain pieces of tape used in the laboratory, holes and even large open regions have been observed in the coating. On the other hand, about as many pieces of tape have been hole-free as far as the eye can tell. Experimental equipment for locating holes by means of spurious signals is being built. Until further evidence is presented, the assumption is made that a means of avoiding pinholes will have to be built into the tape memory system. The method used will probably be nothing more or less than the avoidance of certain portions of the tape after they have been proven to make mistakes in a test run. The avoiding decision can be automatic or taken care of in the programming. The automatic decision is discussed elsewhere.

Noise signals can arise in the following ways, aside from tape pinholes. A low-frequency noise has been observed in the drive that has been traced to tape or head vibrations (probably induced by gear hum). Since the useful reading pulses are of relatively short duration, proper adjustment of the amplifier time constants will reduce this noise. However, the

the amplifier tends to overshoot under these conditions, creating an effective noise for signals of opposite polarity. Our experience is that the proper frequency response adjustments in the amplifier will reduce the combined amplitude low frequency jitter and pulse overshoot to less than 5% of nominal signal amplitude.

Another source of noise is cross talk between the heads on adjacent channels. It has been established that the cross-talk amplitude is 30% of signal amplitude with absolutely no shielding between heads. It is not unreasonable to expect that a tenfold improvement in this figure will be attained in the shielded heads currently under development. Hence a 3% cross-talk amplitude is assumed between adjacent pairs. Since all but the outside channels have two neighbors, the total cross-talk amplitude is assumed to be 6%.

A third and troublesome source of noise is that caused by channel drift. Because the tape cannot be made to run through the drive in exactly the same way during successive passes, some swaying of the channels in a sideways fashion is bound to occur. Suppose that in one recording run a record was created with the tape at an extreme limit of permissible sway, and that in a subsequent new recording run the impression is made with the tape at the opposite extreme. If the tape sway were a maximum of $X\%$ of a channel width, then the new recording has erased all but $X\%$ of the former record. Therefore, it is possible that in reading the latest record, $X\%$ of the old record is introduced as noise. At the same time only $100-X\%$ of the new record is being read. Lateral distortions in the tape caused by humidity and temperature changes will lead to the same effect as tape sway, the amount of tape sway being, in fact, directly dependent on these changes. As previously pointed out, maximum sways on the order of 0.010 inch (0.2%) will be possible in the present drive. The track width is 0.100 inch (with a 0.015-inch spacing) so that the $X\%$ in the above argument becomes 10%.

Lateral variations in gap locations on various heads (to be used on the same tape) can also simulate the effect of tape sway. However, the precision to which the gaps can be placed is much better than 10% of the track width and will be neglected. Also, noise signals generated in the amplifiers can be made negligible with no difficulty.

Summing the expected noise amplitudes from the three items, namely, vibration and overshoot, cross talk, and old records, the predicted noise level is seen to be a maximum of around 20% of nominal signal.

Loss of signal amplitude can arise in three ways. First and most predictable is a loss of tape speed. If the clutch mechanism under construction functions at all, the speed of the tape will definitely be within 5% of maximum during reading and writing operations. Since signal amplitude

is closely proportional to tape speed, a maximum signal loss of 5% is assumed for this imperfection.

A further loss in signal, pointed out above, is that caused by tape sway, which is estimated at no more than 10%.

The third possible loss of signal arises from variations in oxide coating thickness. It has been observed that signal amplitude is more or less proportional to coating thickness. Since the nominal coating is less than 0.001 inch thick (2 mil tape), direct measurement of variations in coating thickness is difficult. However, by utilizing an endless loop of tape in a special testing device where the sway and speed are slowly changing, observations of variation in signal amplitude are possible. No variations larger than 20% were found, and the vast majority of pulses were, for practical purposes, identical in height. The largest loss in signal amplitude from this cause will be assumed 20%.

Adding the foregoing losses, one finds that it is possible to lose as much as 35% of the signal amplitude if the above imperfections are all present at the reading of a pulse. Substituting $L=0.35$ and $N=0.20S$ in the relation $S(1-L) - N > N$, one finds that it is satisfied by more than a factor of 2. Hence it is reasonable to expect the reading toggles to function correctly, provided adequate measures are used to avoid the use of regions containing pinholes.

To summarize, a discussion of amplitude errors shows that the ratio of the amplitude of a wanted pulse will always be greater by a factor of two than any unwanted pulse. This factor is more than enough to establish positive triggering of a flip-flop.

Experiments aimed at obtaining statistics on the amplitude of many millions of reading pulses are being planned. Values for the probabilities of small-signal and large-noise pulses will be one of the results.

The operation of 40 parallel digit channels implies a certain precision of timing. Timing errors in the gates can be neglected since they are actuated by a common source. The important timing errors are those caused by imperfect spacial relationships between the digit channels and synchronizing channel. It is convenient to assume that no error exists at the time of recording. An error in read-out timing occurs if (1) the tape has been distorted in such a way as to displace the digit channels relative to the sync channel, (2) the direction of tape motion has changed in such a way as to advance or retard digit channels with respect to the reference channel, (3) the head used in reading differs from that used in creating the record, and (4) the amplitude of the digit or sync pulses varies. The timing will be acceptable if the total effective displacement of any digit channel relative to the sync channel does not exceed $1/2$ a word length.

(digit length). The displacements caused by any one of the four imperfections must therefore be substantially less than $1/2$ a word length.

Tape distortion may be either shear or stretch or both. A conservative estimate of the stretch is $\pm 1\%$. This estimate includes the stretch caused by mechanical stress, humidity changes, and temperature changes. Until further experimental evidence indicates otherwise, it is assumed that the tape does not shear. This assumption is based on the fact that the drive mechanism has no way of imposing large shearing strains on the tape, and that humidity- and/or temperature-induced distortions are shear-free. The latter was verified by direct measurement on a thoroughly wet piece of tape subsequently dried.

The displacement caused by tape stretch is a function of the longitudinal distance (sometimes called "staggering" distance) between the digit heads and sync head. For a tape stretch of 1% , the displacement is $1/100$ of the word lengths separating the heads.

The head assembly will use a maximum "stagger" of about 4 word lengths. Therefore, one finds that the timing errors induced by tape stretch are no more than $1/25$ word length.

The displacement caused by changes in the direction of tape motion (skew) is dependent on the transverse distance between digit and sync heads. If the greatest possible skew is the angle α , and the greatest transverse distance involved is R , then the maximum displacement error is αR . It is clearly desirable to locate the sync heads in the center of the tape and to pack the heads as closely together as possible.

On our drive, R is $2\frac{1}{2}$ inches. The skew angle α is extremely difficult to measure while the drive is in motion. It may be estimated by imagining the "free" tape between the windup reels to be laid out on a flat surface (Figure VI.8). Provided the tape is straight, the skew angle is the ratio of maximum sway to "free" tape length. Using a maximum sway of 0.010 inch (0.2%) and a tape length of 30 inches, the skew turns out to be $1/3000$ inch per inch (radians). Hence αR , the skew error, is $1/1200$ inch or $1/12$ word length.

The timing errors caused by differences in head construction will depend on the precision which can be achieved in the longitudinal placement of the gaps. We believe that a precision of 0.0005 inch can be attained by suitable construction techniques. A total variation of 0.001 inch or $1/10$ word length in relative gap placement is therefore assumed.

The greatest possible errors in timing arising from a change of pulse amplitudes in the digit or sync channels depends on the rise time of the pulses. This rise time is about $1/4$ word length. Thus, the maximum

FIGURE VI.8
FLAT VIEW OF TAPE WITH EXAGGERATED SKEW

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deviation in relative timing because of amplitude variation is assumed to be $1/4$ of a word length.

Summing the foregoing timing errors, one finds that a total error of slightly under $1/2$ word length is possible. The timing will be acceptable if the estimates of the errors are correct. However, considerable doubt exists concerning the skew, and, consequently, a direct measurement of timing error will be made in the near future. If the experimental determination indicates unsatisfactory timing, two courses of action are possible. The precision of the drive may be improved, or the length of a word may be increased; the latter is by far the easier procedure.

VI.4. Control. The variety of ways in which control of a tape memory system can be effected is so great that no attempt is made to discuss them. Instead, a rough description of the contemplated control for this tape drive is presented. The description is not very detailed because at the present stage of development, modifications are highly probable.

The parallel nature of the tape mechanism, together with its relatively high tape speed, enables operating speeds of the order of $1/10$ that of the electrostatic memory to be attained. However, these same factors cause the starting/stopping distances to be several words in length. It is apparent, therefore, that information transferred between the two memories in a single operation should be several words in extent. That is to say, the shortest operation involved should consist of the transfer of a group of words called a block. The number of words to be used in a block is a quantity not easy to specify. It is desirable to use as high a number as possible for reasons of tape efficiency. On the other hand, flexibility in programming requires the use of a minimum number.

From an engineering point of view, the number of words in a block should be a power of two. This follows from the use of binary counters, and the desire that an integral number of blocks shall fill the high-speed memory (2^{10} words).

The contemplated control scheme will provide for the reading and writing of any number of blocks from 1 to that number necessary to fill the fast memory. The words/block will be a flexible quantity in the sense that one of the values $2^5, 2^6, \dots, 2^{10}$ can be selected manually. The setting used will be governed by the problem under solution.

The operating speed of the tape is high enough so that hunts of an extended nature are feasible. In order that the computer proper will not waste time during hunts, provision will be made for the tape to be able to obey hunting orders without tying up the rest of the machine. Of course, an interlock feature to prevent the acceptance of a new tape order until a hunt is finished must be provided. In programming a problem for hunts of

the foregoing nature, greatest efficiency results when the hunts are given as early in the coding sequence as possible. The hunting order will cause the tape to traverse from 1 to 2^{10} blocks without affecting the contents of either memory system.

A better understanding of the general control scheme results from a study of the tape orders. Of the twenty digits in an order, one digit will always be used to distinguish between tape and other orders. If the order is a tape order, four digits will select the following possibilities:

2 digits for selecting the actions read, write, hunt forward, hunt back (read/write in forward direction only);

2 digits to select one out of four possible tape units.

In a read/write order, the usual ten digits will denote the address (in the electrostatic memory) of the starting point of the sequence of words to be transferred. The remaining five digits will establish the number of blocks to be transferred (32 maximum).

In a hunt order, 10 digits will specify the number of blocks to be traversed; the remaining five are unused.

As an intermediate storage device, the tape unit must be capable of locating a block of information as short as 0.32 inch in length (32 words at 100 words/inch). Since total tape lengths will be several thousand times this distance, some precise means of locating the blocks is demanded. Furthermore, it has already been pointed out that a precision synchronizing channel for gating out individual words in a block is necessary. The most difficult aspect of the location problem is connected with the recording operation. In a discussion of read-out errors, it was pointed out that cross talk is not negligible. The cross talk mentioned was that existing when every channel in the recording head assembly is reading out. The cross-talk interference on a read-out channel is expected to be severe if some of the other channels are recording. This is particularly true when the read-out channel is a single sync channel and the recording channels are the 40 digit channels. Hence, for the sake of reliability, the sync channels will be assumed useless (for reading purposes) while writing takes place in the digit channels. The immediate consequence is that precision placement of the words in a block is impossible. It is necessary, instead, to place the words in as accurate a manner as practical and simultaneously impress a new synchronizing record. The required precision will be regained in subsequent reading operations. The starting point for each block will be contained on a second channel, the pulses from this channel to be sensed only when the digit heads are quiescent.

For convenience, the second channel will be called the block channel, and the pulses thereon, block pulses. Similarly, the first channel containing the detailed synchronizing record is called the word channel, and the associated pulses are called word pulses. The latter pulses are of two types, denoted by P and N. When writing is taking place, the equivalents of the word pulses are called the clock pulses; they are also of the types P and N.

The block channel is initially recorded on the tape as part of the setup process on a problem. Thereafter, the channel is used in a read-out fashion only.

Assume a tape with the block channel in place. The block pulses are spaced so that ample room between successive pulses is available for placing the desired number of words regardless of minor speed and stop/start variations.

The sequence of events to take place in a writing operation is as follows:

- 1) Receipt of the write order causes the forward starting clutch to be energized. The five digits describing the number of blocks to be written are set up in a counter called the block counter. The writing current is turned on in the word and digit channels; the writing toggles for these channels are simultaneously cleared to zero.

- 2) Receipt of the first block pulse* from the tape causes the block pulse reading apparatus to be rendered inoperative as soon thereafter as possible. The timing clock for generating the PN clock pulses is set into motion.

- 3) The first P clock pulse causes a transfer from memory to accumulator of the first word of the sequence. The pulse also sets the word channel writing toggle to 1.

- 4) The first N clock pulse opens the gates from accumulator to the digit writing toggles and resets the word channel writing toggle to "0."

- 5) (Assuming 16 words/block)

The sequence of alternate P and N clock pulses repeats the action of the first pair, i.e., transfers a sequence of words from the memory to accumulator and thence onto the tape. The P pulse of the 17th PN pair, however, is disregarded as a memory to accumulator action pulse. The

*The relays that initiate the writing current will operate before the arrival of the first block pulse. Thus the writing heads will be quiescent during the block pulse.

17th N pulse immediately following causes a 1 to be subtracted from the block counter and clears the writing toggles to "0." The word channel writing toggle is cycled by the PN pulse pairs, including the 17th.
(n)...

Immediately after the 17th N pulse, the clock is stopped, and the block pulse reading apparatus rendered once more operative.

The successive block pulses repeatedly initiate the cycle (2)... The 17th N pulse always causes a 1 to be subtracted in the block counter. When this counter reads zero, an order-finished signal is sent to the control, the stop clutch is set, and the writing current removed.

A timing chart of the foregoing action is shown in Figure VI.9. For brevity, a single digit channel of a 16-word block is illustrated.

In reading back such a record, the reading toggles must be cleared to the state "0" as the heads pass into the block. From then on, the reading toggles will faithfully follow the magnetic patterns. By differentiating the output of the word channel reading toggle, a replica of the PN clock pulses is obtained.

The sequence of events in a reading operation is very similar to that of the writing operation:

- 1) Receipt of the read order causes the forward starting clutch to be energized. The five digits describing the number of blocks to be read are set up in the block counter.

- 2) Receipt of the first block pulse from the tape causes the clearing to "0" of the digit and word channel reading toggles.

- 3) The second P word pulse opens the gates from digit reading toggles to accumulator, thereby transferring the first word to the accumulator.

- 4) The second N word pulse is an action pulse causing the transfer of the first word from memory to accumulator.

- 5) The alternating PN word pulses repeat the action of the second pair. The 17th P word pulse causes the transfer of the last word to the accumulator, and the 17th N pulse moves it into the fast memory. The 17th N pulse also subtracts 1 from the block counter.
(n)...

FIGURE VI.9 TIMING DIAGRAM FOR WRITING 1 16-WORD BLOCK

Subsequent block pulses initiate the cycle (2)··· until one of the 17th N word pulses causes the block counter to read 0. At this time an end-of-operation signal is passed to the control, and the stop clutch is energized.

Figure VI.10 is a timing diagram for the reading operation corresponding to the previous writing diagram. The digit toggle is shown lagging behind the word channel toggle by about $1/4$ word length for the sake of illustrating timing error. It is clear that timing errors of nearly $1/2$ word length are tolerable. The basic requirement is that the contents of the digit reading toggles be correct during the P pulses.

The sequence of events in the hunt operation is very simple, namely:

- 1) Receipt of order inserts the number of blocks to be traversed into the block counter. The proper start clutch is energized, and an operation-finish signal sent to the control.

- 2) Successive block signals subtract 1 from the block counter. The stop clutch is energized when the block counter reads zero.

A necessary feature of the control system is that starting/stopping the tape shall not cause the missing of a block pulse. To say the same thing in a different way, the tape must always be moving at full speed when block pulses pass under the reading station. The simplest way of satisfying this requirement is to make the space between block pulses large enough to contain the required words and the necessary room for one full stop-start operation.

Since the stopping operation will last for a few milliseconds, it is entirely possible that a new order tending to restart the tape drive will occur before the stop is complete. In the case where the new order implies a reversal in motion (hunt back followed by read/write, or read/write followed by hunt back) the clutch must follow through with the stop and then bring the tape up to speed in the reverse direction. The design of our clutch is such that it is highly desirable to delay all start signals until the latest stop is complete. The situation is similar to that of the hunt order. That is, the computer does not have to wait for the stop clutch, but no new tape order should be permitted until the stop is complete.

The same interlock feature can be used for both situations. The interlock is set at the start of a tape order and opened by a stop-finished signal. An end-of-operation signal will be sent to the control, however, as soon as possible.

A certain waste of time is inherent in the foregoing stopping procedure. The waste of time will appear when any forward moving order is followed closely in the code sequence by another forward moving order.

The most likely case is the forward hunt followed by read/write. Since the hunt is apt to hold the machine up anyway (for as much as several seconds), the wasted time is of small import. A great increase in the complexity of clutch control circuits is necessary to recover this lost time. No attempt at recovery will be made.

If more than one tape unit is used, most of the tape control apparatus will be common to all units. The control that must be built into each unit to achieve the hunt-while-computing feature is that necessary to (1) sense the block pulses (2) count them up to 2^{10} , (3) set the stop clutch, and (4) operate an interlock circuit. A rough block diagram of the tape control is shown in Figure VI.11.

In discussing amplitude errors on the digit channels, the stipulation was made that regions of the tape containing pinholes must be avoided. The avoidance of the affected blocks can be considered as a control problem, of which there are two possible solutions, namely:

- 1) Discover the faulty blocks by means of a check routine utilizing the computer. The blocks so discovered are to be omitted in the coding process.

- 2) Discover the faulty blocks by means of a checking apparatus. Suppress the block pulses belonging to the affected blocks.

The procedure involved in method 1) is self-evident. A brief description of method 2) is presented in order to show the amount of extra equipment needed.

If a continuous state of magnetization at a constant polarity is impressed on a tape, the flux lines will be confined to the tape except at the ends of the record and at places where there is an absence of coating. Therefore, pulses will be obtained in a reading operation only at the locations of coating imperfections (aside from the ends of the record).

Figure VI.12 shows a typical circuit for sensing pulses of magnitude greater than some fixed value on one or more groups of channels. The input diodes will conduct only if the output of the amplifiers exceeds the cathode bias on the diodes. Clearly, the required equipment for forty channels is of limited extent.

The suppressing signals in Figure VI.11 are generated for spurious signals of one polarity only. This is sufficient; every spurious pulse of one polarity is associated with a nearby pulse of opposite polarity.

FIGURE VII CONTROL SYSTEM FOR MULTIPLE TAPE OPERATION

Figure VI.13 shows a block pulse signal generator of somewhat more complicated design than a simple multivibrator and coil driver. In the absence of pulses on the suppression line, this generator will impress return-to-zero pulses at a uniform rate. The recursion period is governed by the time constants of the circuit. However, if a pulse is received on the suppression line, the next following block pulse will not occur.

The suppression of faulty blocks using the above apparatus is automatically accomplished at the time of creating the block pulses. The tape is passed through the drive in a reverse direction; i.e., the block pulse follows the block to which it belongs. The desired suppression takes place because a block pulse cannot be recorded unless every channel has been free of spurious signals for one recursion period. Of course, the recursion period here is intimately related to the block length discussed heretofore.

One limitation of the foregoing system of suppression is that no provision is made for checking the block channel. The use of return-to-zero recording in the block channel greatly reduces the probability of pinhole errors. In fact, the troublesome case is that wherein a pinhole occurs at the same instant the block pulse is being recorded. If necessary, the presence of the block pulses may be confirmed by utilizing the block pulse counter. If a count of block pulses is made during the recording and a subsequent playback, agreement of the counts will establish the correctness of the block channel. The playback count should actually be made twice at different discrimination levels so as to confirm a better than 6 db signal/noise ratio. This ratio is necessary for reliable sensing of the block pulses.

If the counter fails to confirm the reliable operation of the block channel, the simplest procedure is to erase the block channel and start over. Random variations in the block pulse generator will automatically insert the new set of block pulses at new locations. If repeated trials do not prove adequate, the tape should be discarded.

FIGURE VII.13
BLOCK PULSE RECORDING UNIT

NO.	PH6-103-B
DRAFTS	B. G.
AUTHOR	CNU
DATE	6-8-51
D.C.V.	

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