CONF-9605101--4
SAND95-2797C

# Low-Power Modular Parallel Photonic Data Links

R. F. Carson, M. L. Lovejoy, K. L. Lear, M. E. Warren,
P. K. Seigal, G. A. Patrizi, S. P. Kilcoyne,* and D. C. Craft
Sandia National Laboratories
* Now with Optical Concepts, Inc.

## Abstract

Many of the potential applications for parallel photonic data links could benefit from a bi-directional Optoelectronic Multi-Chip Module (OEMCM), where the optical transmitter, receiver, and first-level interface electronics are combined into a single package. It would be desirable for such a module to exhibit low power consumption, have a simple electronic interface that can operate at a variety of speeds, and possess a capability to use interchangeable optics for a variety of external connections. Here, we describe initial results for a parallel photonic link technology that exhibits those properties. This link uses high-efficiency, back-emitting, two-dimensional Vertical Cavity Surface-Emitting Laser (VCSEL) arrays operating at 980 nm. The lasers are matched, via integrated microlenses, to corresponding monolithically-integrated photoreceiver arrays that are constructed in a InGaAs/InP Heterojunction Bipolar Transistor (HBT) technology. In initial breadboard-level tests, the photonic data channels built with these devices have been demonstrated with direct (3.3 V) CMOS drive of the VCSELs and a corresponding CMOS interface at the photoreceiver outputs. These links have shown electrical power consumption as low as 42 mW per channel for a 50% average duty cycle while operating at 100 Mb/s.

## 1. Introduction

Advancements in low power photonic and optoelectronic devices allow new implementations of parallel links both in optical fiber and in free space. Examples of these enabling device technologies include high-efficiency vertical-cavity surface-emitting lasers (VCSELs) and Heterojunction Bipolar Transistor (HBT) photoreceiver circuits that are optimized for low power consumption. If the components resulting from these technologies are designed for modular use, then a variety of implementations can be realized without major changes in the underlying optoelectronic devices. These modules will be particularly useful if they have the ability to be directly interfaced to any point within a digital circuit without major changes to the circuit.

In addition to low power consumption, desirable attributes for modular implementation of optical transmitter and receiver components would be direct, high-fidelity interface with standard CMOS microelectronics and the ability to be mounted in a variety of different packaging arrangements, including Multi-Chip Modules (MCMs) that are connected either by guided-wave or lensed connection optics.

The underlying device technologies for these modular links are currently being studied for use in z-axis interconnection of stacked MCM arrangements. The requirements of the candidate system for these stacks imply highly parallel, dense array of optical links. Design goals associated with this application include direct 3.3 V CMOS interfacing, a total electrical power consumption of only 10 mW per channel, and minimal excess circuitry for operation and implementation. Such an approach would also require CMOS-like data fidelity, thus implying low latency, non-latched Non-Return-to-Zero (NRZ) operation, an extremely low Bit Error Rate (BER), minimal impact on timing margin (about 1 ns rise and fall for a 100 MHz clock), and low latency.

## 2. A Two-Layer Modular Stack Demonstrator

A basic demonstration of the z-axis stacking would be implemented as in Fig 1. Here, the laser and photoreceiver are combined with simple CMOS driver and buffer chips, respectively, in the two layer stack arrangement. This arrangement forms an optoelectronic MCM that could be directly interfaced with processing electronics on a larger module or used for connection on a circuit board.

A cross-section of the modular stack appears in Fig. 2 with a corresponding optical design for collimation and refocus of the light from each laser channel. This approach implies 980 nm light, thus making use of integrated micro-optics in the transparent optoelectronic device substrates. The collimating lens at the back surface of the laser substrate allows for stack misalignment, and keeps the f-number of the refocusing lens at the receiver within a reasonable range. The receiver lens allows the beam to be refocused into a small detector area (50 μm diameter, for this design). This results in a small detector capacitance, which helps keep electrical power consumption at the receiver low, while still maintaining the rise and fall times needed for high data fidelity.

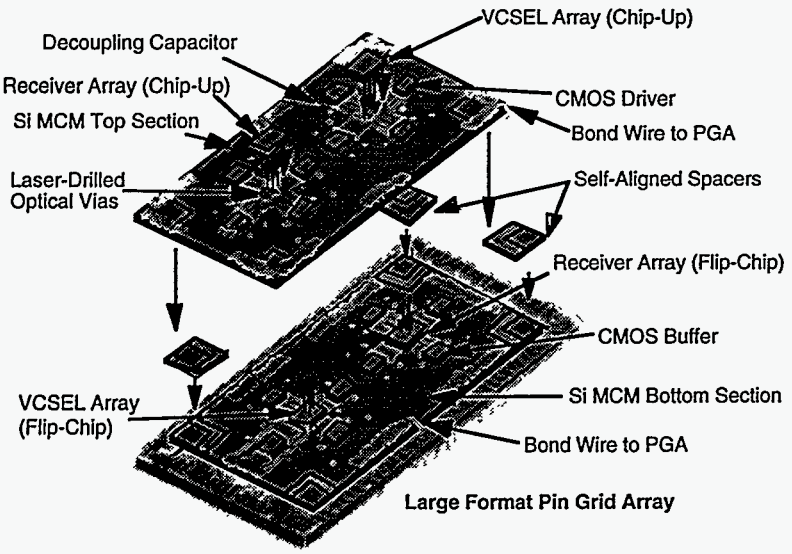



**Figure 1.** A prototype two-layer MCM stack to demonstrate and test concepts using VCSELs, HBT photoreceivers, integrated lenses, direct CMOS interface, and passive alignment methods.

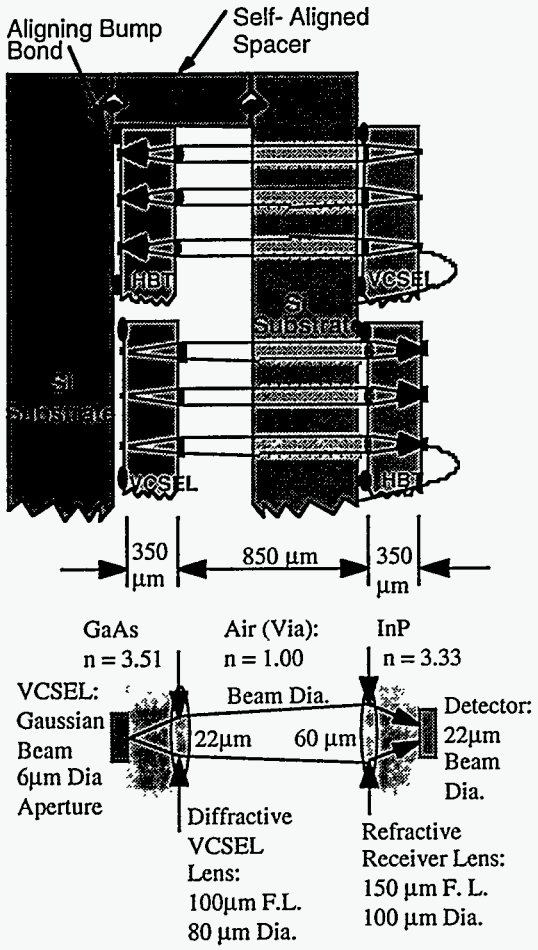



Figure. 2 Cross-section of the two layer stack and a corresponding optical design.

The optical design for this demonstration stack is based on GaAs and InP device substrates having a thickness of 350 µm and a separation of 850 µm as in Fig 2. Based on simple Gaussian beam approximations, this design accommodates lens-to-device misalignments of up to 3 µm and level-to-level misalignments of up to 10 µm by the use of a receiver lens that is larger than the diameter of the optical beam. In our first implementation, the VCSEL lens diameter was 80 µm with a 100 µm focal length for a F/ 1.4 lens. The receiver lens diameter was 100 µm, with a focal length of 150 µm, resulting in a F/ 1.5 lens. This yields a corresponding $1/e^2$ beam diameter of 22 µm at the detector, thus placing the beam well within the detector area.

Note that the VCSEL lenses are implemented on the back side of the GaAs substrate as diffractive optical elements, while refractive lenses are used on the back of the InP receiver substrate. The design and fabrication of these lenses are described elsewhere [1,2]. The alignment tolerance between each VCSEL and its back-side lens is particularly important. Every 1 µm of misalignment between the VCSEL and the lens causes a 10 µm beam offset at the design distance. Thus, accurate front-to-back alignment during the two-sided lithography steps is a needed capability for the integrated lenses. The detector-to-lens alignment at the receiver is less critical, but should still be maintained within a few micometers to allow for greatest system tolerance.

An important packaging feature for the modular stack is also shown in Fig. 2. Note that the VCSEL and photoreceiver die are alternately wire-bonded and flip-chip mounted on the upper and lower submount layers of the stacked module arrangement. On the lower level, the solder bump bonding will provide both alignment and electrical connection to the epitaxial layers of the optoelectronic die. On the upper layer, the bump bonds would only be used for die-to-submount alignment, and the wire bonds would provide electrical connection to the epitaxial device layers. This mixed mounting arrangement results from the fact that light is emitted and collected through the back of the transparent device substrates. In actual multi-level MCM stack arrangements, reflective off-axis binary lenses could be used to effect upward and downward communication between sources and receivers without the mixed mounting described above [3].

High-aspect ratio laser-drilled holes (shown in light shading in the upper substrate) are used to provide optical vias for light to pass through, since the silicon submount material is

not transparent at the 980 nm wavelength. Etched alignment features provide stack alignment tolerance.

The lower layer of the demonstration stack in Fig. 2 can be used in a variety of modular configurations to realize either guided-wave or free space optical interconnects. One approach for longer distances in free space would be to add external microlens arrays to provide additional tolerance for board-to-board communications. An alternative to this would be to provide integrated collimating and focusing lenses on the VCSEL and photoreceiver that are optimized for the distances and tolerances required for board-to-board interconnects. As demonstrated in [4], this would require lenses with longer focal lengths, resulting in the need for thicker substrates and/or wafer bonding techniques. The external lens approach, however, uses a relatively standard wafer thickness for the photonic and optoelectronic devices.

In other arrangements, the laser-drilled via holes in the top layer of the silicon stack in Fig. 2 could be used to hold a two-dimensional array of optical fibers. This would enable communications over a longer link length by taking advantage of the ability of optical fiber to confine the generated light.

## 3. Enabling Device Technologies

Because of their low-divergence beams and highly efficient light generation characteristics at the mW level, VCSEL-based transmitters enable optical links with high efficiency, low cross-talk, and (with integrated lenses) bi-directional transmission. In addition, VCSEL devices have shown high (14-16 Ghz) [5,6] small-signal modulation bandwidths. It follows that the devices should easily meet the speed requirements of directly-driven parallel links and have a substantial capacity for scaling to higher bit rates (with a corresponding increase in driver complexity and power consumption). VCSELs can also be designed for optimized sensitivity to ambient temperature excursions [7]. VCSEL arrays have been constructed that are compatible with the interconnect of Fig. 1. These are 4 x 4 arrays of 980 nm back-emitting devices on GaAs substrates, built both as gain-guided and index-guided devices. The relative merits of both device types have been discussed previously [3]. Important features of the VCSELs that are to be used in the modular stack approach are the ability to be operated directly from 3.3 V CMOS (no pre-bias) with low power consumption and turn-on delays less than 1 ns.

Photoreceiver arrays that match the 980 nm VCSELs have been constructed in a InGaAs/InP Heterojunction Bipolar Transistor (HBT) technology. These circuits use back-illuminated p-i-n detectors monolithically integrated as the base-collector junction of the HBT epitaxial stack. Circuit details have been described elsewhere [8].

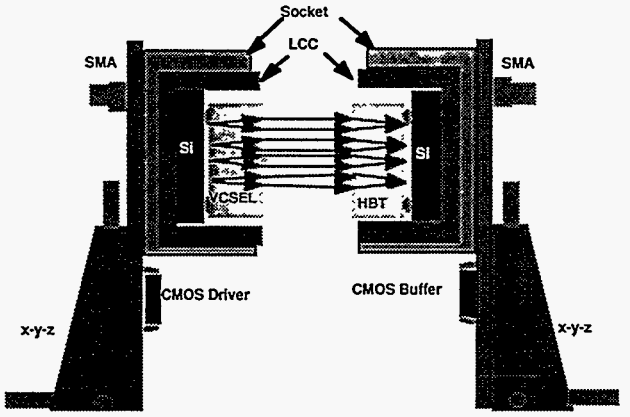
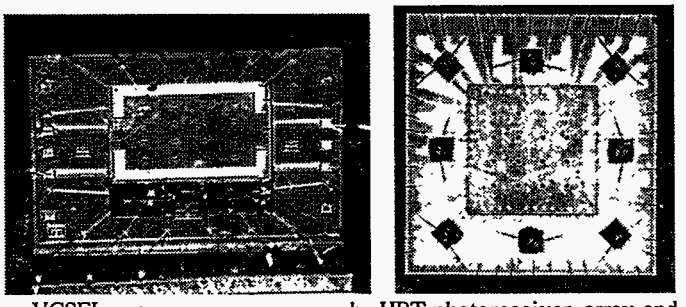



**Figure 3.** Breadboard test cross-section. The lensed VCSEL and HBT can be brought into close proximity for alignment testing. The laser and HBT arrays are directly interfaced to 3.3V CMOS circuits.

## 4. Board-Level Demonstration Results

The devices and optics to be used in the modular arrangements of Figs. 1 and 2 were tested in a board-to-board cross-section as in Fig. 3. Circuit boards were designed and fabricated to allow for simultaneous testing of up to 16 channels of optically-linked data. These tests were done both to determine performance of the VCSELs and photoreceivers with direct CMOS drive and buffering, and to explore the range of stack alignment tolerance afforded by the optical design of Fig 2.

The laser and photoreceiver die were flip-chip mounted on silicon submounts and placed in Leadless Chip Carriers (LCCs), thus allowing for interchange of devices in the board-level tests. The VCSEL die were mounted on the silicon subcarrier as in Fig. 4a. Here, the 350 μm thick GaAs VCSEL substrate was flip-chip bonded using indium-alloy solder paste. The 4 x 4 diffractive lens array with 0.5 mm pitch is visible on the back side of the die in Fig. 4a. One-mil gold wedge wire bonds connect the carrier to the



a. VCSEL array. b. HBT photoreceiver array and supply capacitors.

**Figure 4.** Transmitter and receiver die flip-chip bonded onto silicon submounts in leadless chip carriers.

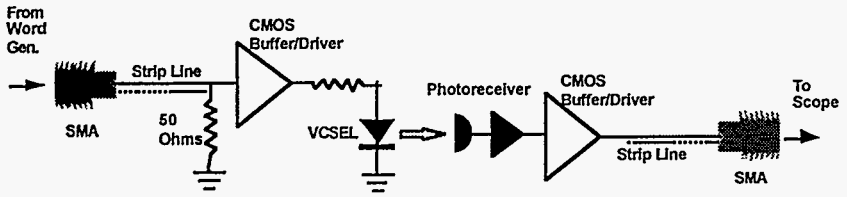



**Figure 5.** Board-level test circuit schematic.

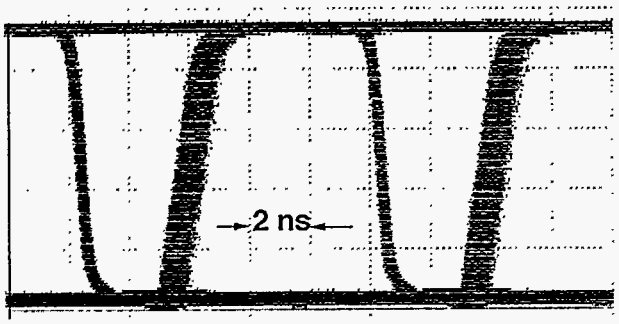
pads of the 28 pin LCC. Multiple ground connections on the LCC minimize common-path de-bias and signal cross-talk effects. In order to further minimize any de-bias effects, ground lines on the submount were constructed with additional width. Capacitance for each packaged laser channel at zero bias was measured at 28 pF when 20 μm diameter implanted VCSELs were used.

The photoreceiver was mounted on a silicon submount as in the top view of Fig. 4b. In this case, the InP substrate (with its array of refractive lenses on a 0.5 mm pitch) was thermosonically bonded onto the silicon submount using Au/Pd bumps. Though thermosonic bonding does not allow for the self-alignment effects that make solder bumps advantageous [9], it is a process that is readily available for prototyping, and in could result in acceptable die placement on a MCM when used with high-accuracy pick-and-place technology. Separate $V_{cc}$ lines for each channel on the device die were carried to the LCC. One ground line was provided for every two circuit channels. As shown in Fig. 4b, a 140 pF capacitor was placed between the power and ground for every two circuits.

The circuit of Fig. 5 was reproduced by each of the sixteen channels on the circuit board pair. Input data was applied via a 50 Ohm line into the SMA on the input side of the link. The data signal traveled down approximately 4 inches of microstrip line to a 50 Ohm termination resistor at the input to a CMOS driver. The drivers used were Integrated Devices 74FCT163244 3.3V CMOS buffer/driver circuits designed to operate at 50 Mb/s. To keep untuned line lengths short and equidistant as possible, only eight of the sixteen possible channels were used on each of two driver ICs on the VCSEL board. A series resistor was placed between each driver output and its VCSEL to control input current and corresponding light output. The resulting photoreceiver response was fed into an identical CMOS buffer/driver on the second board. The buffer circuit was used to drive the 50 Ohm lines that fed data to a digital oscilloscope.

The eye diagram of Fig. 6a was generated for a single channel on the test board pair, operated at the design supply voltage of 3.3V with optimal laser-to-receiver alignment. The lasers used were implanted devices with a 20 μm active region diameter. A 24 ohm series resistor was used as in Fig. 5, to give a nominal laser drive current of 20 mA leading to a total demonstrated power consumption of 45 mW (66 mW peak for the laser, multiplied by a 50% average duty cycle, and 12 mW for the receiver). Peak laser output into the 100 μm receiver lens (including optical losses associated with imperfections on the diffractive lens) was 0.9 mW. Here, 100 Mb/s NRZ pseudo-random data was used,


a. Board level test results: eye diagram with a 3.3 V source for the VCSEL board.




b. Eye diagram for a 2.7 V supply voltage on the VCSEL board. Note degradation of usable pulse width and jitter.

**Figure 6.** Test results for the board level demonstration interconnect, showing operation at a supply level of 3.3 V (0.9 mW peak laser output) and 2.7 V (0.5 mW peak laser output).

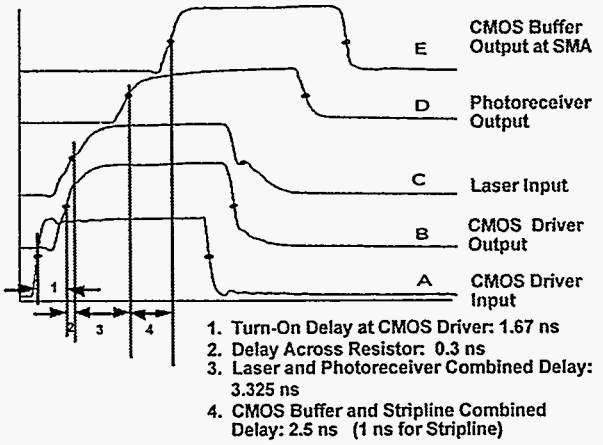



**Figure 7.** Timing diagram for various points on the test board arrangement. Traces were taken using an active, high-impedance probe, and show the origin of delays within the interconnect.

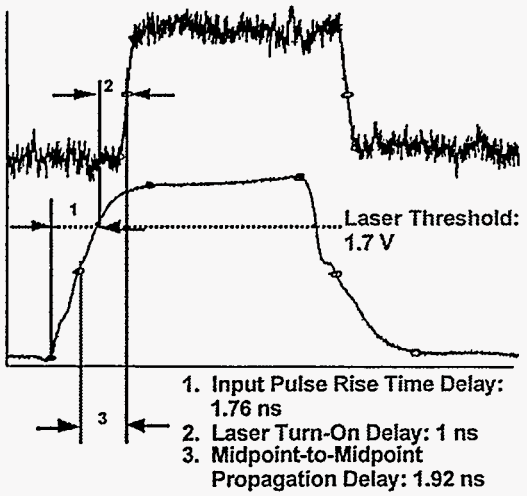



**Figure 8.** Laser timing response when driven in the test board circuit. Note the combined effects of rise time and turn-on delay.

and the resulting eye in Fig. 6a is very open, with transition times of 1 ns and a jitter of approximately 0.25 ns. In order to test the effects of laser power, the source voltage for the transmitter circuit was dropped to 2.7 V. In this case, the laser was operated at a nominal 16 mA peak input current for an output of 0.53 mW. This lower laser power reduced the usable portion of the 10 ns window to 5 ns and increased jitter to near 1 ns as in Fig. 6b.

The timing curves of Fig. 7 were generated using a single, 100 k Ohm active probe on a 3 GHz oscilloscope sampling head and storing the voltage traces from the measurements taken at various points within the circuit of Fig. 5. The design value of 3.3V for transmitter and receiver was again used as the supply voltage. The results of Fig. 7 indicated that the total delay from buffer-to-buffer for this link was 6.8 ns. Of this total, 3.3 ns of the delay could be attributed to the laser and photoreceiver. The input and output CMOS buffer/drivers (with their 50 Mb/s design rating) accounted for 1.7 and 1.5 ns, respectively. To evaluate the relative proportions of the delay due to the laser and the photoreceiver, the light output from the laser was measured using a fast photodiode as in Fig. 8. Here, 1.7 ns of the total delay is due to the time needed for the drive signal to reach the laser threshold point and 1.0 ns is due to laser turn-on delay.

These results were obtained for an implanted (gain-guided) VCSEL with a 20 μm active region diameter. Smaller (10 μm) diameter implanted VCSELs showed much larger turn-on delays (up to several hundred ns) that precluded their use in non-pre-biased NRZ operation. Such long delays were not present in 10 μm diameter etched-post (index-guided) devices [3]. Both device types showed an overall delay that was dominated by the rise time of the CMOS drive pulse and the level of the drive above threshold. It follows that index-guided devices might be advantageous in these direct CMOS drive applications if built smaller to produce lower capacitance and threshold current.

The relative positions of the transmitter and receiver boards could be manipulated to test alignment tolerances as indicated in Fig. 3. This was done for several different separation distances and results appear in Fig. 9. The criterion used to evaluate alignment tolerance was pulse width from the CMOS buffer on the receiver board. As demonstrated by comparing the curves in Figs. 6a and 6b, the pulse width from the CMOS fell as laser power was decreased, thus reducing the effective timing margin for the link. This was due both to increased delay in the photoreceivers for lower input photocurrents, and reduced output amplitudes from the photoreceiver into the CMOS buffer. The latter effect is illustrated by output curve D in Fig. 7, where the output must reach a certain level to trigger the CMOS buffer. As input laser power is reduced, the overall peak level of the photoreceiver output drops. The threshold point then moves farther along curve D, eventually transferring from the steep portion to the more gradually rising portion. This would also increase jitter, as in Fig. 6b. At even lower powers, the entire output will fall below the threshold point of the CMOS, and the link will cease to function. This same effect occurs as the receiver and laser boards are offset in Fig. 9. Note that the collimation and re-focus of the optical system

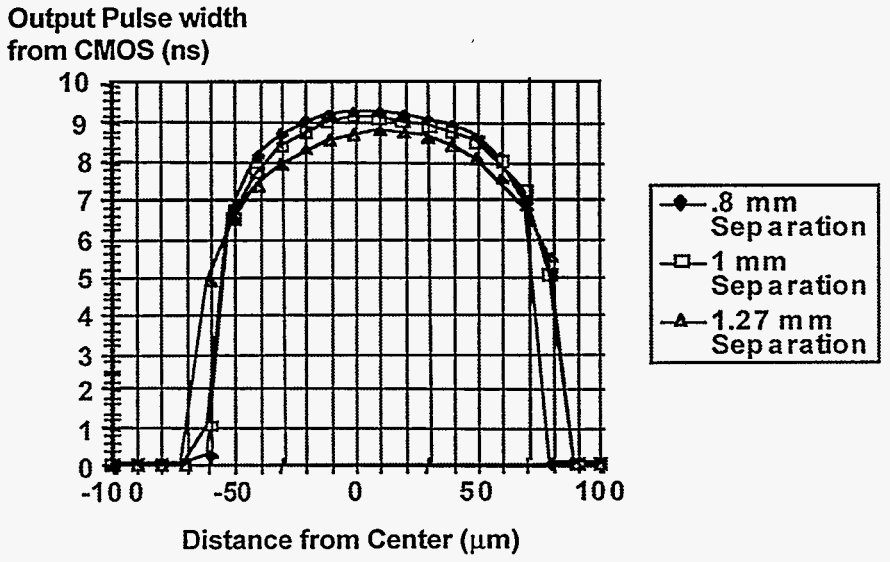



**Figure 9.** Effects of misalignment on output pulse width and link operation for three laser-to-photoreceiver separation distances.

allows for operation with greater than 9 ns of width over a +/- 25 μm alignment tolerance. As the misalignment becomes worse, the timing margin and jitter would degrade as in Fig. 6b. This experiment shows that timing margins can be maintained within reasonable stacking tolerance values for the z-axis MCM interconnect application, that the basic drive and timing characteristics needed for a modular implementation could be realized using the lensed VCSEL and HBT devices described, and that the use of such devices can greatly ease alignment constraints for modular MCM-based interconnects of various types.

## 5. CONCLUSION

The results of the board-level demonstration indicate that this photonic interconnection link technology is compatible with the system requirements of many optoelectronic MCMs. The VCSEL and HBT devices can be optimized to meet stringent power budgets, and arrays could be expanded to produce large numbers of synchronous, uncoded, parallel photonic data channels. Each channel will operate at clock speeds up to several hundred MHz, limited by the speed of the direct CMOS interface. Integrated microlenses can greatly increase alignment tolerances and provide for easier packaging. This interconnect approach could thus solve the problem of providing separable, high density, two-dimensional interconnects for stacking of MCMs and could additionally be applied to more generalized modular optical links that are to be interfaced to CMOS circuitry.

### Acknowledgments

The authors gratefully acknowledge the technical support of Denise R. Tibbets-Russell, Melissa A. Cavaliere, Glen Knauss, Terry Hardin, Florante Cajas, John Nevers, and Tony Carter. Contributions were also made by the related work of Tu Du, Joel Wendt, Alan Vawter, Olga Blum, Kent Choquette, and Ben Rose. All work was performed at the Sandia National Laboratories for the United States Department of Energy under Contract DE-AC04-94AL85000

### References

[1]. O. Blum, S. Kilcoyne, M. E. Warren, T. C. Du, K. L. Lear, R. P. Schneider, R. F. Carson, G. Robinson, and F. H. Peters," Vertical Cavity Surface-Emitting Lasers with Integrated Refractive Microlenses," *Electronics Letters.*, vol. 31, no. 1, pp. 44-45, 1995

[2]. M. E. Warren, T. C. Du, J. R. Wendt, G. A. Vawter, R. F. Carson, K. L. Lear, S. P. Kilcoyne, R. P. Schneider, and J. C. Zolper, "Integration of Diffractive Lenses with Addressable Vertical-Cavity Laser Arrays," *Proceedings of the SPIE,* vol. 2398, pp. 12-20, 1995.

[3]. R. F. Carson, M. L. Lovejoy, K. L. Lear, M. E. Warren, P. K. Seigal, D. C. Craft, S. P. Kilcoyne, G. A. Patrizi, and O. Blum, "Low-Power Approaches for Parallel, Free-Space Photonic Interconnects," *SPIE Critical Reviews of Optical Sciences and Technology,* vol. CR62, pp. 35-63, 1996.

[4]. L. A. Coldren and B. J. Thibeault, "Vertical-Cavity Surface-Emitting Lasers for Free-Space Interconnects," *SPIE Critical Reviews of Optical Sciences and Technology,* vol. CR62, pp. 3-34, 1996.

[5]. G. Stengel, H. Temkin, P. Brusenbach, T. Uchida, M. Kim, C. Parsons, W. E. Quinn, and S. E. Swirhun, "High-Speed Vertical-Cavity Surface Emitting Laser" *IEEE Photonics Technology Letters,* vol. 5, no. 12, pp. 1359-1362, 1993.

[6]. K. L. Lear, A. Mar, K. D. Choquette, S. P. Kilcoyne, R. P. Schneider, and K. M. Geib, "High-Frequency Modulation of Oxide-Confined Vertical Cavity Surface Emitting Lasers," Submitted to *Electronics Letters.*

[7]. D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. A. Coldren, "Enhanced Performance of Offset-Gain High-Barrier Vertical-Cavity Surface-Emitting Lasers," *IEEE J. of Quantum Electronics,* vol. 29, no. 6, pp. 2013-2021, 1993.

[8]. M. L. Lovejoy, G. A. Patrizi, P. M. Enquist, B. H. Rose, D. B. Slater, Jr., R. J. Shul, R. F. Carson, D. C. Craft, and J. A. Hutchby, "Low-Power, High Speed InGaAs/InP Photoreceiver for Highly-Parallel Optical Data Links," *GaAs IC Symposium Technical Digest 1995*, pp. 181-184, 1995.

[9]. Y. C. Lee and N. Basavanhally, "Solder Engineering for Optoelectronic Packaging," *Journal of Metals*, vol. 46, no. 6, pp. 46-50, 1994.

## DISCLAIMER