Development of High-Efficiency, Thin-Film CdTe Solar Cells

Final Subcontract Report 1 February 1992 - 30 November 1995

A. Rohatgi, H. C. Chou, S. Kamra, A. Bhat
*Georgia Institute of Technology
Atlanta, Georgia*

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

Development of High-Efficiency, Thin-Film CdTe Solar Cells

**Final Subcontract Report
1 February 1992 – 30 November 1995**

A. Rohatgi, H. C. Chou, S. Kamra, A. Bhat
*Georgia Institute of Technology
Atlanta, Georgia*

NREL technical monitor: B. von Roedern

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of
the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

Prepared under Subcontract No. XG-2-11036-3

January 1996

MASTER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

This publication was reproduced from the best available camera-ready copy
submitted by the subcontractor and received no editorial review at NREL.

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (615) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650

ACKNOWLEDGMENTS

The authors would like to thank Dr. R.R. Arya and Ms L. Russell of Solarex Corporation for providing the SnO_2 -coated glass substrates and the recipe for solution growth of CdS films. We would also like to thank Dr. Bolko von Roedern, Dr. Harin Ullal, and Dr. Kannan Ramanathan of NREL for their constant help and useful discussion throughout this project period. We would like to acknowledge Dr. R.K. Ahrenkiel and Dr. D.H. Levi of NREL for the time resolved PL measurements, Dr. M.M. Al-Jassim and Mr. R.J. Matson of NREL for the EBIC measurements. We give our special thanks to Dr. R.W. Birkmire of IEC, Dr. A.D. Compaan of U. of Toledo, Dr. C. Ferekides of USF, Dr. P.V. Meyers of SCI, and Dr. J.R. Sites of CSU for the collaboration and useful discussion in this work, Dr. I. Bhat of RPI for the supply of CdTe/GaAs samples.

We would like to acknowledge the support of Microelectronic Research Center and the Material Science and Engineering Dept. at Georgia Tech for the use of their facilities. We would like to thank Dr. N.M. Jokerst for her guidance in developing lift-off/etch-back cell structure, Dr. E.W. Thomas for his help in the SIMS measurement and useful discussion. We would also like to thank Dr. Alan Doolittle for his help in instrumentation and useful discussion and Dr. A.W. Smith for his assistance in writing the J-V-T program for transport analysis. We would like to acknowledge Dr. W.B. Carter for the assistance in the AES measurements, Dr. S.R. Stock and Mr. S.L. Lowrie for the help in the DCRC measurements, Dr. Arun Gokhale and Mr. Shichen Yang for the helpful discussion related to the fractional coverage associated with the grain boundaries.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS	ii
LIST OF TABLES	vii
LIST OF FIGURES	viii
SUMMARY	xiv

CHAPTER

I INTRODUCTION

1.1 Introduction and Statement of Problem	1
1.2 Historical Survey of CdTe Solar Cells	4
1.2.1 CdTe Material: Advantages and Problems	4
1.2.2 CdTe Solar Cell Structures	8
1.2.3 CdTe Deposition Techniques for Thin Film Solar Cells	11
1.3 Overview of the Report	17

II TECHNICAL BACKGROUND, MOTIVATION, AND RESEARCH OBJECTIVES

2.1 Introduction	19
2.2 Solar Cell Device Physics	20
2.3 Heterojunction Theory	26
2.4 Current Transport Mechanisms in Heterojunction	30
2.5 CdTe/CdS Cell Efficiency Limiting Defects and Mechanisms	44
2.5.1 Native Defects in CdTe	45
2.5.2 Grain Boundary Effects in Polycrystalline CdTe Cells	48
2.5.3 The Effects of CdTe/CdS Interface States	49
2.5.4 Photocurrent Loss in CdS Window Layer	51
2.5.5 CdCl ₂ Treatment Induced Loss Mechanisms	52
2.5.6 Ohmic Contacts to CdTe Cells	55
2.6 Specific Research Objectives and Tasks	63

III EXPERIMENTAL TECHNIQUES AND PROCEDURES

Table of Contents

3.1	Introduction	70
3.2	Materials Growth, Processing and Device Fabrication	70
3.2.1	Solution Growth of CdS Film	71
3.2.2	Metalorganic Chemical Vapor Deposition (MOCVD) of CdTe Film	75
3.2.3	CdTe/CdS Solar Cell Fabrication	82
3.3	Materials Characterization	84
3.3.1	Scanning electron microscopy (SEM)	84
3.3.2	Auger electron spectroscopy (AES)	87
3.3.3	Secondary ion mass spectroscopy (SIMS)	94
3.3.4	X-ray diffraction(XRD)	98
3.4	Device Characterization	104
3.4.1	Lighted Current-Voltage (I-V) Measurements	104
3.4.2	Current Density-Voltage-Temperature (J-V-T) Measurements ..	105
3.4.3	Quantum Efficiency Measurements	108
3.4.4	Reflectance Measurements	112
 IV ANALYSIS OF PHOTOCURRENT LOSS FROM REFLECTANCE AND ABSORPTION IN CdS AND SnO₂ LAYERS		
4.1	Introduction	116
4.2	Simulation of Current Loss from Reflectance and Absorption	117
4.3	Theory and Modeling of Reflectance	118
4.4	Results and Discussion	120
4.4.1	Theoretical Optimization of CdS and SnO ₂ Thicknesses for Minimum Reflectance	120
4.4.2	Practical Optimization of CdS Thickness for High Efficiency Cells	121
4.4.3	Effect of SnO ₂ Thickness on Photocurrent Losses	127
4.4.4	Minimization of the Front Glass Surface Reflectance	130
4.5	Conclusion	135
 V THE IMPACT OF MOCVD GROWTH AMBIENT ON LOSS MECHANISMS ASSOCIATED WITH THE CdTe LAYER AND CdTe/CdS INTERFACE		
5.1	Introduction	137
5.2	MOCVD Growth and Cell Fabrication	139
5.3	Results and Discussion	142

Table of Contents

5.3.1	Effect of Native Defects on CdTe Thin Film Properties	142
5.3.2	Correlation between Defects, Interface Quality, and Cell Performance	147
5.3.3	Light- and Voltage-Bias-Dependent QE Analysis of CdTe Cells Grown in Cd- and Te-rich Conditions	153
5.3.4	Correlation between Carrier Transport Mechanism and Cell Performance	157
5.3.5	Correlation between Carrier Life Time, Interdiffusion, and Cell Efficiency	164
5.4	Conclusion	166
 VI EFFECTS OF CHEMICAL AND HEAT TREATMENTS ON CdTe MICROSTRUCTURE AND CdTe/CdS INTERFACE PROPERTIES		
6.1	Introduction	168
6.2	Experimental Techniques	170
6.3	The Effects of CdCl ₂ Treatment on Morphology and Grain Size	171
6.4	Rapid Thermal Processing of CdTe Solar Cells	180
6.4.1	Investigation of RTP Solar Cell Performance	180
6.4.2	Correlations Between Interface Diffusion and Post-growth Treatment Using Non-destructive XRD Technique	188
6.5	Conclusion	192
 VII MULTIPLE EFFECTS OF Cu ON CONTACT PROPERTIES AND CELL PERFORMANCE		
7.1	Introduction	195
7.2	Experimental Techniques	196
7.3	Results and Discussion	200
7.3.1	The Effects of Cu on CdTe Cell Performance	200
7.3.2	Effects of Cu Thicknesses on Cell Performance	209
7.3.3	Effect of Cu Thickness on Carrier Transport Mechanism in the CdTe Cells	211
7.3.4	Effect of Cu Deposition Rate on Cell Performance	214
7.4	Conclusion	220
 VIII DEVELOPMENT OF LARGE GRAIN AND SINGLE CRYSTAL CdTe THIN FILM SOLAR CELLS		

Table of Contents

8.1	Introduction	223
8.2	Growth of CdTe Films with Different Degrees of Crystallinity	224
8.3	Investigation of Selective Etch for CdTe, CdS, and GaAs	229
8.4	Development of Large Grain CdTe/CdS and Single Crystal CdTe Thin Film Structures by Selective Etching	231
	8.4.1 Two-step Transfer Process	231
	8.4.2 One-step Transfer Process	232
8.5	Investigation of the Quality of the ELO Surface and Structures	237
8.6	Cu Migration in the CdTe Solar Cells with Varying Degree of CdTe Crystallinity	243
8.7	Conclusion	246
IX CONCLUSIONS AND FUTURE DIRECTIONS		249
APPENDIX PUBLICATIONS		261
REFERENCES		263

LIST OF TABLES

Table 1.1	Electrical and physical properties of CdTe at 300 K	5
Table 3.1	Standard X-ray diffraction parameters for power CdTe and CdS	103
Table 4.1	Solar cell data for the CdTe/CdS cells grown with different CdS thicknesses	126
Table 4.2	Photocurrent losses before and after AR coating which were calculated from (a) simulated reflectivity spectrum, (b) measured reflectivity of a practical cell	133
Table 5.1	Comparison of cell parameters from various investigators	138
Table 5.2	The flow rates and temperatures of the Te and Cd sources for various Te/Cd mole ratios used in this study	141
Table 5.3	Solar cell data for CdTe/CdS cells grown with different Te/Cd mole ratios in MOCVD growth ambient	152
Table 5.4	J-V-T parameters (J_0 and A) for MOCVD-grown CdTe/CdS cells, extracted from fit to Equation (3.12)	158
Table 5.5	Photoluminescence lifetime in cells processed with and without CdCl_2 treatment and with different Te/Cd mole ratios in MOCVD ambient	165
Table 6.1	Cell data with varying CdCl_2 concentration	177
Table 6.2	Cell results for different post-growth treatment conditions	181
Table 7.1	CdTe solar cell parameters with different Au/Cu contact	201
Table 7.2	J-V-T parameters for CdTe cells with different Cu thicknesses in the contact	215
Table 7.3	CdTe solar cell parameters with different Au/Cu deposition rates	218

LIST OF FIGURES

Figure 1.1	Theoretical single junction solar cell efficiency versus semiconductor bandgap for ideal homojunction cells	6
Figure 1.2	Optical absorption coefficients of various semiconductors as a function of photon energy	7
Figure 1.3	The typical structures of the (a) front wall, (b) back wall CdTe/CdS heterojunction thin film solar cells	10
Figure 2.1	Equivalent circuit for a solar cell under illumination with one diode transport mechanism operating: (a) ideal solar cell and (b) R_s and R_{sh} included	22
Figure 2.2	I-V characteristics of a solar cell: (a) dark and illuminated, (b) the maximum power rectangle, and (c) the effect of a high R_s and low R_{sh} on the fill factor	24
Figure 2.3	Ideal energy band diagram for CdTe/CdS system (a) before and (b) after the junction are formed	27
Figure 2.4	Schematic of diode current transport by (a) injection/diffusion, (b) depletion region recombination, and (c) interface recombination in a forward biased CdTe/CdS heterojunction	32
Figure 2.5	Schematic of diode current transport by (a) single step tunneling and (b) multi-step tunneling via interface and depletion region states	39
Figure 2.6	Schematic of diode current transport via thermally-assisted tunneling from the valence band into interface states followed by fast interface recombination	42
Figure 2.7	(a) DLTS spectrum of a CdTe/CdS cell annealed with $CdCl_2$, (b) measured V_{oc} and J_{sc} as a function of trap concentration as determined from the DLTS data	54

List of Figures

Figure 2.8	Schematic of a metal/semiconductor band diagram for (a) depletion, (b) neutral, and (c) accumulation	57
Figure 2.9	Specific contact resistance ρ_c of a CdTe Schottky barrier as a function of the barrier ϕ_B	59
Figure 2.10	Specific contact resistance of a CdTe Schottky barrier as a function of the doping N of the base material	60
Figure 3.1	Schematic of CdS solution growth process	73
Figure 3.2	Four regimes in the MOCVD reactor, including the boundary layer over the substrate surface	78
Figure 3.3	Schematic diagram of a SEM system	86
Figure 3.4	(a) Auger Electron Generation Process and (b) Energy distribution of scattering electrons from a solid surface	89
Figure 3.5	A typical differentiated Auger spectrum for (a) Cd and (b) Te element	92
Figure 3.6	Bragg Diffraction Schematic diagram	99
Figure 3.7	The collection intensity depend on the area of the band, which varies with different θ_B	102
Figure 3.8	(a) An Optronics Laboratory system for QE measurements. (b) Circuit diagram for light- and bias-dependent QE measurement	111
Figure 3.9	Schematic diagram of a integrating sphere for reflectance measurements	113
Figure 4.1	Photocurrent loss in CdTe solar cells due to the absorption in CdS window layer and the reflection with varying CdS thicknesses	123
Figure 4.2	Measured reflectance for CdTe/CdS solar cells with different	

List of Figures

	CdS thicknesses	124
Figure 4.3	Photocurrent loss in CdTe solar cells due to the reflection with varying SnO ₂ thicknesses	129
Figure 4.4	Calculated reflectance for different AR coatings on glass	131
Figure 4.5	Measured reflectance for CdTe/CdS solar cells with and without MgF ₂ AR coating on glass	134
Figure 5.1	Auger depth profiles at and near CdTe/CdS interface for cells grown with different Te/Cd mole ratios in MOCVD ambient	143
Figure 5.2	QE measurements of cells under different growth and treatment conditions with illumination from glass and Au/Cu sides	145
Figure 5.3	PL spectra of CdTe films under (a) Te/Cd~0.02 growth ambient, (b) Te/Cd~6.0 growth ambient, (c) Te/Cd~0.02 growth ambient after CdCl ₂ treatment	148
Figure 5.4	J _{sc} and V _{oc} of MOCVD CdTe/CdS solar cells grown with different Te/Cd mole ratios in MOCVD ambient	150
Figure 5.5	Light-biased quantum efficiency at zero and 0.6 V forward bias for cells grown with different Te/Cd mole ratios in MOCVD ambient	154
Figure 5.6	Change in quantum efficiency with 0, 0.3 and 0.6 volts forward bias for cells grown in different Te/Cd mole ratios	156
Figure 5.7	Plot of C-factor vs 1000/T (T/IR model), supporting contention that Cd-rich cells exhibit higher degree of tunneling	160
Figure 5.8	The tunneling probability decreases because the enhanced interdiffusion enlarges the energy barrier thickness for tunneling	162
Figure 5.9	Plot of ln(J ₀ T ^{-2.5}) vs 1000/T for CdTe/CdS cells grown in Te-	

List of Figures

	rich ambient (Te/Cd~6) after CdCl ₂ post-growth treatment	163
Figure 6.1	(a) AET ADDAX Rapid Thermal Processor, (b) Typical annealing profile generated by RTP control	172
Figure 6.2	SEM Microstructure of CdTe (a) as-grown film, (b) after CdCl ₂ treatment	174
Figure 6.3	PL spectra for CdTe treated with different CdCl ₂ concentration, (a) saturated, (b) 0.5, (c) 0.25, (d) 0.75. The corresponding V _{oc} are also shown	179
Figure 6.4	SIMS data shows a relatively low Cl content in the RTP CdTe films	184
Figure 6.5	EBIC signals in CdTe films, (a) as-grown CdTe, (b) CdCl ₂ furnace anneal at 400°C 30 min, (c) RTP anneal at 700°C 5 sec.(Signal level not same)	185
Figure 6.6	SEM Microstructure of CdTe (a) as-grown film, (b) after furnace 400°C, 30min, (c) after RTP 550°C, 5 sec, (d) after RTP 700°C, 5 sec	187
Figure 6.7	XRD scan on the CdTe/CdS films with CdTe layer grown at Te/Cd ratio of 0.02, 0.1 and 6	189
Figure 6.8	XRD scan on the CdTe/CdS films before annealing and after different annealing conditions	191
Figure 6.9	XRD scan on the CdTe/CdS films with RTP or furnace anneal	193
Figure 7.1	SIMS record of Cu ⁺ ions through the CdTe layer for a Au/Cu/CdTe/CdS cell structure	203
Figure 7.2	The Cd/Te ratio of SIMS signals near the Cu/CdTe interface	205
Figure 7.3	The acceptor concentration in the CdTe layer by C-V measurement with different metal contact on CdTe solar cells	207

List of Figures

Figure 7.4	R_s and R_{sh} of the CdTe solar cells with different Cu thickness in the Au/Cu contact	210
Figure 7.5	CdTe solar cell efficiency with different Cu thickness in the Au/Cu contact	212
Figure 7.6	Cu depth profiles from SIMS measurement on the cells with 50 Å and 150 Å Cu contact	213
Figure 7.7	Plot of $\ln(J_0 T^{-2.5})$ vs $1000/T$ for CdTe/CdS cells with 50 Å, 100 Å, and 150 Å Cu contact	216
Figure 7.8	The acceptor concentration in the CdTe layer by C-V measurement with different Au/Cu deposition rate for contact on CdTe solar cells	219
Figure 7.9	The Cd/Te ratio of SIMS signals near the Cu/CdTe interface for the cells with different Au/Cu deposition rate on the contact	221
Figure 8.1	XRD patterns for the CdTe in the CdTe/CdS/SnO ₂ /glass(a), and in the CdTe/CdS/GaAs(b). DCRC pattern for the CdTe in the CdTe/GaAs(c)	226
Figure 8.2	SEM measurements on the CdTe layers for (a) CdTe/CdS/SnO ₂ /glass, (b) CdTe/CdS/GaAs, and (c) CdTe/GaAs structures	228
Figure 8.3	Large grain thin-film CdTe/CdS solar cell fabrication procedures with two-step film transfer	233
Figure 8.4	Large grain thin-film CdTe/CdS solar cell fabrication procedures with one-step film transfer	234
Figure 8.5	Large grain thin-film CdTe/CdS solar cell fabrication procedures with a metal bonding technique	236
Figure 8.6	Rocking curves for the 400 CdTe on CdS/GaAs substrate before and after the separation from GaAs substrate	238

List of Figures

Figure 8.7	Rocking curves for the 400 CdTe near the CdTe/air interface and near the CdTe/GaAs interface	240
Figure 8.8	PL spectrum of CdTe near the CdTe/air interface before lift-off and near the CdTe/GaAs interface after lift-off	242
Figure 8.9	Comparison of Cu SIMS profiles in the CdTe layers with different degrees of crystallinity	244
Figure 8.10	SIMS record of Ga, S, and Cd ions near the CdTe/CdS region	247
Figure 9.1	The increase in the CdTe cell efficiency by understanding the loss mechanisms in the cell structure in this study	256
Figure 9.2	A 11.9% efficient CdTe solar cell was accomplished by the fundamental understanding of loss mechanisms	257
Figure 9.3	Future guidelines to raise the cell efficiency beyond 12%	259

SUMMARY

The objective of this research was to bring the polycrystalline CdTe cell efficiency a step closer to the practically achievable efficiency of 18% through fundamental understanding of defects and loss mechanisms, the role of chemical and heat treatments, and investigation of new process techniques. This objective was accomplished by a combination of in-depth characterization, modeling, materials growth, device fabrication, and carrier transport analysis of Au/Cu/CdTe/CdS/SnO₂/glass front wall heterojunction solar cells. Attempts were made to understand the loss mechanism(s) in each layer and interface by a step-by-step investigation of this multilayer cell structure.

The first step was to understand, quantify, and reduce the reflectance and photocurrent loss in polycrystalline CdTe solar cells. Model calculations were performed to determine the optimum thicknesses of CdS and SnO₂ films along with appropriate refractive index and thickness of antireflection (AR) coating on glass that can minimize the reflectance and enhance the performance of CdTe/CdS/SnO₂/glass solar cells. Photocurrent loss resulting from absorption in the CdS film was calculated as a function of CdS thickness. It was found that the current loss from reflectance and absorption is quite sensitive to the CdS film thickness below 1500 Å. Model calculations also showed that reducing the CdS thickness from 1500 Å to 600 Å can increase the short-circuit current density (J_{sc}) of the cell by 3 mA/cm² because of reduced reflectance and

absorption. It was found that the decrease in the CdS thickness below 600 Å increases the reflectance loss but still results in higher J_{sc} , because the current gain resulting from reduced absorption in thin CdS offsets the current loss resulting from higher reflectance. Practical optimum thickness is 600 Å, provided the CdS film can be grown without pin holes at this thickness. Model calculations showed that photocurrent loss from reflectance is not sensitive to SnO_2 thickness above 4000 Å. However, because of the competition between the resistive and absorption losses, SnO_2 thickness in the range of 6000-10000 Å is recommended. Finally, the practical optimum thickness and refractive index for a single layer AR coating on glass was found to be 1100 Å and 1.38, respectively, which provided an additional increase of 0.7 mA/cm² in J_{sc} .

The second phase of this research involved the investigation of defects and loss mechanisms associated with the CdTe layer and the CdTe/CdS interface. Attempts were made to investigate the role of native defects in CdTe on the cell performance. It was shown for the first time that native defect concentration in the polycrystalline CdTe films can be altered by changing the MOCVD growth ambient. For example, Films grown in highly Cd-rich ambient produced n-type CdTe, while the films grown in highly Te-rich ambient were p-type. This is because Cd vacancies act as acceptors, while the Te vacancies give rise to donors. CdTe cells were fabricated by depositing CdTe films on CdS/ SnO_2 /glass substrates in different metalorganic chemical vapor deposition (MOCVD) growth ambients with varying Te/Cd mole ratio in the range of 0.02 to 15 in order to alter

native defect concentration in the CdTe film, which also had significant effects on the CdTe cell parameters. The short-circuit current (J_{sc}) showed a minimum at the Te/Cd ratio of 0.1. The open-circuit voltage V_{oc} increased monotonically from Cd-rich ambient to te-rich ambient and then leveled off after Te/Cd ratio of 6. These trends resulted in highest cell efficiency (~12%) on the Te-rich CdTe films. Since V_{oc} is quite sensitive to interface quality, the trend in V_{oc} suggests better interface quality in the Te-rich cells. In order to verify this hypothesis, Auger electron spectroscopy (AES) and carrier transport measurements were performed. AES measurements revealed a high degree of atomic interdiffusion at the CdS/CdTe interface when the CdTe films were grown in the Te-rich conditions. It was found that the current transport in the cells grown in the Cd-rich ambient was controlled by the tunneling/interface recombination mechanism, but the depletion region recombination became dominant in the Te-rich cells. These observations suggest that the enhanced interdiffusion reduces interface states due to stress reduction or gradual transition from CdS to CdTe. The hypothesis of reduced defect density in the CdTe cells grown in the Te-rich conditions was further supported by the high effective carrier lifetime, measured by time-resolved photoluminescence and the reduced sensitivity of quantum efficiency to forward/light bias.

The third major objective of this research was to investigate the effect of chemical and heat treatments on CdTe films and cells. To accomplish this task, the $CdCl_2$ concentration and annealing conditions were varied. It was found that $CdCl_2$ treatment

of CdTe films tends to densify the film, changes the surface morphology, makes the grains flat and less faceted, and serves as a flux to recrystallize the CdTe structure. This reduces the effective grain boundary surface area per unit volume (S_{v1}) or decreases the grain boundary conduits for impurity or metal migration, which results in enhanced cell performance. Light I-V and PL measurements revealed optimum CdCl_2 concentration in the range of 50% to 75% for our MOCVD cells, because higher CdCl_2 concentration gives rise to higher Cl-related defect density and degrades the cell performance. Therefore, even though CdCl_2 treatment is essential for high efficiency CdTe cells, it could place an upper limit on the practically achievable cell efficiency. Rapid thermal processing was performed on CdS/CdTe structure to achieve grain regrowth in the CdTe films with lower CdCl_2 concentrations, or even without any CdCl_2 treatment. It was found that RTP conditions produced significant changes in the CdTe cell parameters. A cell with 10.7% efficiency was achieved using the 700°C, 5 second RTP without any CdCl_2 treatment. SEM and EBIC measurements showed that the microstructure and the diffusion length in the CdTe after the RTP were similar to the CdTe cell with conventional CdCl_2 treatment, which involves 400°C/30min furnace anneal. However, reduced interdiffusion at the CdTe/CdS interface in the RTP cells was probably responsible for the lower RTP cell efficiency compared with the CdCl_2 treated and furnace annealed cells.

The fourth major objective of the research was to achieve a better and reliable

contact to CdTe solar cells by improving the fundamental understanding of the effects of Cu on cell efficiency. CdTe solar cells were fabricated by depositing Au/Cu contacts with varying thicknesses and deposition conditions on the polycrystalline CdTe/CdS/SnO₂/glass structures. It was found that Cu plays a dual role on the cell performance; on one hand it helps the formation of better ohmic contact and increases the acceptor doping concentration, but on the other hand, excess Cu diffuses all the way to the CdTe/CdS interface to form recombination centers and shunt paths to degrade the cell performance. Both SIMS and C-V measurements confirmed the incorporation of Cu into the bulk of the CdTe films. Cd out-diffusion toward the surface of the CdTe was also observed during the Au/Cu deposition. It was found that the thickness of Cu plays a critical role in dictating the CdTe solar cell performance because both series and shunt resistances decrease with the increase in Cu thickness. Carrier transport analysis showed that the depletion region recombination dominates the current transport in the CdTe solar cells with Au/Cu contact, regardless of the amount of Cu incorporation in the bulk and near the CdTe/CdS interface. SIMS measurement showed that higher Au/Cu deposition rates resulted in a greater pile-up of Cd near the CdTe surface, generating more Cd vacant sites below the surface and causing a reduction in the cell performance.

The final phase of the research involved the investigation of the effect of crystallinity and grain boundaries on Cu incorporation in the CdTe films, including the fabrication of CdTe solar cells with larger CdTe grain size. Three different CdTe

structures, CdTe/CdS/SnO₂/glass, CdTe/CdS/GaAs, and CdTe/GaAs, were prepared to achieve CdTe films with different degrees of crystallinity and grain size. The CdTe/CdS/GaAs structure gave large CdTe grains (~10 μm) which was used to fabricate a large grain polycrystalline CdTe thin film solar cell structure for the first time in this study by a combination of selective etching of the GaAs substrate and the film transfer onto a glass substrate. X-ray diffraction measurements on the CdTe films, before and after the transfer, were used to assess lattice mismatch-induced changes in the CdTe lattice constant near the CdTe/GaAs interface. SIMS measurement showed that poor crystallinity and smaller grain size (~2 μm) of the CdTe film in the conventional polycrystalline CdTe/CdS/SnO₂/glass structure promotes Cu diffusion from the contact and decreases cell performance. In the large grain (~10 μm) CdTe film, Cu concentration was about a factor of 2 lower than the small grain CdTe film, while in the single crystal CdTe film, Cu was virtually undetectable. Therefore, we concluded that grain boundaries are the main conduits for Cu migration, and larger CdTe grain size or an alternate method of contact formation needs to be developed to mitigate the adverse effect of Cu and improve the CdTe cell performance.

Through a combination of fundamental understanding of the loss mechanisms associated with different layers and interfaces in the cell structure and process optimization, we were able to increase the CdTe cell efficiency systematically. Solar cells fabricated without any material and process optimization gave an efficiency of less than

2%. After the optimized CdCl_2 treatment and 400°C furnace anneal, which reduces grain boundary area per unit volume and makes CdTe more p-type, the cell efficiency went up to 6.6%. Solar cell efficiency increased to 9.3% when the CdTe film was grown under the Te-rich MOCVD growth ambient, which reduced the defect density in the CdTe and at the CdTe/CdS interface by promoting interdiffusion. Contact optimization resulted in additional increase in cell efficiency. A combination of optimized Au/Cu contact thickness and deposition rate, Te-rich MOCVD growth of CdTe, and optimized CdCl_2 treatment and furnace anneal, resulted in approximately 12% efficient CdTe solar cells with $V_{oc}=781.4\text{ mV}$, $J_{sc}=23.26\text{ mA/cm}^2$ and fill factor=0.657. This represents the highest efficiency achieved for the MOCVD grown CdTe solar cells to date. Finally, based on the fundamental understanding of defects and loss mechanisms, guidelines were provided for raising the CdTe cell efficiency from 12% to ~18% by a combination of thin CdS, large grain CdTe, and reduced Cu migration and bulk defects.

CHAPTER I

INTRODUCTION

1.1 Introduction and Statement of Problem

The standard of living in modern society depends upon the quality and availability of energy. The demand for energy has been increasing steadily and rapidly over the years, along with the depletion of current energy sources. Among the various alternatives available today, solar energy is particularly attractive because it is not only free but is essentially unlimited and not localized in any part of the world. Photovoltaics (PV) is an ideal candidate to tap this enormous resource because solar cells can convert sunlight directly into electricity without any undesirable impact on the environment. Low cost and high efficiency are the keys for large-scale applicability of PV systems. Unfortunately, the cost of solar cell modules is about a factor of four too high to be attractive for very large-scale utility application in the United States. However, given the fact that in the 1970s this factor was about 100, there is reason for optimism that PV will become a cost-effective source of electrical energy in the near future. Photovoltaic modules today cost about \$4/Watt, which can produce electricity at a rate of about \$0.25/kWhr. A factor of 2 in cost reduction will make PV attractive for utility peak-power generation, and a

reduction by a factor of 3 or 4 would make it extremely competitive with conventional energy sources, such as fossil fuels, for base load utility application.

In order to make PV more cost effective, we need to increase the efficiency of solar cells and employ inexpensive abundant materials and low-cost processes for large-scale production. Indirect bandgap materials, such as crystalline Si, require very large thickness ($> 300\mu\text{m}$) in order to absorb the solar spectrum, while a thickness of less than $5\mu\text{m}$ is needed for direct bandgap semiconductors, such as CdTe and CuInSe_2 , which are being utilized for thin-film solar cells [1,2]. Besides the reduced thickness and cost of materials, other advantages of thin-film solar cells include the availability of several low-cost, high-throughput, scalable fabrication techniques and possible utilization of inexpensive substrates such as glass. In spite of the high potential for low-cost terrestrial PV, thin-film solar cell efficiencies are not quite as high as crystalline Si cells today. Therefore, a fundamental understanding of efficiency limiting defects and mechanisms in thin-film cells has become an area of active investigation.

Among the various thin-film candidates, cadmium telluride (CdTe) is one of the most promising for cost-effective photovoltaic conversion of solar energy because of the optimal bandgap (1.45 eV) and large absorption coefficient. CdTe solar cell structure consists of glass/ SnO_2 /CdS/CdTe/contact, where glass serves as substrate, conductive SnO_2 as anti-reflection (AR) coating and front contact, and widegap (2.4 eV) CdS as n^+ window

layer to form an n^+ -p heterojunction device, which allows most of the solar spectrum to absorb in the p-type CdTe. There has been a steady increase in the efficiency of these cells in the past few years, with the maximum reported efficiency of 15.8% to date [3]. However, most of the CdTe cells made by different groups are still within 10-12% efficiency range [4], while the practically achievable efficiency is in the range of 18-20%. In order to achieve high efficiencies reproducibly and approach the estimated potential efficiency of $\geq 18\%$, much more basic research on defects, loss mechanisms, and process optimization is required. The efficiency limiting defects and mechanisms in CdTe/CdS devices have not been revealed, understood, and quantified to any degree of satisfaction. This makes it hard to increase the CdTe cell efficiency systematically and intelligently because it is not clear which layer, interface, or process step should be modified to improve reproducibility and cell performance. The above facts present considerable opportunity and challenge to achieve high-efficiency polycrystalline CdTe solar cells. Therefore, the overall goal of this research is to bring the polycrystalline CdTe cell efficiency a step closer to the projected potential value through a fundamental understanding of defects and loss mechanisms, the role of chemical and heat treatments, and investigation of new process techniques to achieve cost-effective high-efficiency CdTe cells.

1.2 Historical Survey of CdTe Solar Cells

1.2.1 CdTe Material : Advantages and Problems

Modern interest in CdTe dates back to 1947, when single crystal CdTe was grown by Frerichs [5]. Single crystal CdTe is widely used today for nuclear radiation detectors, electro-optical modulators, and infrared windows [6]. Table 1.1 summarizes the electrical and physical properties of CdTe. Its potential as a solar cell material was recognized in 1959 by Rappaport [7], who predicted the optimum bandgap of 1.5 eV for a single junction solar cell (Figure 1.1). Besides the optimum bandgap of 1.5 eV, CdTe is also a direct bandgap semiconductor with a high absorption coefficient ($> 1 \times 10^4 \text{ cm}^{-1}$) for photons above the bandgap energies (Figure 1.2) [8]. Therefore, 1-2 μm thick CdTe is sufficient to absorb more than 90% of solar spectrum. These features make CdTe a very attractive candidate for cost-effective thin-film solar cells.

Cadmium telluride is among the few large bandgap II-VI semiconductors that can be made p or n type with considerable ease. Based on the defect models, an excess of Cd produces n-type CdTe and an excess of Te results in p-type doping [9]. The solubility of Cd and Te in the CdTe has been found to be in the range of 0.01-1 atomic percent with electrically active species on the order of 10^{-3} atomic percent only. Conductivity can also be altered by the presence of impurities. For example, highly conductive n-type CdTe can be formed by In, Ga[10], and Cl[11] doping. The impurities utilized for p-type

Table 1.1 Electrical and physical properties of CdTe at 300 K.

Parameters	CdTe
Crystal structure	Zincblende
Density	6.2 g/cm ³
Melting point	1092°C
Lattice constant	6.481 Å
Bandgap (E_g)	1.44 eV
Electron affinity (χ)	4.3 eV
Dielectric constant (ϵ)	9.4
Electron mobility	1050 (cm ² V ⁻¹ s ⁻¹)
Hole mobility	80 (cm ² V ⁻¹ s ⁻¹)
Electron effective mass	0.1 m_0
Hole effective mass	0.8 m_0
N_c	8.0×10^{17} (cm ⁻³)
N_v	1.8×10^{19} (cm ⁻³)
N_i	3.2×10^6 (cm ⁻³)

Figure 1.1 Theoretical single junction solar cell efficiency versus semiconductor bandgap for ideal homojunction cells (after ref. 8).

Figure 1.2 Optical absorption coefficients of various semiconductors as a function of photon energy (after ref. 8).

dopant are Li, Na, Cu, Ag, As[12], N, P, Sb[13], Cs[14], and O[15]. However, high-conductivity p^+ CdTe is generally hard to realize in a single crystal form and even harder in the form of polycrystalline film [16].

The ohmic contact to CdTe is greatly affected by its conductivity type. It is much easier to form good ohmic contact on n-type films than on the p-type ones. Because low-resistivity p^+ material is difficult to achieve, it is hard to form low-loss tunneling metal/semiconductor contacts. The electron affinity of CdTe is about 4.3-4.5 eV [17] and for n-type CdTe, the work function is about the same. However, for p-type material, the work function is approximately equal to the sum of electron affinity and energy gap, or about 5.8 eV. Thus, ohmic contact to p-type CdTe requires a metal with work function in excess of 5.8 eV, which is rarely found. This presents a real challenge for achieving high efficiency CdTe cells because high contact resistance lowers J_{sc} , fill factor and cell efficiency.

1.2.2 CdTe Solar Cell Structures

Since both n- and p-type CdTe materials are available, homojunction CdTe solar cells with efficiency of 10.7% have been fabricated [18]. However, it is difficult to achieve higher-efficiency CdTe homojunction cells because of the (a) short optical absorption length in the CdTe, (b) difficulty of forming a shallow junction ($< 0.1 \mu\text{m}$)

with a high conductivity surface layer, and (c) high surface recombination velocity [19]. Therefore, a heterojunction configuration is generally preferred for thin-film CdTe solar cells.

For a heterojunction CdTe solar cell, a transparent conducting semiconductor is used as the heterojunction partner or "window" layer. This window material not only needs to have a large bandgap to allow the solar spectrum to be absorbed in the CdTe, but should also form a good-quality junction with the CdTe. Since there are limited choices for p-type widegap window materials, heterojunctions with n-type CdTe are rarely investigated. However, a number of n-type wide-bandgap materials like CdS, ITO[20], SnO₂[21], ZnO[22], and ZnSe[23] can be used with p-type CdTe to form heterojunctions. The most common window layer utilized with p-type CdTe is cadmium sulfide (CdS) because of its good optical transparency (a bandgap of 2.4 eV or 0.9 eV higher than CdTe [24]), ability to lower the CdTe surface recombination velocity, reasonable quality CdTe/CdS interface, availability of low-cost large-scale growth techniques, and the ease of depositing low-resistivity films. Both "front wall" (CdTe deposited on the window material) and "back wall" CdTe/CdS heterojunction solar cell structures (Figure 1.3) have been fabricated. The maximum reported efficiency for the CdTe back wall solar cells to date is 9.16% [25], while the CdTe solar cell efficiency of 15.8% has been achieved for the front wall structure. All the CdTe cells with efficiency over 10% have a front wall

Figure 1.3 The typical structures of the (a) front wall, (b) back wall CdTe/CdS heterojunction thin film solar cells.

structure consisting of a glass substrate, transparent conducting oxide (usually SnO_2) for front contact, CdS window layer, CdTe absorber, and back contact (Figure 1.3). The success of the front wall structure is attributed to the fact that the p-CdTe contact is formed last and, therefore, can be optimized at the end of the cell fabrication process. In the back wall case, p-CdTe is deposited on the contact material, which results in interdiffusion and chemical reactions between the metal and the CdTe and degrading cell performance. This provided the motivation to use the front wall structure in this research. The rest of the discussion in this section will focus on the front wall CdTe solar cells.

1.2.3 CdTe Deposition Techniques for Thin Film Solar Cells

Thin-film polycrystalline CdTe/CdS solar cells with front wall structures have been produced at many organizations using various CdTe deposition techniques, including electrodeposition, screen printing, spray pyrolysis, atomic layer epitaxy (ALE), MOCVD, and close-spaced sublimation (CSS). These techniques are briefly discussed below.

A. Electrodeposition

The electrodeposition of CdTe has become a promising method for producing efficient thin-film solar cells. This technique is relatively simple in principle. CdTe films of well-defined composition are deposited cathodically from an acid solution of a cadmium salt (such as CdSO_4) and TeO_2 (HTeO_2^+ being the principal species in solution)

according to the following reaction:

A CdS and TCS (transparent conducting semiconductor) coated glass substrate is used as the cathode. Both reactions take place simultaneously at cathode potentials (versus the standard calomel electrode) between -0.2V and -0.65V, just below the deposition potential of metallic Cd. The concentration of HTeO_2^+ in solution, limited by the solubility of TeO_2 , is small and is replenished by switching a Te anode into the circuit. The important process parameters are the stirring rate, the concentration of HTeO_2^+ , and the temperature of the solution. Since the deposition rate of CdTe is limited by the concentration of HTeO_2^+ in the cathode region, the deposition rate is relatively slow at $1\text{-}2\ \mu\text{m h}^{-1}$.

The electrodeposited CdTe films at room temperature are generally amorphous, but those deposited at 85-90°C have a grain size of 500-1000 Å. The grain size can be increased to about 0.5 μm or larger by heat treatment in air or in an oxygen-containing atmosphere, particularly in the presence of CdCl_2 as a flux. It has been shown that the as-deposited n-type films are converted to p-type by this treatment.

The use of electrodeposited CdTe films for thin-film solar cell fabrication has been

under investigation for over 15 years. Continued progress has led to the development of heterojunction solar cells with efficiencies in excess of 10%. Using CdS, pyrolytically deposited on SnO₂-coated sodalime glass as the cathode for the electrodeposition of CdTe, small-area (1 cm²) thin-film solar cells with a conversion efficiency of 11.2% have been produced [26]. Solution-grown CdS films have also been used in conjunction with electrodeposited CdTe films for the preparation of thin-film CdTe solar cells [27].

B. Screen printing

The screen-printing technique utilizes the application of a paste of electronic material through a screen onto a substrate, followed by heat treatment. It is a low-cost process and has been used successfully for the fabrication of large-area, thin-film CdS/CdTe solar cells. In this process, a CdS film is deposited on a borosilicate substrate by screen printing of a paste of CdS, CdCl₂ (flux) and propylene glycol (binder), followed by drying and sintering in a nitrogen atmosphere at about 700°C in a belt furnace. During the sintering process, grain growth of CdS occurs via recrystallization from the flux, and the resulting film, usually 20-30 μm thick, has a grain size of 20-30 μm and a resistivity of 0.2-0.5 Ω-cm. The paste for the screen printing of CdTe films consists of an equimolar mixture of Cd and Te (or CdTe) with CdCl₂ as flux and propylene glycol as binder. This paste is applied to screen-printed CdS/glass structure and then sintered at 590-620°C; CdTe is formed by the reaction between Cd and Te, with subsequent grain

growth. Furthermore, the interface reaction results in the formation of CdS-CdTe solid solutions of $\text{CdS}_x\text{Te}_{1-x}$, which reduces the effects of mismatch between CdS and CdTe to some extent. The important parameters of the screen-printing process are the screen size, composition of the pastes, sintering time and temperature. The short-wavelength response of screen-printed CdS/CdTe solar cells is poor because of the large thickness of CdS, which absorbs essentially all the solar radiation below the wavelength of less than 500 nm, whereas the photoresponse cut-off wavelength is extended beyond 850 nm, owing to the interface reaction.

Conversion efficiencies of screen-printed CdS/CdTe solar cells have been reported to be 12.5% [28], 11.3% [29], and 8.1% [30] for devices of 0.3 cm², 1 cm² and 1200 cm², respectively.

C. Spraying

Early work on the sprayed CdTe/CdS solar cells was based on the spray pyrolysis technique, which yielded 4% efficient devices. In this approach, an aqueous solution of CdCl_2 and thiourea was first sprayed onto a heated (300-350°C) ITO/glass substrate, forming a thin CdS layer. A CdTe film was then grown over the CdS layer by spraying a solution containing Cd and Te species.

Fabrication of high-efficiency CdTe/CdS devices by the spraying technique involves post deposition heat treatments of the CdS and the CdTe films for grain growth

[31]. CdS and CdTe films are 6 μm and 3 μm thick, respectively, and a $\text{CdTe}_x\text{S}_{1-x}$ solid solution is formed at the CdTe/CdS interface as a result of the above-mentioned annealing steps. Recently, a sprayed CdTe/CdS cell with a metal/carbon/CdTe/CdS/ SnO_2 /glass structure was measured to be 12.3% efficient [32].

D. Atomic layer epitaxy (ALE)

Atomic layer epitaxy (ALE), developed for the controlled epitaxial growth of compound semiconductors in the early 1980s, has been applied to the deposition of CdS and CdTe films and CdS/CdTe solar cells. In this process, Cd and S vapors are introduced alternately onto the surface of heated SnO_2 /glass substrates to form a CdS film, followed by the deposition of a CdTe film from Cd and Te vapors.

This technique offers the advantages of the in-situ substrate cleaning and the deposition of low resistivity (200 $\Omega\text{-cm}$) CdTe films. However, reasonably high growth rate (0.3-0.4 $\mu\text{m}/\text{min}$) can only be obtained at high temperatures (550°C). In addition, the deposited films consist of large grains, and thicknesses of 15-20 μm are required to eliminate pinholes, resulting in long deposition times where the reaction of CdTe with the CdS substrate could be a problem.

E. Metal organic chemical vapor deposition (MOCVD)

Metal organic chemical vapor deposition (MOCVD), widely used for the epitaxial growth of compound semiconductors, has been applied only recently to the deposition of

polycrystalline CdTe films. CdTe films can be deposited at rates of up to $4 \mu\text{m h}^{-1}$ on CdS/SnO₂/glass substrates at 350-400°C by the reaction between dimethylcadmium (DMCd) and diisopropyltelluride (DIPTe) in a hydrogen atmosphere. The deposited CdTe film is polycrystalline, consisting of densely packed columnar grains with an average grain size of about 1-3 μm . The conductivity type of CdTe films is determined by the DMCd/DIPTe molar ratio in the reaction mixture. The near-stoichiometric films can be p-type because of the Cd vacancies or n-type because of the Te vacancies. Thin-film CdS/CdTe solar cells have been prepared from MOCVD of CdTe films on solution or MOCVD grown CdS films [33,34].

F. Close-spaced sublimation

The close-spaced sublimation (CSS) technique, developed for the epitaxial growth of III-V compounds in the 1960s, has been applied successfully to the deposition of CdTe films and solar cells. It is based on the reversible dissociation of CdTe at high temperatures:

The CdTe source and the substrate are separated by a small distance (0.1-0.2 cm) in a controlled atmosphere. The source material is maintained at a higher temperature (650-700°C) than the substrate (550-600°C). The CdTe source dissociates into its elements, which recombine on the surface of the substrate to deposit a CdTe film. Since the spacing between the source and the substrate is less than a few percent of the dimension

of the substrate, the material transport conditions are mainly independent of conditions elsewhere in the system. The CSS process is essentially diffusion limited, and the close spacing of the source and substrate provides direct transport of each element from the source to the substrate.

The CSS technique has resulted in the highest efficiencies (15.8%) CdTe/CdS thin-film solar cells to date [3]. In-situ heat treatment of the CdS films at 400°C in a hydrogen atmosphere prior to the deposition of CdTe greatly enhances the junction characteristics by reducing the number of interface states.

1.3 Overview of the Report

In Chapter II, heterojunction device physics, current transport mechanisms, theory and operating principles of solar cell, along with the CdTe/CdS cell efficiency limiting defects and mechanisms, are reviewed. Chapter III discusses the experimental procedures and the main characterization and analysis techniques used in this research. Chapters IV to VIII present a systematic step-by-step investigation of glass/SnO₂/CdS/CdTe/Cu/Au cell structure to understand the efficiency limiting defects and loss mechanisms in the CdTe/CdS solar cells. Chapter IV analyzes the photocurrent loss from reflectance and absorption in the CdTe cells. Chapter V investigates the impact of MOCVD growth ambient on carrier transport mechanism, defects, and performance of CdTe/CdS solar

cells. Chapter VI studies the effects of CdCl_2 treatment and discusses the results of rapid thermal processing of CdTe solar cells. Chapter VII presents the effects of Cu on CdTe solar cells with Au/Cu contacts. Chapter VIII involves the development of a new process technique to fabricate single crystal CdTe thin-film solar cells and the investigation of the role of CdTe crystallinity on the Cu migration and CdTe cell performance. Finally, Chapter IX summarizes the major findings related to efficiency limiting defects and mechanisms in CdTe cells, along with the guidelines for improving reproducibility and cell efficiency.

CHAPTER II

TECHNICAL BACKGROUND, MOTIVATION, AND RESEARCH OBJECTIVES

2.1 Introduction

This chapter reviews the theoretical background necessary to investigate the material and device properties of CdTe/CdS heterojunction solar cells. The motivation and research objectives of this research are also described. First, a brief review of solar cell device physics is presented. Second, the theory and concept of heterojunction band diagrams are reviewed in order to understand and analyze CdTe/CdS heterojunction cells. Third, heterojunction current transport mechanisms are discussed since they will be utilized in determining the loss mechanisms in heterojunction solar cells. Fourth, the potential efficiency limiting defects and mechanisms in CdTe/CdS solar cells are discussed to lay the foundation for the work covered in this research. Finally, the specific objectives and tasks of this research are presented.

2.2 Solar Cell Device Physics

This section reviews the device physics pertaining to homojunction and heterojunction solar cells [1,2,3]. It is well known that without external voltage or light bias applied to a p-n junction, the diffusion and drift current within the junction are balanced and there is no net current flow. However, when a p-n junction is exposed to light with energy greater than the semiconductor bandgap energy (E_g), the equilibrium is disturbed, and measurable currents and voltages can be observed. Photons with energy less than E_g make no contribution to the junction voltage or current. Photons with energy higher than E_g generate excess electron-hole pairs (EHP) in both regions of the junction. Excess electrons generated in the p region within a diffusion length from the depletion region diffuse to the edge of the depletion region and are swept to the n-side by the electric field in the junction region. Similarly, excess holes generated in the n-region may diffuse to the depletion region and are swept to the p-side by the electric field.

In the case of homojunction cells, such as the Si or GaAs p-n structure, the active region consists of the p-type emitter, the depletion region on both sides of the homojunction, and the n-type base. In the case of heterojunction cells, such as the CdTe/CdS structure, the wide bandgap CdS window does not significantly contribute to minority carrier photogeneration, even though it is an active (emitter) part of the device, which forms the p-n junction with the absorber. To quantitatively describe the J-V

characteristics of an operating solar cell, the superposition principle is typically invoked, which is a good approximation for most homojunction cells. The result of superposition is that the photocurrent and the diode current are independent of each other and can be linearly added to describe the net J-V behavior of the cell under illumination[1]. The equivalent circuit for an ideal solar cell consists of a constant current source in parallel with the junction as shown in Figure 2.1a, where the current I_{ph} is the result of the optically generated carriers. However, for a practical solar cell, the ideal equivalent circuit is modified by the addition of a series resistance (R_s) from ohmic losses and a shunt resistance (R_{sh}) from leakage currents, as shown in Figure 2.1b. The resulting J-V relationship is given by:

$$J = J_o [\exp(\frac{q}{kT}(V_A - JR_s)) - 1] + \frac{V_A - JR_s}{R_{SH}} - J_{ph} . \quad (2.1)$$

While the superposition principle sufficiently describes homojunction cell characteristics, it usually does not reflect the behavior of heterojunction cells, such as CdTe/CdS structures. In these devices, the leakage current may be influenced by the presence of light and J_{ph} , which results in a more sensitive voltage dependent characteristics. This is because the occupancy or charge state of deep trapping centers at or near the heterointerface may be altered by illumination [1]. A change in charge density modifies the depletion layer width, the junction field distribution, and possibly the carrier transport

Figure 2.1 Equivalent circuit for a solar cell under illumination with one diode transport mechanism operating: (a) ideal solar cell and (b) R_s and R_{sh} included.

mechanisms. Such behavior has been identified in $\text{Cu}_2\text{S}/\text{CdS}$ heterojunction solar cells [4]. These effects not only decrease the collection efficiency as the bias voltage is applied, but also cause a cross-over in the light and dark I-V curves. The collection probability $h(V)$ of photon-generated carriers through the junction in the presence of interface recombination can be approximated by [5,6]

$$h(V) = \frac{\mu E_o}{\mu E_o + S_i}, \quad (2.2)$$

where μ is the electron mobility within the junction region, E_o is the electric field across the junction, and S_i is the interface recombination velocity. Since S_i is proportional to the interface defect density, higher defect density results in poor carrier collection and lower quantum efficiency (QE).

Figure 2.2 shows the dark and illuminated I-V characteristics of a solar cell. Under illumination, the dark characteristics are shifted into the fourth quadrant, where the I-V product is negative and power can be delivered to an external circuit. Furthermore, the cell can be operated at a bias point where the I-V product is maximum for the maximum power output. The maximum power is related to the open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}) by the fill factor (FF), given by equation:

$$FF = \frac{|I_m| V_m}{|I_{sc}| V_{oc}}, \quad (2.3)$$

Figure 2.2 I-V characteristics of a solar cell: (a) dark and illuminated, (b) the maximum power rectangle, and (c) the effect of a high R_s and low R_{sh} on the fill factor.

where I_m and V_m are defined in Figure 2.2b. A small shunt resistance has an effect on the slope of the illuminated I-V curve at the point crossing the $V=0$ axis; while a large series resistance affects the slope of I-V curve at the $I=0$ crossing point. The net result is a poor fill factor as shown in Figure 2.2c.

Finally, the conversion efficiency of a solar cell is given by:

$$Eff = \frac{|P_{max}|}{P_{in}} = \frac{|I_{sc}| V_{oc} FF}{P_{in}}, \quad (2.4)$$

where P_{in} is the incident power density. Note that under open circuit conditions and assuming $R_s = 0$ and $R_{sh} = \infty$, Equation (2.1) can be rearranged to give

$$V_{oc} = \left(\frac{kT}{q} \right) \ln \left[\left(\frac{J_{ph}}{J_o} \right) + 1 \right]. \quad (2.5)$$

Thus the V_{oc} depends on the diode leakage current, J_o , and J_{sc} . The maximum obtainable J_{sc} from a given material and device structure depends upon surface reflection and recombination of photogenerated carriers. The fill factor depends on all of these factors in addition to shunt and series resistance effects shown in Figure 2.2c. Notice that V_{oc} is also reduced by a small R_{sh} , and J_{sc} can be reduced by a large R_s . The material properties that dictate these loss mechanisms must be understood and controlled to maximize solar cell efficiency for a given material and device structure.

2.3 Heterojunction Theory

A heterojunction is a junction formed between two dissimilar semiconductors. When the two semiconductors have the same type of conductivity, the junction is called an isotype heterojunction. When the conductivity types are different, the junction is referred to as anisotype heterojunction [7]. Since we are interested in the p-CdTe/n-CdS devices in this research, the discussions will be limited to the anisotype heterojunction. Several physical quantities need to be defined for characterizing the behavior of the junction. These includes (a) work function ϕ , where $q\phi$ is the energy needed to move an electron from the Fermi level to the vacuum level; (b) electron affinity χ , where $q\chi$ is the energy needed to move an electron from the conduction band minimum to the vacuum level; (c) ΔE_c and ΔE_v are the conduction and valence band edge discontinuities, respectively.

The equilibrium energy band diagram for the heterojunction system can be easily determined by applying two simple rules: (a) the Fermi level is flat throughout the junction and (b) the bulk energy band diagrams must be recovered far from the junction [7,8,9]. Figure 2.3 illustrates how the ideal p-CdTe/n-CdS heterojunctions energy band diagram can be determined from these rules by assuming no interface charge. In these figures, E_G is the bandgap, E_F is the Fermi level, and the n and p subscripts refer to the parameters associated with the n-type and the p-type materials, respectively. Because of

Figure 2.3 Ideal energy band diagram for CdTe/CdS system (a) before and (b) after the junction are formed.

the differences in electron affinity and band gaps in each constituent material, there exists a discontinuity in the conduction and valence band edges at the metallurgical interfaces, which are respectively given by[7]

$$\Delta E_c = q(\chi_p - \chi_n) \quad (2.6)$$

and

$$\Delta E_v = E_{Gn} - E_{Gp} - \Delta E_c . \quad (2.7)$$

The ΔE_c and ΔE_v values for the CdTe/CdS heterojunction have been calculated to be -0.22eV and 1.20eV respectively. Since ΔE_c is negative and ΔE_v is positive, there is no spike in the conduction and valence bands. The absence of potential spikes constitutes an important criterion in selecting heterojunction pairs for solar cells, since the spikes can impede the current flow and limit device performance.

The diffusion voltage, V_D (also called built-in potential), represents the full band bending or potential resulting from Fermi level alignment across the interface to maintain charge neutrality. The diffusion voltage is defined as the difference in the work functions of the two semiconductors, and can be expressed as

$$qV_D = qV_{Dn} + qV_{Dp} = q\phi_p - q\phi_n = E_{Gp} + \chi_p - \delta_p - \delta_n - \chi_n , \quad (2.8)$$

where the parameters are defined in Figures 2.3. The diffusion potential, along with the band edge discontinuities, dictates the leakage current and V_{oc} of the solar cell. The diffusion voltage is divided across the junction according to

$$\frac{V_{Dp}}{V_{Dn}} = \frac{N_D \epsilon_{sn}}{N_A \epsilon_{sp}}, \quad (2.9)$$

which can be obtained by requiring the normal component of the electric displacement to be continuous across the interface, i.e. $\epsilon_{sn} E_n = \epsilon_{sp} E_p$, where ϵ_s is the relative dielectric constant. The depletion region width, W , can be found as the sum of W_p and W_n , where W_p , W_n are the width of the depletion region in p and n material respectively. W_p and W_n are given as[7,8]

$$W_{Dp} = \sqrt{\frac{2\epsilon_{sp}\epsilon_{sn}N_D V_D}{qN_A(\epsilon_{sp}N_A + \epsilon_{sn}N_D)}} \quad (2.10)$$

and

$$W_{Dn} = \sqrt{\frac{2\epsilon_{sp}\epsilon_{sn}N_A V_D}{qN_D(\epsilon_{sp}N_A + \epsilon_{sn}N_D)}}. \quad (2.11)$$

When an external voltage (V_A) is applied, V_D in the above equations is replaced by ($V_D - V_A$).

It is useful to define an ξ -factor as

$$\xi = 1 + \frac{N_A \epsilon_{sp}}{N_D \epsilon_{sn}}, \quad (2.12)$$

which quantifies the division of the depletion region in the p and n materials. The ξ -factor varies according to the relative doping concentrations. For heterojunction solar

cells such as CdTe/CdS, the wide bandgap window layer (n-CdS) is doped much more heavily than the absorber (p-CdTe), i.e. $N_D \gg N_A$, to minimize resistance losses from the CdS. Hence, the depletion region exists almost exclusively in the p-type CdTe absorber, i.e., $W \sim W_p$ and $\xi \sim 1$. We will apply the $\xi \sim 1$ condition (depletion region exists almost entirely in the p-type CdTe absorber) in the next section, which discusses the current transport mechanisms.

2.4 Current Transport Mechanisms in Heterojunction

Section 2.3 reviewed important basic properties of heterojunctions. In this section, heterojunction current transport mechanisms relevant to CdTe/CdS are described. Electron-hole pairs are generated in a solar cell device when the light illuminates. Before the light generated carriers can be collected, they could recombine at the native defects, grain boundary states, or CdTe/CdS interface states. Therefore, in order to understand the CdTe bulk and CdTe/CdS interface quality, the dominant carrier loss mechanisms need to be analyzed. Current transport analysis is the best way to reveal and quantify the recombination mechanisms in the CdTe/CdS heterojunction solar cells, and to understand the bulk as well as interface properties. This provided the motivation to conduct current transport analysis on the CdTe/CdS devices. If CdTe cells grown under different conditions show different transport mechanisms, it may reveal the correlation between

defects, cell performance, and current transport mechanisms.

The general J-V characteristic of a p-n heterojunction can be described as follows:

$$J = J_0 \left[e^{\frac{qV_j}{AkT}} - 1 \right], \quad (2.13)$$

where V_j is the voltage across the junction, J_0 is the diode reverse saturation current density, and A is the diode ideality factor, which equals to $(q/kT) \times [\partial V_j / \partial (\ln J)]$. A number of models describing current transport in heterojunction have been proposed [8]. They can be divided into two groups: thermally-activated transport and nonthermally-activated transport. Thermally-activated transport can be classified into three major categories: (a) minority carrier injection and diffusion into quasi-neutral region, (b) depletion region recombination, and (c) interface recombination (Figure 2.4). All the thermally-activated transports reveal temperature-dependent slopes ($=q/AkT$) of the $\ln(J)$ - V_j curves, and the diode ideality factor A remains constant. Nonthermally-activated current transport is generally described by tunneling processes, which involve interface and/or bulk states. For the tunneling transport, the slopes of the $\ln(J)$ - V curves are temperature-independent. It is also possible to combine thermally-activated and tunneling processes to form thermally-assisted tunneling mechanisms.

Current transport in heterojunctions like CdTe/CdS junction is complicated by the presence of the heterointerface, which introduces not only band edge discontinuities but

Figure 2.4 Schematic of diode current transport by (a) injection/diffusion, (b) depletion region recombination, and (c) interface recombination in a forward biased CdTe/CdS heterojunction.

also interface defects. The presence of electrically-active interface states can affect heterojunction properties by providing a large density of recombination centers and/or interface charge which can distort the ideal band profiles. As a result, heterojunctions can exhibit various combinations of current transport mechanisms. However, while many transport mechanisms may operate simultaneously, usually one mechanism dominates or limits the terminal current-voltage (I-V) characteristics of a heterojunction device [1].

The basic model of heterojunction transport in the ideal situation is similar to the homogeneous p-n junction in which current flows entirely by injection of carriers over the conduction or valence band barriers, followed by diffusion into the quasi-neutral regions. As the electrons are injected into the p-type region, they recombine with the majority carrier, exhibiting a diffusion profile. If there are no interface or bulk defect states, the electron current injected into the p region can be obtained by solving the diffusion equations. The total current is the sum of the electron current and hole current [8,9]:

$$J = J_o [\exp(\frac{qV_j}{kT}) - 1] \quad (2.14)$$

and

$$J_o = J_{op} + J_{on} = q \left[\frac{D_p n_{po}}{L_p} + \frac{D_n p_{no}}{L_n} \right], \quad (2.15)$$

where D_p and D_n are the hole and electron diffusion coefficients in the n-type and p-type

regions, n_{po} and p_{no} are the electron and hole carrier density in p and n quasi-neutral region, respectively. For the heterojunction case, n_{po} and the electron carrier density in n quasi-neutral region (n_{no}) can be expressed as [7]:

$$n_{po} = N_{cp} \exp\left(-\frac{E_{cp} - E_F}{kT}\right), \quad n_{no} = N_{cn} \exp\left(-\frac{E_{cn} - E_F}{kT}\right), \quad (2.16)$$

where N_{cp} and N_{cn} are the conduction band density of states in the p-type and n-type material, respectively. Since the difference between the conduction band edge in p quasi-neutral region (E_{cp}) and n region (E_{cn}) is $V_D + \Delta E_c$, the relationship between n_{po} and n_{no} can be expressed as:

$$n_{po} = \frac{N_{cp}}{N_{cn}} n_{no} \exp\left(-\frac{qV_D + \Delta E_c}{kT}\right). \quad (2.17)$$

Similarly, the relationship between the hole carrier density p_{po} and p_{no} can be written as:

$$p_{no} = \frac{N_{vn}}{N_{vp}} p_{po} \exp\left(-\frac{qV_D + \Delta E_v}{kT}\right). \quad (2.18)$$

Therefore, the J_o for a heterojunction becomes:

$$J_o = q \left[\frac{D_p N_{vn}}{L_p N_{vp}} p_p \exp\left(-\frac{qV_D + \Delta E_v}{kT}\right) + \frac{D_n N_{cp}}{L_n N_{cn}} n_n \exp\left(-\frac{qV_D + \Delta E_c}{kT}\right) \right] \quad (2.19)$$

Upon inspection of Figure 2.3, hole transport across the CdTe/CdS interface into the n-type CdS is negligible compared to the electron current because of the large barrier to holes compared to electrons. Hence, the first term on the right hand side of Equation (2.19) is negligible and the diffusion current is dominated by minority carrier electrons injected into the p-type absorber. Even though the current transport by minority carrier injection and diffusion indeed occurs at heterojunction, it is generally not the dominant current component in heterojunctions because the assumption of no interface and bulk defects does not hold for most heterojunction devices.

The next thermally-activated transport mechanism involves depletion region recombination. Depletion region recombination is described by the Shockley-Read-Hall (SRH) recombination model, in which the carriers recombine through defect traps in the depletion region. The recombination current can be obtained by integrating the recombination rate U throughout the depletion region width W [7,10]:

$$J_{rec} = \int_0^W qU dx \quad (2.20)$$

and

$$U = \frac{\sigma_p \sigma_n v_{th} (np - n_i^2) N_t}{\sigma_n \left[n + n_i \exp\left(\frac{E_t - E_i}{kT}\right) \right] + \sigma_p \left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right) \right]}, \quad (2.21)$$

where σ_p and σ_n are the hole and electron capture cross sections, respectively, v_{th} the

carrier thermal velocity, N_t the trap density, E_t the trap energy level, E_i the intrinsic Fermi level, and n_i the intrinsic carrier density. If we use simplified conditions $\sigma_n = \sigma_p = \sigma$ and $E_t = E_i$ (midgap traps), the J-V characteristics for the depletion region recombination become [11,12]:

$$J = J_o \left[\exp\left(\frac{qV_i}{2kT}\right) - 1 \right] \quad (2.22)$$

where

$$J_o = \frac{qW_D}{2} \sigma v_{th} N_t n_i = \frac{qW_D}{2} \sigma v_{th} N_t \sqrt{N_c N_v} \exp\left(\frac{E_g}{2kT}\right). \quad (2.23)$$

Notice that the midgap trap assumption leads to a diode ideality factor of 2.

Interface recombination in heterojunctions is the third thermally-activated transport mechanism, which occurs via thermionic emission of electrons and holes over their respective barriers into the interface states where they recombine, as shown in Figure 2.4c. This process is modeled by back to back Schottky diodes (metal/semiconductor contacts) in series on either side of a metallic-like interface layer characterized by a large interface recombination velocity, S_i . S_i is the rate at which electrons and holes recombine at the interface. Because the doping concentration in the CdS window is much greater than that of the CdTe absorber, the supply of holes from the CdTe limits the rate of recombination. Hence, the interface recombination current can be expressed as [8]

$$J \approx J_p = qp_I S_I , \quad (2.24)$$

where p_I is the hole carrier concentration at the interface region. The relationship between p_I and the hole density in the quasi-neutral region p_o is given by

$$p_I = p_o \exp\left(-\frac{q(V_D - V_i)}{AkT}\right) . \quad (2.25)$$

Therefore, the interface recombination current can be rewritten as [13,14]

$$J = J_o \exp\left(-\frac{qV_i}{kT}\right) = qp_o S_I \exp\left(-\frac{qV_D}{kT}\right) \exp\left(-\frac{qV_i}{kT}\right) . \quad (2.26)$$

The three carrier transport mechanisms described above (injection/diffusion, depletion region recombination, and interface recombination) predict temperature-dependent slopes ($= q/AkT$) of the $\ln J$ - V characteristics because they can all be described by thermally-activated processes such as recombination or diffusion. However, in many heterojunctions, the slopes of the $\ln J$ - V curves are found to be relatively constant and independent of temperature which can not be explained by thermally-activated processes. For the nonthermally-activated processes, the J - V behavior often follows [8,15]

$$J = J_{oo} \exp(\beta T) \exp(\alpha V_i) , \quad (2.27)$$

where the constants α and β are independent of voltage and temperature. J - V characteristics of this form are attributed to current transport via quantum mechanical

tunneling. Because no spikes or barriers exist in the band diagram of Figure 2.3, any tunneling in the CdTe/CdS heterojunctions must involve interface states and/or energy levels within the depletion region. Figure 2.5 shows some examples of possible tunneling routes [7]. An electron starting at C could drop down to an empty level at B, then it could tunnel to D. Another route that could occur is a staircase from C to D, which consists of a series of tunneling transitions between local levels, A, together with a series of vertical steps by transferring from one level to another. The basic requirements for tunneling current are a large number of electrons separated from a large number of empty states (these can be either energy states on conduction band, interface states or energy levels within the depletion region) by a narrow barrier of finite height. Since the tunneling current depends upon the width of the barrier, it is important that the metallurgical junction be sharp, so that the transition region W extends only a very short distance for the carrier to tunnel through [16]. The interband tunneling mechanism (routes C-B-D in Figure 2.5), which was proposed by Riben and Feucht [17], assumed direct (or nonthermal) tunneling to be the rate-limiting process. Therefore, the J-V characteristics will reflect the tunneling behavior of the junction, which can be described by [18]

$$J = BN_i \exp(-\alpha V_D) \exp(\alpha V_i) \quad (2.28)$$

and

Figure 2.5 Schematic of diode current transport by (a) single step tunneling and (b) multi-step tunneling via interface and depletion region states.

$$\alpha = \frac{8\pi \sqrt{m_v^* q}}{3hH} , \quad (2.29)$$

where H and B are constants, N_t is the density of traps, m_v^* is the hole tunneling effective mass, and h is the Planck's constant. Notice that for the CdTe/CdS device, the current transport is dictated by the CdTe since the depletion region exists almost entirely within the lower doped absorber. Riben and Feucht later extended this model to include the possibility of stepwise tunneling and recombination through closely spaced states within the depletion region which allows their model to be applied to devices with much thicker depletion regions than does the single step tunnel model (Figure 2.5). To account for the possibility of multi-step tunneling, the single step tunnel model is modified by [18]

$$\alpha = \frac{8\pi \sqrt{m_v^* q}}{3hH} \frac{1}{\sqrt{R}} , \quad (2.30)$$

where R is the number of tunneling steps required to traverse the depletion region.

In addition to the single and multistep tunneling models, it is also possible to combine tunneling and thermal activation, in which carriers are thermally activated to higher energies (where the potential barrier is thinner and tunneling probability is increased), where they tunnel through the barrier into interface states and recombine. This is called thermally-assisted tunneling (or thermionic field emission) mechanisms.

The barrier energy where the tunneling current is maximum is determined by maximizing the product of the tunneling probability and the carrier density, which requires detailed knowledge of the band structure in the depletion region. Miller and Olsen[19] attempted to quantify the thermally-assisted tunneling process in an approximate form for cases in which exact determination of the band structure in the depletion region is difficult, such as polycrystalline heterojunction solar cells (they modeled $\text{CuInSe}_2/\text{CdS}$ devices), where grain boundaries complicate the picture. They approximated the thermally-assisted tunneling process by a series combination of direct tunneling and pure interface recombination. In this tunneling/interface recombination (T/IR) model, a linear potential relation is assumed in the space charge region, and the tunneling occurs at a diffusion potential V_m described by

$$V_m = f(V_p - V_0) + V_0 = fV_p + (1-f)V_0, \quad (2.31)$$

where V_m , V_p , and V_0 are depicted in Figure 2.6. The f parameter quantifies the extent of tunneling, where $f=1$ represents pure interface recombination with no tunneling, and $f=0$ corresponds to direct tunneling. According to the T/IR model, the J-V relation is given by[19]

$$J = J_o [e^{qV_f} - 1], \quad (2.32)$$

where

$$J_o = J_{oo} e^{\frac{-\Delta E}{kT}} \quad (2.33)$$

Figure 2.6 Schematic of diode current transport via thermally-assisted tunneling from the valence band into interface states followed by fast interface recombination (after ref.19).

and

$$C = (1 - f)B + \frac{f}{(\xi kT)} \quad , \quad (2.34)$$

where ΔE is the thermal activation energy, B is a temperature-independent tunneling parameter, C is the slope of the $\ln J$ vs V_j curve, and ξ represents the voltage division between the CdTe and CdS.

The above discussion summarizes the various carrier transport mechanisms possible in the CdTe/CdS heterojunctions, which will be used later in this research to determine the efficiency limiting defects and loss mechanisms. By careful analysis of the temperature dependence of the measured J-V-T characteristics (mainly diode ideality factor A and saturation current density J_0), it is clear that the dominant current transport mechanisms in CdTe/CdS heterojunction devices can be determined. The experimental techniques used to fit and obtain the measured J-V-T data are discussed in Chapter III.

The relevant transport analysis procedures used in this study are summarized as follows: (a) if the diode ideality factor A is temperature-dependent, it eliminates the possibility of transport via straight depletion region or interface recombination[13,20]; (b) if the ideality factor is temperature-independent, and the activation energy (slope of $\ln(J_0 T^{-2.5})$ vs $1000/T$) is half of the bandgap[20], then the transport is dominated by depletion-region recombination and J_0 can be written as Equation (2.23); (c) if the $\ln J$ - V_j slope ($=q/AkT$) is temperature-dependent, and J_0 is thermally activated, it eliminates the

possibility of direct tunneling as the dominant transport mechanism; and (d) if the current transport can be described by the tunneling/interface recombination (T/IR) model, then the J-V characteristics will follow Equations (2.32) to (2.34), and the f parameter can be utilized to quantify the extent of tunneling at the heterojunction.

2.5 Efficiency Limiting Defects and Mechanisms in CdTe/CdS

Solar Cells

There has been a steady increase in the efficiency of front wall CdTe solar cells in the past few years with one group reporting the maximum efficiency of 15.8% to date. However, most of the CdTe cells, made by different groups, are still in the efficiency range of 10-12% with significant variation in cell parameters. The theoretical maximum photocurrent available from a CdTe solar cell under the standard global spectrum, 100 mW/cm² (air mass 1.5), is 30.5 mA/cm² [21]. It is found that a short-circuit current density (J_{sc}) of 26-28 mA/cm² [22] can be achieved by minimizing the reflection and absorption losses. For a 1.44 eV bandgap material, if the recombination at the interface and in the bulk can be reduced, over 900 mV open- circuit voltage (V_{oc}) can be attained [23,24]. Combining the above practically attainable cell parameters, J_{sc} and V_{oc} , it is possible to achieve 18% efficient polycrystalline CdTe solar cells [17,22]. However, there is a big gap between current and achievable CdTe cell efficiency because the efficiency

limiting defects and mechanisms have not been identified or understood. This provided the motivation to investigate loss mechanisms in the CdTe/CdS solar cells and to improve the fundamental understanding of the efficiency limiting factors.

2.5.1 Native Defects in CdTe

In a II-VI compound like cadmium telluride, the outer shells of the group II (Cd) and group VI (Te) elements have the ns^2 and mp^4 configuration, respectively. Since the II-VI compounds are partly ionic, the group II element exists as a doubly charged cation (M^{2+}) and the group VI element exists as a double charged anion (X^{2-}) [9]. As the II-VI compounds become more ionic, they possess a lower cohesive energy, which increases the probability of forming native defects such as vacancies and interstitials. These native defects can also interact with the residual impurities in the material to form complexes. Hence, the electrical properties of CdTe are dominated by native defects, impurities, and defect-impurity complexes [25].

A. Interstitial defects in CdTe

Consider the electrical activity of native interstitial defects, Cd_i and Te_i . The electropositive Cd_i will tend to give one or more electron to the conduction band according to the following equation:

The extent of ionization depends on how strongly the outer electrons are bound to the interstitial atom, or the energy level E_i with respect to the conduction band. For Te interstitial, similar equation can be applied for the ionization of Te_i :

Thus, Cd interstitials behave as donors and Te interstitials act as acceptors [9].

B. Vacancies in CdTe

Because of the absence of the more electropositive Cd atom from the lattice, cation vacancies (V_{Cd}) are devoid of electrons, and hence behave as an acceptor type defect. The neutral Cd vacancy becomes negatively charged when it traps an electron (or donates a hole). Similarly, the Te vacancy (V_{Te}) behaves as an electron donor defect.

In the case of Schottky defects, where an equal number of Cd and Te vacancies are present in the material, the electrical activity of the defects opposes one another. Similarly, the Frenkel defect associated with Cd interstitial (Cd_i) tends to neutralize the electrical activity of Te interstitial (Te_i). Because the extent of ionization depends on the energy of the defect levels, complete compensation may not occur even when donor and acceptor defects are equal in number. Therefore, the net carrier concentration depends on the number of defects as well as the energy levels of the defects in the CdTe material.

C. Electrical compensation

The presence of native defects makes the control of carrier concentration in CdTe

more difficult [26], therefore, high conductivity CdTe materials cannot be obtained easily because of the self-compensation effects [27]. Consider a compensation model with indium donor [25], the existence of In atoms in the CdTe not only forms a donor (In_{Cd}^+) but also forms an acceptor type complex ($\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+$) and a fairly neutral entity ($\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+$) with Cd vacancies. Therefore, the total In concentration $[\text{In}_{\text{Cd}}]_{\text{T}}$ can be written as:

$$[\text{In}_{\text{Cd}}]_{\text{T}} = 2[\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+] + [\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+] + [\text{In}_{\text{Cd}}^+] . \quad (2.37)$$

Charge neutrality is maintained in the crystal primarily by the Cd vacancies (acceptor), In donor, and $\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+$ acceptors so that

$$2[\text{V}_{\text{Cd}}^{2-}] + [\text{V}_{\text{Cd}}^{2-}\text{In}_{\text{Cd}}^+] \approx [\text{In}_{\text{Cd}}^+] . \quad (2.38)$$

Because of the high resistivity of CdTe material, the concentration of free electron and holes are small. If more In atoms are added to the CdTe material in an attempt to increase donor concentration then, because of the charge neutrality, the acceptor concentration also increases to compensate the increase in donor density. Similarly, compensation phenomena can also be found in p-type CdTe [25]. For example, the noble metals Au, Cu, and Ag primarily substitute for Cd and act as acceptor but they can also fill interstitial positions and act as donors. Mandel [27] calculated the dopant activity in n-CdTe, p-CdTe, n-ZnTe, and GaAs to be 3, 0.11, 0.32, and 99 %, respectively, at the growth temperature of the bulk materials. Therefore, the compensation effect is much

greater in II-VI materials compared to the III-V compounds like GaAs.

Native defects, impurities, and defect-impurity complexes affect the CdTe material properties as well as solar cell performance because (a) these defects can form recombination centers to reduce the carrier collection and increase the diode reverse saturation current density (J_0), lowering the J_{sc} and V_{oc} , and (b) highly resistive CdTe film because of the compensation effect not only decreases the built-in potential at the CdTe/CdS interface to lower V_{oc} , but also makes the ohmic contact with CdTe more difficult resulting in increase in the series resistance (R_s). This provided the motivation to investigate the impact of native defect concentration on the CdTe cell parameters.

2.5.2 Grain Boundary Effects in Polycrystalline CdTe Cells

Thin-film technology is a leading candidate for low-cost solar cells because very small quantity of materials is deposited on inexpensive substrate, like glass. Since the CdTe and CdS layers are deposited on a disordered substrate, it forms a polycrystalline structure in which the presence of grain boundaries lowers the cell efficiency. The grain boundary consists of a layer of disordered atoms in a transition region between neighboring grains. This results in the formation of high density of trapping states which can trap and immobilize carriers [28]. The existence of these donor and acceptor-like states often pins the Fermi level, producing band bending and potential barriers [29].

The major effects of grain boundaries on the material quality and solar cell performance include: (a) potential barriers at the grain boundaries which may impede current flow and raise resistivity by lowering the carrier mobility [13], (b) high grain boundary recombination velocity, as high as 4×10^5 cm/s [14], which can increase the dark currents and lower photocurrent to degrade V_{oc} and J_{sc} , and (c) possible conduction along the grain boundaries which can cause shunting paths [6] and lower fill factor. It has been shown that the degradation of junction properties and solar cell performance in many materials are related to grain boundary effects. The above grain boundary effects can be minimized by increasing the grain size, which reduces the grain boundary surface area per unit volume. This provided the motivation to increase the CdTe grain size by post-deposition chemical and heat treatment.

2.5.3 The Effects of CdTe/CdS Interface States

In a normal p-n homojunction, the same crystal structure continues right through the junction. In a heterojunction structure like CdTe/CdS, band edge discontinuity occurs along with the lattice mismatch at the interface, resulting in defect states. The presence of interface states in heterojunction has been attributed to (a) dangling bonds due to lattice mismatch, (b) difference in thermal expansion coefficients, (c) impurities, and (d) growth-induced defects. Therefore, the interface quality can be improved by gradually changing

the band edge from one material to the other to release lattice mismatch [30,31], and by optimizing the growth conditions to reduce impurities and growth-induced defects. The interface states give rise to energy levels within the forbidden gap, which act as efficient recombination centers. The recombination behavior of the interface states can be quantified by an effective interface recombination velocity S_i [32]. A high value of J_o can be expected in heterojunctions because of interface recombination. These interface states can also provide sites for quantum mechanical tunneling for carrier transport from one side of the junction to the other.

Interface states have a significant effect on the CdTe/CdS solar cell performance [33]. In addition, grain boundaries that intersect CdTe/CdS junction make the interface quality even worse. The value of J_{sc} is reduced because the photo-generated carriers are lost via recombination at the interface. High recombination current, J_o , causes V_{oc} to diminish according to Equation (2.5). In addition, the photocurrent in the CdTe solar cells becomes a function of bias voltage [34]. It has been shown that these effects not only decrease the collection efficiency as the bias voltage is applied, but also cause a cross-over in the light and dark I-V curves, resulting in further decrease in fill factor and V_{oc} . The collection probability $h(V)$ of photon-generated carriers through the junction in the presence of interface recombination is shown in Equation (2.2). Since S_i is proportional to the interface defect density, higher defect density results in poor carrier

collection and lower quantum efficiency (QE).

Interface quality can be improved by intermixing of CdTe/CdS interface (interdiffusion) to release lattice mismatch. Some amount of interdiffusion has been observed in the CdTe/CdS solar cells after the post-growth treatments. The diffusion of sulphur into the CdTe layer forms a $\text{CdTe}_{1-x}\text{S}_x$ interlayer and reduces the CdTe lattice constant slightly. Ohata et al. [35] found that the addition of small amount of S ($x < 0.25$) reduces the CdTe bandgap, and the $\text{CdTe}_{1-x}\text{S}_x$ energy gap could be expressed by a quadratic equation as a function of composition x : $E_g(x) = 1.74 x^2 - 1.01 x + 1.51$. This provided the motivation to enhance interdiffusion at the CdTe/CdS interface by optimizing the CdTe growth conditions and post-deposition treatments like rapid thermal anneal.

2.5.4 Photocurrent Loss in the CdS Window Layer

The CdS window layer plays a critical role in determining the electrical and optical properties of CdTe solar cells. It has been found that annealing the CdS films at temperatures greater than 400° C in hydrogen atmosphere, before the CdTe deposition, improves the CdTe cell performance [36]. This is because the heat treatment removes the oxygen, which is known to be a detrimental recombination center in the CdS [37]. The heat treatment of the CdS film also changes the current transport mechanism from temperature independent tunneling to a thermally-activated process. However, some

degree of interface recombination is still involved [38]. These results indicate that further enhancement of the CdTe/CdS interface quality is possible by optimizing the growth and heat treatment conditions.

Sites [21] showed that the major photocurrent loss in the present front wall CdTe/CdS solar cells is associated with the reflection and the absorption in the CdS window layer. Since the CdS film acts as a dead layer, resulting from recombination of most of the photo-generated carriers in the CdS, its thickness has significant impact on the cell efficiency. In addition, CdS thickness also affects the multiple beam interference at the CdS/SnO₂/glass interface, which could change the reflectance of the cell surface. However, CdS should not be too thin because pin-holes in the thin CdS films can give rise to low shunt resistance and reduce V_{oc} and fill factor [39,40]. The diode ideality factor also increases as the thickness of the CdS films is reduced. This provided the motivation to investigate the correlation between CdS thickness, absorption and reflection losses, and cell performance.

2.5.5 CdCl₂ Treatment Induced Loss Mechanisms

A CdCl₂ treatment is performed during the CdTe solar cell processing, which involves treating or dipping the CdTe/CdS structure in a CdCl₂:CH₃OH solution followed by an air anneal at 400°C. This treatment is utilized to promote grain growth [41] and

is known to produce significant increase in the CdTe/CdS solar cell efficiency [42]. Romeo et al. proposed a possible mechanism for the grain growth [43]. According to this model, some gas-phase Cd and TeCl_2 are formed from dissociation reaction at the annealing temperature and are transported by the carrier gas. They could react again to form additional CdTe grains according to the following dissociation-recombination equation:

Since the chemical potential for large grain is less than that of small grains, when the grains begin to form, the grain size is enhanced at the expense of the small grains.

Several investigators [39,44] have studied the role of CdCl_2 treatment on the CdTe/CdS interface and bulk quality. The CdCl_2 treated CdTe cells generally show a higher QE and a smaller bias-dependent QE, indicating an improved interface collection function, $h(V)$, resulting from the reduced number of interface defect states after the CdCl_2 treatment. However, Ringel et al. showed by DLTS measurements [44] that CdCl_2 treatment could result in a large density of deep acceptor-like states at $E_v + 0.64$ eV since traps in the vicinity of $E_v + 0.6$ eV have been attributed to V_{Cd} and $V_{\text{Cd}}\text{-Cl}$ related complexes. It was found that the V_{oc} is inversely proportional to the trap density while there is no apparent correlation between the J_{sc} and trap density (Figure 2.7). Thus, on one hand CdCl_2 treatment is critical for high efficiency CdTe cells, but on the other hand

Figure 2.7 (a) DLTS spectrum of a CdTe/CdS cell annealed with CdCl₂, (b) measured V_{oc} and J_{sc} as a function of trap concentration as determined from the DLTS data (after ref. 44).

it could place an upper limit on the practically achievable efficiency. This provided the motivation to study the role of CdCl₂ treatment along with the objective of modifying or optimizing the process to maximize its benefit.

2.5.6 Ohmic Contacts to CdTe Cells

Low resistance contacts between the electrodes and semiconductor films are critical for high efficiency solar cells. It is especially difficult to make a low-resistance contact to p-type CdTe for CdTe/CdS solar cells. The difficulties come from the compensation mechanism of II-VI semiconductor, and the properties of p-type CdTe material, which are discussed below.

An ohmic contact has a negligible potential drop. The specific contact resistance R_c can be evaluated from the slope of the current-voltage characteristics at zero voltage, that is[45]:

$$R_c = A \left(\frac{dI}{dV} \right)^{-1}_{V=0}, \quad (2.40)$$

where A represent the contact area.

In general, CdTe solar cells should have a total contact resistance $R_c < 0.9 \Omega\text{-cm}^2$ in order to limit the $J^2 R_c$ loss to about 3%[46]. The realization of an ohmic contact can be based on one of the following mechanisms: (a) utilizing a contact material with the proper work function to provide a lower barrier height (ϕ_b), (b) heavily doping the

semiconductor adjacent to the contact to provide tunneling, or (c) adding recombination centers to the semiconductor adjacent to the contact which can increase the current flow.

Schottky model of a metal/semiconductor interface gives the barrier height $\phi_b = \phi_m - \chi$ for n-type semiconductor and $\phi_b = E_g - (\phi_m - \chi)$ for p-type semiconductor, where ϕ_m is the metal work function and χ is the electron affinity of the semiconductor (Figure 2.8). The model predicts that the choice of the ϕ value can result in accumulation, neutral, or depletion contact[45]. According to this model, ohmic contact requires a metal whose work function (ϕ_m) is lower than the n-type semiconductor, while the work function needs to be about equal to the energy gap plus the electron affinity for p-type semiconductor. The electron affinity of CdTe is about 4.3-4.5 eV, therefore, for a p-type material, the metal ϕ_m needs to be over 5.8 eV for a good ohmic contact. No metal meets this requirement. Even with the metals like Au, Pt, and Ni, which have a large work function ($\phi_m=5.1$ to 5.2 eV), the barrier height for the metal/CdTe contact is still about 0.6 eV. Based on the thermionic emission theory, I-V characteristics of a metal-semiconductor junction can be expressed as:[7]

$$J = \left(\frac{4\pi q m^* k^2}{h^3} \right) T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \exp\left(\frac{qV}{kT}\right), \quad (2.41)$$

where m^* is the effective mass of the majority carrier. For $\phi_b=0.6$ eV, the corresponding R_c value is calculated to be about 200 $\Omega\text{-cm}^2$ [46] using an effective hole mass of 0.12 m_0 .

Figure 2.8 Schematic of a metal/semiconductor band diagram for (a) depletion, (b) neutral, and (c) accumulation.

Figure 2.9 shows how the contact resistance R_c varies with the barrier height for the CdTe at 300 K. It is clear that in order to get low R_c value ($0.1 \Omega\text{-cm}^2$), the ϕ_b needs to be less than 0.4 eV, which can not be achieved by using a metal contact.

Various schemes for making ohmic contacts to CdTe have been investigated. For example, low resistivity HgTe or $P^+\text{-ZnTe}$ have been shown to be satisfactory contact material. ZnTe can be made p-type more easily than the CdTe [47] and the electron affinities predict a valance band discontinuity of 0-0.2 eV with CdTe. HgTe is another such material and R_c values as low as $0.2 \Omega\text{-cm}^2$ have been obtain by growing HgTe on p-CdTe doped to $8 \times 10^{15} \text{ cm}^{-3}$. However, the stability of the contact is questionable [46].

One alternative to relax the requirement of lower ϕ_b is to dope the semiconductor heavily enough so that the field emission (tunneling) rather than thermionic emission becomes the dominant mechanism for current transport. The I-V characteristics for the field emission transport is similar to Equation (2.28). Using this equation and the model proposed by Yu[48], the contact resistance value can be calculated as a function of the doping level and barrier height (Figure 2.10). The functional dependence of R_c on these two factors can be written as:

$$R_c \propto \exp\left(\frac{\phi_b}{\sqrt{N}}\right). \quad (2.42)$$

Based on the above relationship, Ponpon predicted that carrier density (N_A) of about $3 \times$

Figure 2.9 Specific contact resistance ρ_c of a CdTe Schottky barrier as a function of the barrier ϕ_B (after ref. 49).

Figure 2.10 Specific contact resistance of a CdTe Schottky barrier as a function of the doping N of the base material (after ref. 49).

10^{18} cm^{-3} for $\phi_b=0.6 \text{ eV}$ would be required to make $R_c < 0.2 \Omega\text{-cm}^2$ [49]. For the p-CdTe, such high doping density is difficult to obtain because of the compensation effects.

The third scheme to make an ohmic contact involves high density of recombination centers within the junction to promote multistep tunneling. Most ohmic contacts to CdTe involve a combination of low ϕ_b metals, heavy surface doping and surface modification. Some of the promising contact strategies and methods are summarized below.

One of the first method to produce ohmic contact on p-CdTe was electroless deposition of a noble metal from a solution, generally a chloride. Ag, Au, Ir, Pt, and Rh contact have been formed by this method. In the Au contact formation, Cd diffuses out of the CdTe adjacent to the growing Au film, leaving a Te-rich region near the CdTe surface. At the same time, Au tends to diffuse in, aided by the Cd vacancy density, to provide p-type doping. The dopant sites also assist in the tunneling process.

Au contact is also formed by vapor deposition of Au or Au-Cu alloy on an etched surface, using etchants such as $\text{H}_2\text{SO}_4\text{-K}_2\text{Cr}_2\text{O}_7\text{-H}_2\text{O}$ or MeOH-Br_2 [50]. These etches leave a film of Te or a Te-rich surface which significantly lowers the resistivity of the CdTe surface. Anthony et al. reported a reduction of contact resistance for the Cu/Au contact compared to the Au contact [50]. The carrier transport mechanisms through Cu/Au-CdTe contact was found to be a thermally-assisted tunneling with a barrier height

of about 0.6 eV. The addition of Cu not only seems to increase the CdTe surface doping but also introduces more tunneling sites, which enhance the tunneling current and reduce the contact resistance.

Ohmic contact to CdTe solar cells have also been made by applying carbon paste or colloidal graphite with small amounts of Cu, Ag or Hg [51]. Nishitani reported that the penetration of acceptor impurities (mainly Cu) in the C-paste into the CdTe layer helps the formation of better contact [52].

Carbon paste doped with Cu or Hg and Au/Cu contact are the two contact systems that have so far produced over 10% efficient CdTe solar cell. The use of Au or carbon seems to lower the barrier height ϕ_b . The addition of acceptor impurities (mainly Cu) may form a somewhat heavily doped CdTe surface and/or provide tunneling states to reduce the contact resistance further. In spite of the partial success in achieving ohmic contact to p-CdTe, there is a considerable lack of fundamental understanding about the physics and reliability of these contact systems. Therefore, one of the major task in this research was to understand the role of Cu in forming contact and in determining the CdTe cell performance.

2.6 Specific Research Objectives and Tasks

The overall goal of this research is to improve the polycrystalline CdTe cell efficiency systematically through fundamental understanding of defect and loss mechanisms, role of chemical and heat treatments, and investigation of new process techniques. The specific objectives of this research consist of: (a) growth optimization of CdS films from aqueous solution; (b) optimization of CdTe MOCVD growth conditions by varying the Te/Cd mole ratio in growth ambient; (c) study of chemical and heat treatment of CdTe films; (d) fabrication of CdTe solar cells using rapid thermal processing; (e) investigation of contact formation to achieve low-loss and stable ohmic contacts to CdTe, (f) growth and fabrication of larger grain CdTe/CdS films and devices by lift-off process, (g) characterization of CdTe/CdS films using a variety of techniques such as AES, SIMS, XRD, PL, and SEM; (h) investigation of device performance using light I-V, C-V, carrier transport analysis, and spectral quantum efficiency measurements; (i) fundamental understanding of loss mechanisms by in-depth modeling, material growth, material and electrical characterization, and device fabrication; and (j) provide guidelines for fabricating higher efficiency cells. These objectives will be achieved by the following tasks.

A. Task 1: Growth of thin CdS window layer by solution growth process

CdS layer will be grown on SnO₂ coated glass substrate by solution growth

process, prior to CdTe deposition, using acetates or chlorides in the buffer solution. Reaction conditions will be optimized with respect to time, temperature, pH of the solution, and molar concentrations of the reactants in order to obtain thin CdS films with good quality and minimum pin-hole density. CdTe solar cells with different CdS thickness will be fabricated to study the photocurrent loss from the reflectance and absorption in the CdS layer.

B. Task 2: Analysis of the photocurrent loss in CdTe cells

Typical front wall CdTe solar cell consists of Au/Cu/CdTe/CdS/SnO₂/glass structure in which n-type CdS forms a p-n heterojunction with p-type CdTe, and the SnO₂ forms ohmic contact to CdS. Since the light enters from the glass surface, CdS/SnO₂ layers between glass and CdTe could affect the reflectance of the CdTe cells. Additionally, absorption in the CdS dead layer contributes to loss of photocurrent. Reduced CdS thickness and the use of anti-reflective coating on glass can result in substantial increase in short circuit current density of the CdTe cells. However, excessive reduction in the CdS thickness could give rise to pin-holes and shorts. No systematic study or analysis has been conducted so far to optimize the CdS and SnO₂ thicknesses to maximize the CdTe solar cell performance. Therefore, the purpose of this task is to minimize the reflectance and photocurrent loss in the CdTe solar cells by optimizing the thickness of CdS and SnO₂ layers. This will be done by a combination of modeling of

reflectance and absorption induced photocurrent loss, actual cell fabrication, and material and device characterization.

C. Task 3: Study of the impact of MOCVD growth ambient on CdTe solar cells

Since the native defects affect the bulk as well as the interface properties of CdTe/CdS structures, as discussed in Section 2.5.1, it is important to adjust and control the native defects to improve the CdTe cell performance. The metalorganic chemical vapor deposition (MOCVD) growth technique is a low temperature process, which is capable of controlling the growth ambient as well as the composition of deposited films. This technique can be used to alter the native defect concentration in a controlled manner. In this study, polycrystalline CdTe solar cells will be fabricated by MOCVD with varying Te/Cd mole ratio in the growth ambient in order to alter and investigate the impact of native defect concentration on CdTe cell parameters. If the effect of growth ambient is translated into the films, then the Cd-rich ambient should introduce Te vacancies, and the Te-rich ambient should introduce Cd vacancies in the bulk and at the interface. A systematic study will be conducted to understand the correlation between defects, CdTe/CdS interface properties, carrier collection, and carrier transport mechanism because of the change in the Te/Cd ratio in the MOCVD growth ambient.

D. Task 4: Investigation of the effect of CdCl₂ heat treatment on the performance of CdTe solar cells

The CdCl₂ treatment followed by a furnace anneal is known to improve cell performance significantly (Section 2.5.5). However, the exact role of the chemical and heat treatments in enhancing the cell performance is not fully understood. Therefore, an attempt will be made to increase the fundamental understanding of the CdCl₂ treatment by varying the CdCl₂ concentration and anneal conditions. The effect of CdTe growth conditions and CdCl₂ treatment on the surface morphology and grain structure of polycrystalline CdTe films will be studied. Light I-V and PL measurements will be performed on the finished devices in an attempt to correlate the CdCl₂ treatment induced change in defects with the cell performance.

E. Task 5: Fabrication of CdTe solar cells using rapid thermal processing

In addition to the conventional furnace anneal, rapid thermal processing (RTP) will be used to fabricate solar cells. The advantage of RTP lies in its ability to selectively enhance desirable processes, such as defect removal, dopant activation, grain growth, and compound formation, while minimizing undesirable effects such as re-evaporation, diffusion, and film decomposition. In addition, rapid thermal processing lowers energy consumption and can speed production. RTP has been used for homojunction formation in CdTe, InP, and CuInSe₂ thin film solar cells, as well as for grain growth in

amorphous/polycrystalline silicon cells. However, no research has been conducted on the CdTe/CdS heterojunction cells using RTP. In order to avoid the possible deleterious effects from the CdCl₂ treatment (Section 2.5.5), the use of a low-cost RTP at high temperatures may allow larger grain regrowth in CdTe films with lower concentrations, or no CdCl₂ treatment, thus reducing chlorine related defects. The controllability of temperature and time of RTP can also be used to tailor the interface interdiffusion to optimize the interface quality which is critical for the CdTe solar cell performance. Several parameters such as concentration of CdCl₂ in methanol, anneal temperature and duration of RTP anneal, and annealing ambient will be investigated in this task by complete device fabrication and detailed characterization and analysis. A comparison of the RTP and furnace annealed devices will be made to understand the role of heat treatments on bulk and interface properties on the CdTe cell performance.

F. Task 6: Improve the fundamental understanding of the role of Cu on CdTe cell performance

As mentioned in Section 2.5.6, lack of availability of a stable low-resistive and reliable contact has been a major stumbling block for the success of CdTe/CdS solar cells for terrestrial applications. Several investigators have obtained reasonable cell efficiencies by utilizing Au/Cu metal films or graphite paste doped with Cu or Hg to form ohmic contact on CdTe. Copper seems to play an important role in the above contacts by acting

as a substitutional acceptor for Cd to form a good ohmic contact. On the other hand, if Cu diffuses into the cell, it may form defect complexes or recombination centers and shunt the CdTe/CdS junction to degrade the cell performance. However, no systematic study has been conducted to date to understand the behavior of Cu in the CdTe films and CdTe/CdS cells. In order to achieve a better and reliable contact to CdTe solar cells, in this task, an attempt will be made to improve the fundamental understanding of the effect of Cu on defects and loss mechanisms in CdTe solar cells. Polycrystalline CdTe/CdS solar cells will be fabricated with different Cu thicknesses and deposition rates to alter the Cu-related defects. Measurement techniques, such as SIMS, C-V, and I-V, will be used to probe the extent of Cu migration and its influence on doping density, shunt and series resistance, and cell performance.

G. Task 7: Development of single crystal and large grain CdTe/CdS thin-film solar cells

Most of the efficiency-limiting mechanisms in the CdTe solar cells come from the polycrystalline nature of the CdTe/CdS films. It is generally believed that the existence of a high density of trapping states in the grain boundaries degrades the cell performances. Grain boundary-induced recombination and dark current can be reduced in larger grain or single crystal thin-film CdTe devices, therefore, an increase in photocurrent and V_{oc} can be expected. If there are fewer grain boundaries intersecting

CdTe/CdS heterojunction, the interface states could also be reduced, thus, the cell performance may be further enhanced. The grain boundaries in CdTe may also allow the Cu to diffuse from Au/Cu contact into the CdTe layer, which could affect the cell performance. Thus, comparisons between CdTe devices with different degrees of crystallinity will not only improve the fundamental understanding of the efficiency limiting mechanisms in polycrystalline cells, but may also expose the regions of the device that are more vulnerable to grain boundary-induced degradation. Therefore, in this task, an attempt will be made to grow CdTe thin films with different degrees of crystallinity and grain size by varying substrates and growth conditions. Solar cells will then be fabricated on these CdTe films by lift-off/etch back and film transfer techniques to understand the effect of crystallinity and grain boundaries on Cu incorporation in the CdTe films, and its impact on the CdTe cell performance. Detailed material and cell characterization will be performed by SEM, XRD, PL, and SIMS to understand the role and impact of loss mechanisms associated with defects and grain boundaries.

CHAPTER III

EXPERIMENTAL TECHNIQUES AND PROCEDURES

3.1 Introduction

This chapter describes the experimental methods used to accomplish the research goals. Details of material growth techniques, device processing, material and device characterization tools, and analytical techniques are discussed in this section.

3.2 Materials Growth, Processing and Device Fabrication

The CdTe solar cell fabrication procedure used in this research involves the following major steps:

- Solution growth of CdS on an SnO₂/glass substrate.
- CdCl₂ treatment and furnace anneal of the CdS film.
- MOCVD growth of CdTe on the CdS/SnO₂/glass substrate.
- CdCl₂ treatment and furnace anneal of the CdTe film.
- Au/Cu metallization on CdTe to form an ohmic contact.
- Contact anneal and Br₂:CH₃OH etch.

The details of the growth of CdS and CdTe films and fabrication of CdTe/CdS solar cells

are described in the following sections.

3.2.1 Solution Growth of CdS Film

In the CdTe solar cells, a transparent conducting semiconductor (TCS) is used to form heterojunction with the CdTe material. Among the various options available today, CdS is widely used as the n^+ TCS window layer. CdS films can be deposited by various techniques including vacuum evaporation, chemical vapor deposition, chemical spraying, and solution growth. The growth of CdS film from aqueous solution is a low-cost, versatile, and manufacturable for large-area thin film solar cells. Because of its promise, various investigators have used this process successfully and have made attempts to study and monitor the chemical reactions during the solution growth process [1-3].

CdS film is often deposited from the reaction between a Cd-salt (acetate, chloride, etc.), ammonia, and thiourea ($CS(NH_3)_2$) in an aqueous solution. Ammonia acts as a complexing agent, thiourea furnishes S^{2-} , and the NH_4 -salt (NH_4Cl) serves as a buffer. The following reactions are involved in the formation of CdS:

The successful deposition of CdS films of high conductivity, uniformity and smooth morphology requires a very delicate balance between various experimental parameters, such as molar concentration of the reactants, the PH of the solution, the temperature of the solution and deposition time. The solubility product plays a key role in determining the stoichiometry constant for any ratio of cations and anions. The free Cd and S ions are present in a basic aqueous medium at moderate temperature and are therefore strongly dependent on the PH and the temperature of the solution.

Solution growth of CdS is a self limiting process. The first 500-1000 Å film is smooth and generally adherent to the SnO₂/glass substrate. This step is controlled by the heterogenous nucleation which results in the formation of CdS on the growth substrate by an ion by ion condensation reaction. The reaction then moves to the next phase which is wasteful since large particles of CdS are formed throughout the solution. It is desirable to suppress this homogenous reaction since it leads to pin holes and shunting paths.

In this study, a CdS layer was grown on an SnO₂/glass substrate by the solution growth technique (Figure 3.1). The concentration of the CdCl₂, NH₄Cl, and CS(NH₃)₂ reactants was 0.002M, 0.005M, and 0.01M, respectively. The following procedure describes the growth of CdS films on SnO₂ coated glass substrates:

(a) Two 3" × 3" 1mm thick SnO₂ coated glass substrates with sheet resistance 8-10 Ω/□ were cleaned ultrasonically with TCE, ACE, methanol, followed by a DI water rinse for

CdS SOLUTION GROWTH PROCESS

Figure 3.1 Schematic of CdS solution growth process.

10 minutes.

(b) About 100ml of the CdCl_2 solution, 100ml of the NH_4Cl solution and 1470 ml of DI water were added in a 4 liter beaker.

(c) The beaker was then placed on a hot plate equipped with a magnetic stirrer and heated to 82°C . The two substrates were clamped together, with SnO_2 coating on the outside, and rinsed thoroughly with DI water and then blown dry with N_2 . They were then mounted vertically on a teflon holder and lowered into the beaker containing the above solution.

(d) About 150 ml of 30 % ammonia was added into the beaker. After allowing sufficient time for the reaction mixture to attain a steady state temperature of 82°C , 200 ml of hot thiourea solution was added to start the film growth. The stirring was kept at moderate speed to avoid vibrations and the beaker was covered with a pyrex or a glass plate to reduce the evaporation of ammonia and prevent the changes in the PH value.

(e) After the addition of thiourea solution, the reaction mixture turned faint yellow in color after 2 or 3 minutes, and orange in 4 to 5 minutes. The substrate was pulled out of the solution at the end of 10 minutes, which resulted in the CdS film thickness of 800 - 1000 Å.

(f) The substrate was thoroughly rinsed in the DI water followed by N_2 blow-dry. It was then ultrasonically cleaned in methanol for 15 minutes followed by a DI water rinse.

(g) To obtain thicker CdS films, the entire process was repeated again on the same substrate. Typically, two consecutive runs resulted in the CdS thickness in the range of 2000 Å to 3000 Å. Furthermore, it was found that the CdS thickness was 100-200 Å more in the interior of the substrate probably because of insufficient stirring close to the walls of the beaker.

Prior to the deposition of the CdTe layer on top of CdS, several drops of $\text{CdCl}_2 \cdot \text{CH}_3\text{OH}$ solution were poured on the CdS surface and then the sample was placed on a hot plate to dry, leaving a thin CdCl_2 film on the CdS surface. The sample was then annealed in a furnace at 450°C for 50 minutes in N_2 ambient. Finally, the CdS/ SnO_2 /glass substrate was rinsed in DI water to remove the CdCl_2 residue and was then ready for the CdTe growth.

3.2.2 Metalorganic Chemical Vapor Deposition (MOCVD) of CdTe Film

MOCVD growth technique has been utilized to grow thin layers of compound semiconductors by the co-pyrolysis of various combinations of organometallic compounds and hydrides. This technique has been successfully used to fabricate a number of optoelectronic and high-speed electronic devices. These devices include lasers, LED, solar cells, phototransistors, field effect transistors, and modulation doped field effect transistors. The main advantages of MOCVD are: (a) a large driving force (i.e. a large

free energy change) for the pyrolysis of the source chemicals; This means that a wide variety of materials can be grown using this technique that are difficult to grow by other epitaxial techniques; (b) all constituents are in the vapor phase which allows a precise control of important process parameters such as partial pressures; (c) dopant concentration and distribution can be controlled to an extent that is not attainable by other techniques; (d) complex multiple layer structures can be grown; and (e) scale up to production volumes is simpler than other techniques.

A typical MOCVD deposition system is divided into four parts: (a) metalorganic source, (b) gas mixing system, (c) reactor, and (d) power source for substrate heating.

The organometallic sources, which are typically liquids at room temperature, are kept in clean Teflon lined stainless steel containers referred to as bubblers; the temperature of the bubblers is controlled with constant temperature bath circulators. A carrier gas is passed through the bubbler, which transports the source material into the reactor. The temperature of metalorganic source is important because the vapor pressure determines the amount of source that carrier gas can transport into the reaction chamber.

The gas mixing system consists of a network of clean, leak free stainless steel tubing. Each source gas can be directed to the main mixing manifold leading to the reactor or to a bypass manifold leading to the exhaust. Gas flow is controlled by the use of electronic mass flow controllers, and the desired mixing is accomplished by using a

variety of control valves.

Two types of reactors, horizontal and vertical, are commonly used for MOCVD. In a vertical reactor, reactants are introduced from the top and the wafer lies flat on top of a graphite susceptor. The vertical reactor design is more difficult to scale for large wafers, since the gas is not so easy to model as in the case of the horizontal design. The horizontal reactor uses a rectangular graphite susceptor that can be tilted into the gas stream to improve uniformity.

RF induction heating is commonly used to heat the reactants. In certain cases, infrared heating using quartz halogen lamp is used. The exhaust system removes unreacted gases and byproducts from the reaction chamber and also provides a path for reactants to bypass the reaction zone, when needed.

MOCVD growth mechanism is highly complex. In general, the growth process can be divided into four steps: first step involves transport of chemicals into the reactor by means of a carrier gas (reactant input regime), second step is the dissociation of the metals from their alkyls inside the reactor (reactant mixing regime), third step involves the diffusion of reactants to a substrate (boundary layer regime), and the final step is the epitaxial growth of films on a hot substrate (growth surface regime). Figure 3.2 shows these four regimes in the MOCVD reactor as well as the velocity profile of the gas stream at the surface of the susceptor. Next to the substrate, there exists a region called

Figure 3.2 Four regimes in the MOCVD reactor; including the boundary layer over the substrate surface.

boundary layer, where the velocity is very low. The reactants reach the substrate by diffusing through the boundary layer, therefore, the reactant flux density arriving at the substrate surface is inversely proportional to the boundary thickness as indicated by the following equation:[4]

$$J = \frac{D (n_g - n_s)}{y}, \quad (3.4)$$

where J is the reactant flux, n_g and n_s are the gas stream and surface reactant concentrations, respectively, D is the gas phase diffusivity which is a function of temperature and pressure, y is the boundary layer thickness.

The fundamental growth processes are divided into mass transport control and kinetic (reaction rate) limited mechanisms. A study of the dependence of a macroscopic quantity, such as growth rate, gives the first insight into the overall growth mechanism. When the reaction rate limits the growth process, increasing temperature will result in an increase in the growth rate. When the growth process is limited either by the amount of reactant reaching the wafer surface or by the reaction product diffusing away, the process is mass transport or diffusion limited. The growth rate is linearly related the partial pressure of the reactant in the carrier gas and is nearly independent of the substrate temperature, since the diffusion process has a very small activation energy. Other factors, such as substrate orientation, total flow rate, and chamber geometry also determine the growth process.

Sources used in MOCVD are various combinations of organometallic compounds and hydrides. The sources are introduced as vapor phase constituents into a reaction chamber and are thermally decomposed at elevated temperatures by a hot susceptor and substrate to form the desired films. The reaction chamber walls are not deliberately heated (a "cold wall" process). The general overall chemical reaction that occurs during the MOCVD process can be written as:

where R and R' are the organic radicals, M is a group II or III metal, and X is a group V or VI element. The vapor reactants R_nM and R'_mX are thermally decomposed at elevated temperatures to form the nonvolatile product MX, which is deposited on the substrate and the volatile products RH and R'H are flushed by the H_2 gas into the exhaust. The growth temperature for the III-V materials generally range from 550°C to 900°C, while the typical growth temperature for the II-VI compound are in the range of 350°C to 450°C. The low temperature is highly desirable because of the large diffusion coefficients in the II-VI materials, and because a significant decrease in native defect concentration can be realized at low temperature [5].

The MOCVD process used for the growth of CdTe in this study involves the reaction between Dimethylcadmium (DMCd) and Diisopropyltellurium (DIPTe), which can be written as

Polycrystalline CdTe films were grown in a Cambridge MR102 MOCVD system. This system is fully computer controlled. The desired temperature, flow rate of metalorganic source, process time and sequences can be programmed and the growth sequences can be executed automatically. The growth chamber has a horizontal configuration. Substrates were supported on a silicon carbide coated graphite susceptor, which was heated externally by an RF generator. The substrate temperature was monitored by a thermocouple inserted into the susceptor. The Pd-purified hydrogen carrier gas flow was adjusted at 2.0 l/min during the growth process. The procedure for CdTe MOCVD growth is summarized below:

- (a) CdS/SnO₂/glass substrate is cleaned in hot isopropyl alcohol for 10 minutes.
- (b) The sample is loaded in the growth chamber, and purge with H₂ for 5-10 min before the RF heating.
- (c) The substrate is heated to 450°C, and maintained at this temperature for 15 min in H₂ ambient. The purpose of this pre-heat treatment is to remove the oxygen in the CdS, which is known to be a detrimental recombination center [6].
- (d) The temperature is then reduced to 400°C to grow CdTe film.
- (e) The H₂ gas is introduced into DMCd and DIPTe source cylinders respectively. This carrier gas is directed through the bypass (vent) manifold leading to the exhaust for 2 min

to purge the tubing and balance the gas flow.

(f) The carrier gas with DMCD and DIPTe reactants is then introduced into the chamber to start the CdTe growth. The growth temperature is kept at 400°C and 250 torr reactor pressure for 70 min. For a typical CdTe growth run, the H₂ flow rate through DMCD and DIPTe cylinders was set at 20 and 400 c.c./min, respectively, with cylinder temperature of 0°C and 20°C, respectively. This growth condition gives rise to a Te/Cd mole ratio of 6 in the growth ambient. An attempt has been made to vary the Te/Cd ratio in the growth ambient in the range of 0.02 to 15 by controlling the flow rates and the temperatures of the sources, which will be discussed in Chapter V.

(g) When the growth cycle is completed, the sample is cooled in the chamber with the continuous flow of H₂ gas until the temperature below 90°C is reached.

3.2.3 CdTe/CdS Solar Cell Fabrication

After the CdTe film growth on the CdS/SnO₂/glass substrate, solar cells were fabricated and tested. The process steps, after the CdTe deposition by MOCVD, are described below:

(a) Several drops of CdCl₂·CH₃OH solution were poured on the CdTe surface and then the sample was placed on a hot plate to dry, leaving a thin CdCl₂ film on the CdTe surface.

- (b) CdTe/CdS structures were annealed in a furnace at 400°C for 30 minutes in breathing air ambient.
- (c) The CdCl₂ residue on the sample was removed by a DI water rinse and N₂ blow-dry.
- (d) Ohmic back contacts were formed on the CdTe surface by sequential evaporation of 100 Å Cu and 400 Å Au.
- (e) After metalization, a contact anneal was performed at 150°C in Ar ambient for 90 min.
- (f) Cell fabrication was completed by a 0.1% Br₂:CH₃OH etch, followed by a DI water rinse and N₂ blow-dry.

The finished CdTe solar cell structure consists of Au/Cu/CdTe/CdS/SnO₂/glass. Steps (a) and (b), collectively referred to as CdCl₂ treatment, were performed to promote the grain growth and improve the cell performance [7]. The Br₂:CH₃OH etch in step (f) after the metalization and 150°C anneal gave more reproducible results, because the Br₂:CH₃OH treatment removes the residual surface oxides underneath the Au/Cu region and increases V_{oc} by a chemical interaction at the grain boundaries.[8] Surface oxide formation during the annealing process at times degrades the cell performance, if the etching is performed before the metalization. A more detailed investigation of the beneficial and deleterious effects of the baseline process steps like CdCl₂ treatment is presented in Chapter V and VI in order to achieve high efficiency CdTe solar cells.

3.3. Materials Characterization

In order to investigate a material surface, one of three basic probes may be applied to the material: electron, ions, or photons. The analysis consists of measuring the surface response, using one of above three methods. Combination of the probes and analytical methods gives various experimental techniques which can be utilized to characterize a material. Altering the energy, mass, or character of these probes increases the variety of possible experimental methods even further. A number of textbooks [9-15] describe the surface analysis techniques in detail. This section discusses the techniques used in this research to characterize material quality, film composition, surface composition and chemistry, and CdTe/CdS interface properties of CdTe solar cells. These techniques include Scanning electron microscopy(SEM), Auger electron spectroscopy(AES), secondary ion mass spectroscopy(SIMS), and X-ray diffraction(XRD).

3.3.1 Scanning Electron Microscopy (SEM)

The scanning electron microscope (SEM) can reveal topographical image of a surface with clarity and details, and can resolve topographical details of less than 50 Å [10]. It uses lenses to form a demagnified image of the electron source. This fine probe of electrons is scanned across the sample, and signal arising from the electron-specimen interaction is detected, amplified, and used to modulate the intensity of a TV-like image

tube, which is scanned at the same rate as the electron probe. Because the detected secondary electrons can escape only from a very thin layer of the surface, the SEM technique has a surface sensitivity of about several monolayers.

The versatility of the scanning electron microscope for the study on material comes from the rich variety of interactions between the electron beam and the specimen. The interaction can be generally divided into two classes: (a) elastic events, which reflect the incident beam without significantly altering the energy, and (b) inelastic events, which result in a transfer of energy to the solid, leading to the generation of secondary electrons, Auger electrons, X-rays, electron-hole pairs, or lattice vibrations (phonons). In principle, all of these interactions can be used to derive information about the specimen, including shape, composition, crystal structure, electronic structure, etc. A typical SEM image is constructed from the detection of either secondary electrons or backscattered electrons. The technique for detection and analysis of the generated Auger electrons is called Auger electron spectroscopy (AES), which will be discussed in Section 3.3.2. Energy-dispersive X-ray spectrometer (EDX) is utilized to analyze the induced X-rays, while the electron beam induced current (EBIC) technique is based on the detection of current collected from the generated electron-hole pairs.

The essential elements of an SEM are shown schematically in Figure 3.3. The electron path and sample chamber are evacuated. The electron gun, usually fitted with

IMAGE FORMING IN THE SEM

Figure 3.3 Schematic diagram of a SEM system (after ref. 10).

W or LaB₆ filament, operates over the accelerating voltage range of 0.5-40keV. A condenser lens produces a demagnified image of the source, which in turn is imaged by the probe forming lens (objective lens) onto the specimen. Scanning coils deflect the probe over a rectangular raster on the sample. The size of rectangle is relative to the display screen and determine the magnification. Detectors collect the emitted electron signals, which can be used to modulate the intensity of the beam of the display video screen after suitable amplification.

In this research, a Hitachi S-800 SEM system was utilized to investigate the CdTe/CdS structure in order to (a) observe the changes in the microstructure and grain size of polycrystalline CdTe layers after various chemical and heat treatments to correlate the structure to the device performance; and to (b) determine the crystallinity of the CdTe films grown under different substrates and growth conditions. A beam voltage of 15-19 kV with a beam current of 10 pA was used in the SEM measurements.

3.3.2 Auger Electron Spectroscopy (AES)

Auger electron spectroscopy (AES) is a well-known UHV technique for performing elemental identification and chemical analysis of the surfaces. In addition, if combined with a carefully controlled sputtering system, AES can be used for depth-profiling. The AES technique has a surface sensitivity of about 3 monolayers (due to the

high degree of inelastic scattering of Auger electrons which limits the Auger electron escape depth) and an elemental sensitivity of $\sim 0.3\%$ [11]. The various applications and principles of AES are extensively documented in the literature [11,12].

The origin and nature of the Auger process can be understood from a diagram of the electron energy levels in Figure 3.4a. The incident electron ejects an electron from an atom in the solid, leaving a hole in one of the atomic core levels. This core level is quickly filled by an electron from a higher level shell, and energy is released. This energy can leave the atom in the form of an X-ray, or there can be a competing process where another electron gains the energy, and is ejected from the atom. This second ejected electron is called Auger electron, and its energy depends on the energy of the atomic levels involved in its production, not on the energy of the initial ionizing radiation. The energy of the Auger electrons can therefore be used for elemental analysis. Only H and He do not give rise to Auger electrons as the process needs at least three electrons.

The energy of the Auger electron emitted from a solid surface is largely determined by the binding energies of the atomic energy levels in the participating atom. The Auger electron energy can be written as:[9]

$$E_{Auger} = E_x - E_y - E_z - U_{eff} ,$$

where E_x , E_y , E_z are the binding energies of the three participating electrons. The term U_{eff} represents the extra energy needed to remove an electron from a doubly ionized atom,

Figure 3.4 (a) Auger Electron Generation Process and (b) Energy distribution of scattering electrons from a solid surface (after ref. 9).

and the dynamic relaxation of the electrons during the two electron emission process.

In the routine analysis of materials, it is usually not necessary to understand the origin of the Auger transitions in details, as the major Auger energies are tabulated and presented in standard spectra in reference handbooks [16]. These reference spectra are very useful for the initial interpretation of unknown Auger spectra. However, chemical effects can change both the shape, relative intensity, and energy of Auger transitions.

The energy distribution of electrons from a sample under excitation by a primary electron beam is shown in Figure 3.4b. At the high energy side there are the reflected (elastically backscattered) primary electrons. Just to the low energy side of this peak are the primary electrons that have suffered small energy losses near the surface. Below the loss electrons is a long tail of high energy electrons that have lost energy in multiple collisions. Superimposed on this distribution of rediffused primary electrons, are features due to Auger electrons. Below each Auger line is a tail of Auger electrons from deeper in the solid that have lost energy before being emitted. Finally, at the lowest energies are the secondary electrons which are ejected from the valence and conduction bands. The energies of the Auger electrons used for surface spectroscopy are in the range 20-2000 eV. Electrons in this energy can travel only a few monolayers in a solid before losing energy. Therefore Auger spectroscopy is very surface sensitive.

Since the Auger peaks are superimposed on a rather large continuous background,

they are more easily detected by differentiating the energy distribution function $N(E)$. Thus the conventional Auger spectrum is the function $dN(E)/dE$ in order to suppress the background and enhance the Auger peak. Figure 3.5 shows examples of differentiated Auger spectra for Cd and Te elements.

Auger electron spectroscopy consists of an ultrahigh vacuum system, an electron gun for specimen excitation, and an energy analyzer for detection of Auger electron peaks in the total electron distribution. For an AES system, two most popular analyzer designs are the cylindrical mirror analyzer (CMA), and the concentric hemispherical analyzer (CHA).

The CMA analyzer was used for AES measurement in this research. It consists of two concentric cylinders, the inner cylinder at ground, and the outer cylinder at a negative voltage. Electrons entering the analyzer at 42° from the axis, and will be focused through the analyzer if they have the correct energy. The pass energy is scanned by ramping the outer cylinder voltage. CMA is typically used to analyze the emitted energy spectrum because of its large solid angle of acceptance for electrons which improves the signal to noise ratio of the spectrum. This is critical for AES since a large background of secondary electrons is present (Figure 3.4b). The wide acceptance angle penalizes the absolute energy resolution of the analyzer which is typically 1-2 eV [12]. However, this is not critical in AES because the Auger peak features are typically several

Figure 3.5 A typical differentiated Auger spectrum for (a) Cd and (b) Te element (after ref. 16).

electron volts wide. CMAs normally have an electron gun inside the inner cylinder so that the instrument is very compact.

The sensitivity of the Auger technique is determined by the transition probability of the Auger transitions involved, the incident beam current and energy, and by the collection efficiency of the analyzer. Detailed discussion of energy analyzers, resolution, etc., can be found in the book by Briggs and Seah [11], and is beyond the scope of this study.

In addition to surface analysis and element identification, AES can also be used in conjunction with ion sputtering in order to obtain depth profiles of elemental distribution in thin films. Depth profiling uses an ion beam to sputter the specimen surface layer by layer. Only the top few monolayers that have been exposed by the ion beam are analyzed due to the surface sensitivity of AES, and as the ion beam erodes the sample, the intensity of Auger signal at different depth can be obtained. This gives an intensity profile as a function of time. With the knowledge of the sputtering rate and the elemental sensitivity, this can be converted into concentrations with depth. This is widely used in the semiconductor industry to investigate atomic distribution in various layers and the interdiffusion between layers.

In this study, surface as well as depth-resolved AES measurements were performed to (a) determine compositional changes of MOCVD-grown CdTe films with

different Te/Cd mole ratios in the growth ambient; and to (b) study interdiffusion between CdS and CdTe interface as a function of various growth conditions and heat treatments employed during the solar cell fabrication. This was particularly useful in understanding correlations between interface defects, interdiffusion, and cell performance. In this research, a Physical Electronics Model 600 Scanning Auger Multiprobe system was used. The analysis chamber was pumped down to a background pressure of less than 1×10^{-8} torr. Samples were loaded directly from atmosphere. The angle between the sample normal and the incident electron beam was 45° . All Auger data were taken using a 3 keV primary electron beam energy with a current of 1 μA . Sputtering for depth profiling measurements was done using a normally incident 4 keV Ar ion beam with a current density of 50 $\mu\text{A}/\text{cm}^2$.

3.3.3 Secondary Ion Mass Spectroscopy (SIMS)

SIMS is the mass spectrometry of ionized particles which are emitted when a surface is bombarded by energetic primary particles. Primary ions of energy 0.5-20 keV, commonly O^+ , Cs^+ , Xe^+ , Ar^+ , Ga^+ , and O_2^+ , are used to erode the sample surface. Cs^+ is typically used for the detection of electronegative species, while O_2^+ is used for the electropositive species [15]. The emitted (so-called "secondary") particles are detected by a mass spectrometer. It provides a mass spectrum of a surface and enables a detailed

chemical analysis of material. SIMS information may be presented in three ways. First, secondary ion intensities may be collected as a mass spectrum which represents the top monolayer of the surface. Secondly, the secondary ion from selected elements may be monitored as a function of sputter time when the primary ion beam erodes into the sample. A profile of the target elemental concentrations can be obtained as a function of depth into the target. Thirdly, the secondary ion signals may be presented as a function of position on the surface to show the element distribution maps.

The main advantages of SIMS are: (a) SIMS is probably the most sensitive technique currently available for composition analysis with detection limit in the range of 10^{13} - 10^{18} cm⁻³ for impurities in semiconductors; and (b) It can distinguish different isotopes of the same element. The primary disadvantages are: (a) Detection sensitivity could vary over orders of magnitude for different elements in one substrate and for the same element in different substrates; and (b) The alteration of the target by radiation-induced processes during dynamic SIMS measurements. These include ion-beam-induced intermixing of target elements, radiation induced segregation, surface topography changes and redeposition of other material into the analyzed region.

The key components of a SIMS analyzer include (a) a primary ion source, (b) optics to transfer these ions to the target surface, (c) optics to collect secondary ions from the surface and direct them to (d) a mass spectrometer. The mass spectrometer is very

important in affecting the resolution and sensitivity of a SIMS system. There are three different types of mass spectrometer, quadrupole, magnetic sector, and time-of-flight [14]. The quadrupole analyzer is utilized for the SIMS analysis in this research.

In an quadrupole analyzer, low energy (<50eV) secondary ions travel down through the center of four circular rods which are electrically connected in opposite pairs. A combination of dc and RF (~1MHz) voltages is applied to one set of rods and an equal but opposite combination is applied to the other pair. Only ions of a certain M/Z ratio, where the ion charge q is given by $q = Ze$ with e the electronic charge, have a stable trajectory and are transmitted through the quadrupole. Ions of different M/Z ratios move in unstable trajectories and strike the rods or apertures. The mass of the transmitted ion is selected by increasing the RF and dc voltages while keeping their ratio constant. Only one M/Z ratio may be transmitted at any one time. Mass analysis of many elements must therefore be performed sequentially. The mass resolution, $M/\Delta M$ of the quadrupole is normally about 1000 over a restricted mass range. This resolution can be increased by using larger diameter rods at the expense of a lower obtainable mass range. Transmissions of the order of 1% and mass analyzes up to $M/Z \sim 2000$ are typical for quadrupoles [17].

SIMS is a technique which requires careful calibration if quantitative data are to be obtained. Two principal methods for elemental quantification by SIMS involve (a) the

use of ion implanted standard with accurately known fluences, and (b) the use of bulk samples doped to accurately known atom density. The atom density can be estimated by using a relative sensitivity factor (RSF), which is defined as a conversion factor from secondary ion intensity to atom density by the equation:[15]

$$RSF = \rho_i \frac{I_m}{I_i} , \quad (3.8)$$

where ρ_i is the impurity atom density in atoms/cm³, I_i is the impurity ion signal in counts/sec from SIMS, and I_m is the matrix ion signal. By using the tabulated RSF values for some species of interest in a given material (matrix)[15], the rough estimation of impurity atom density can be obtained from Equation (3.8).

In this research, depth distribution of Cu, Au, S, Cd, and Te through various layers of CdTe cell was monitored by depth profiling with an ATOMIKA-ADIDA 3500 SIMS system using a quadrupole mass spectrometers. Profiling was done with a 40 nA, 12 keV O₂⁺ beam. The beam was generally rastered over a 600 micron square area when profiling through the region of contact/CdTe interface and then the raster area was reduced to 200 micron square for a faster profile through the much thicker CdTe/CdS layers. Signals of the monoatomic ions were recorded. Detection was only from the central 30% of the rastered area in order to avoid crater edge effects.

3.3.4 X-ray Diffraction(XRD)

X-ray diffraction (XRD) technique analyzes the relations between the angular position and intensity of X-ray beam diffracted by material to provide the information about the crystal structure of the material. This technique depends on establishing conditions that satisfy the Bragg requirement for the diffraction of X-ray by a crystal lattice:

$$n\lambda = 2d \sin\theta \quad . \quad (3.9)$$

Bragg's law can be easily derived with the aid of Figure 3.6a. A beam of coherent (in-phase) X-rays with wavelength λ is specularly reflected from parallel crystal planes spaced d units apart. Of the two X-ray beams shown in Figure 3.6a, the lower one will travel an additional path length $ABC = 2d \sin\theta$ prior to leaving the crystal. If this distance equals an integral number of wavelengths $n\lambda$, then the reflected beams will combine in phase and an intensity maximum will be detected by the proportional counter. If measured with a high-quality detector, the intensity distribution resulting from the diffraction phenomenon can be relatively narrow.

An X-ray diffractometer is usually utilized to give the information on the crystal structure. A monochromatic X-ray beam strikes the film surface at an angle θ . The sample is slowly rotated and while the detector moves simultaneously, at twice the rate, along the circumference of a circle with the same center as the sample trajectory. Diffraction maxima appear whenever θ coincides with a Bragg angle. A measure of 2θ

Figure 3.6 Bragg Diffraction Schematic diagram.

is used to identify the interplanar spacing (d value) of the crystalline material giving rise to those peaks.

The lattice size and shape determine the direction of the diffracted beams according to the Bragg's law, however, other factors affect the intensity of each diffracted beams. These factors include lattice structure, multiplicity and geometrical factor. The structure factor $|F|$ affects the intensity of each diffracted beam. This can be explained by considering (001) planes in a body-center lattice shown in Figure 3.6b. If the path difference ABC is one wavelength, rays 1' and 2' are in phase and diffraction could occur in this direction. However, there is another plane of atom midway between the (001) plane, and the path difference DEF between rays 1' and 3' is exactly half of ABC, or one half wavelength. Thus, rays 1' and 3' are completely out of phase and cancel each other. Similarly, ray from the next plane down cancel the ray 2', and so on throughout the crystal. Therefore, there is no {001} reflection peak for the body-center lattice. When considering the scattering of X-ray by the electrons and atoms, the structure factor becomes more complicated. The details can be found in the textbook [18] and will not be discussed here.

The multiplicity factor p can be defined as the number of different planes having the same spacing. For example, in a simple cubic lattice, planes with $(\pm 1, 0, 0)$, $(0, \pm 1, 0)$ $(0, 0, \pm 1)$ direction have the same d spacing and Bragg angle, contributes to the same peak

intensity. Since the multiplicity factor p is six for the $\{100\}$ planes and eight for the $\{111\}$ planes. Therefore, the intensity of the 100 diffraction will be $\frac{3}{4}$ that of the 111 diffraction, if all other factors are the same.

The intensity of the collected X-ray signal also depend on the geometrical factor of the collection. For example, the refraction beam corresponding to a particular hkl and Bragg angle θ_B forms a band of width $r\Delta\theta$ on the surface of a sphere (Figure 3.7). The collection intensity depend on the area of the band, which varies with different θ_B . Different geometric factors are combined into one and is called the Lorentz factor in the following form:[18]

$$\frac{1 + \cos^2 2\theta}{\sin^2 \theta \cos \theta} \quad (3.10)$$

A value for the relative intensity of a powder (random orientation) diffraction pattern can be obtained by combining all the above factors. Each material with a particular lattice structure has its own relative intensity pattern, which can be found in textbooks [19]. Table 3.1 listed the standard diffraction patterns for the CdTe and CdS structure with the relative peak intensity at various Bragg angles. By comparing the standard pattern with the measured relative intensity for different $\{hkl\}$ directions, the preferred orientation of the material can be known.

In this research, X-ray diffraction (XRD) measurements were performed to study the orientation and crystallinity of CdTe layers grown on various growth substrates with

Figure 3.7 The collection intensity depend on the area of the band, which varies with different θ_B (after ref. 18).

Table 3.1 Standard X-ray diffraction parameters for power CdTe and CdS.

CdTe (Cubic structure, $a_0=6.481 \text{ \AA}$)				CdS (Cubic structure, $a_0=5.818 \text{ \AA}$)			
d ($\text{\AA}$)	$I/I_M(\%)$	h,k,l	2θ ($^\circ$)	d ($\text{\AA}$)	$I/I_M(\%)$	h,k,l	2θ ($^\circ$)
3.742	100	111	23.7	3.36	100	111	26.053
2.290	60	220	39.3	2.90	40	200	30.83
1.945	30	311	46.42	2.058	80	220	44.00
1.619	6	400	56.8	1.753	60	311	52.18
1.488	10	331	62.3	1.680	10	222	54.63
1.323	10	422	71.2	1.453	20	400	64.09
1.247	4	511	76.3	1.337	30	331	70.42
1.146	2	440	84.4	1.298	10	420	72.87
1.095	4	531	89.4	1.186	30	422	81.08
1.025	4	620	97.43	1.120	30	333 511	86.99
0.9884	2	533	102.39	1.028	5	440	97.16
0.9356	<1	444	110.83	0.985	20	531	103.01
0.9076	2	711	116.13	0.918	5	620	114.23
0.8661	4	642	125.58	0.887	5	533	120.71
0.8438	4	731	131.8				

The X-ray wavelength is $1.5418 \text{ \AA}$,

a_0 is the lattice constant,

d is the spacing between (h,k,l) plane,

I/I_M is the relative intensity of the {h,k,l} peak,

2θ is the angle where the {h,k,l} peak is located.

different growth conditions. The interdiffusion between CdTe and CdS was also investigated by comparing the peak location at a specific orientation angle in the XRD scan spectrum [8]. If S atoms diffuse into the CdTe lattice and form a $\text{CdTe}_{1-x}\text{S}_x$ interlayer, the lattice constant d would change and cause a shift in the Bragg angle or peak location in the X-ray spectrum. In this research, XRD measurements were performed by using a Phillips PW 1800 automatic diffractometer with $1.5418\text{\AA}$ Cu- K_α radiation. The diffraction angle 2θ was varied in the range of 20° to 70° at a scan step size of 0.03° and signal collection time was 1 sec at each step. The peak shift at {220} orientation was investigated using slower scan by changing the diffraction angle 2θ from 38.5° to 40.5° with step size of 0.015° and signal collection time of 7 sec at each step.

3.4. Device Characterization

Experimental techniques used to characterize device parameters, electrical, and optical properties such as cell efficiency, carrier transport mechanisms, surface reflectance, and carrier collection efficiency, are presented in this section.

3.4.1 Lighted Current-Voltage (I-V) Measurements

CdTe solar cell parameters were measured using a lighted J-V measurement stage and an automated data acquisition system. The voltage was applied on the device in the

range of -0.05 to 0.85 volt in a 0.05 volt increment, and the corresponding current was measured. After obtaining the light J-V curve of the solar cell, J_{sc} and V_{oc} values were acquired from J-V curve intersection with the current and voltage axis, respectively. R_s and R_{sh} were calculated from the slopes of the J-V curve at the V_{oc} and J_{sc} points, respectively. The maximum power output (V_m , J_m) was obtained by calculating the J-V product at each bias point and the fill factor was calculated by using Equation (2.3): $FF=(V_m \cdot J_m)/(V_{oc} \cdot J_{sc})$. All the cell data in this study was acquired at 300 K under simulated 100 mW/cm² AM1.5 conditions.

3.4.2 Current Density-Voltage-Temperature (J-V-T) Measurements

Current Density-Voltage-Temperature (J-V-T) measurements were performed to determine the dominant current transport mechanisms in CdTe/CdS heterojunctions and quantify the effects of process variables on current loss mechanisms. An automated J-V-T- measurement and data acquisition system was assembled and used in conjunction with a cryostat. A Keithley electrometer (model 617) was used for the J-V measurements which is capable of measuring currents down to 100 fA with the help of short and low-loss coaxial cables. A liquid nitrogen cooled cryostat with a dc computer controlled heater was used to control the sample temperature. Samples were placed within the cryostat, which was subsequently pumped down using a mechanical pump prior to

cooling. The samples were clamped to the stainless steel baseplate of the cryostat. Electrical contact to the device under test was supplied by the baseplate and a shielded coaxial spring-loaded contact probe. Samples were slowly cooled to the desired starting temperature and then the heater was turned on to start the J-V-T measurement. A slow heating rate was used to insure accurate temperature determination. To monitor the temperature of the thin film CdTe/CdS devices, which were grown on glass substrates, a thermocouple was clamped on top of a glass slide and placed adjacent to the sample in the cryostat chamber.

In order to determine the current transport mechanism in CdTe/CdS heterojunctions (discussed in Chapter II), forward biased J-V data (0 to 0.8 volt) was acquired in the temperature range of 220-300 K in 10 K increments. The J-V characteristic at each temperature was fitted to the following equivalent circuit model with shunt and series resistance,

$$J = J_1 + \frac{V - JR_s}{R_{SH}} , \quad (3.11)$$

where

$$J_1 = J_0 \left[\exp\left(\frac{q(V - JR_s)}{AkT}\right) - 1 \right] . \quad (3.12)$$

A multivariable regression analysis was used to fit the data until less than 5% average error over the fitted voltage range was obtained, and then the fitted values of J_0 , A , R_s ,

and R_{sh} were recorded for each temperature. The temperature dependence of these parameters was compared with the theory to determine the current transport mechanisms in each device as described in Chapter II. The following procedure was used to acquire the J-V-T data, fit the data to the diode equivalent circuit model, and determine the transport mechanisms:

- (a) Sample was loaded into cryostat and cooled to the desired temperature.
- (b) Sample was slowly heated to the desired measurement temperature.
- (c) J-V data was acquired automatically at the preselected temperature intervals, until the desired temperature is reached. Voltage was varied in the range of 0 to 0.8 volt forward bias with 0.05 volt increments. Notice that sample was heated very slowly so that the sample temperature changes less than 1°C during the J-V measurement at any temperature.
- (d) Data file was converted into a proper format for input to the J-V-T fitting routine.
- (e) Data was read into the fitting routine so that the lowest temperature J-V curve was analyzed first.
- (f) An appropriate voltage range was selected to avoid fitting over the region where current tends to saturate at higher bias voltages due to non-ohmic back contact, which was not included in the equivalent circuit model (Equation 3.11)
- (g) Data was fitted until an average fitting error of less than 5% with a maximum error

of less than 8% was obtained.

(h) The J-V curve at the next temperature was then analyzed using fitted parameters for the previous temperature as initial estimates.

(i) The process was repeated until J-V characteristics at all temperatures were fit to Equation (3.11).

(j) Fitting parameters, J_0 , A , R_s , R_{sh} , were tabulated as a function of temperature.

(k) Each parameter was plotted against T and $1000/T$ to separate thermally-activated and nonthermally-activated current transport mechanism.

(l) To determine detailed transport mechanism of each diode, the temperature and voltage dependence of the parameters was compared with the reported theoretical equations that describe various transport mechanisms, discussed in Chapter II. Further confirmation of the assigned transport mechanism was obtained by calculating physical constants using the theoretical transport equations by inserting the experimentally determined parameters from the J-V-T analysis into the equations. For example, if the $\ln(J_0 T^{2.5})$ vs $1000/T$ plot gives an activation energy of $E_g/2$, it reinforces the possibility of depletion region recombination controlled the transport mechanism (Section 2.4).

3.4.3 Quantum Efficiency Measurements

The spectral response (SR, unit of Amp/Watt) of a solar cell at a given wavelength

is defined as the short-circuit current per unit of incident power in the monochromatic light. It is also useful to define the external quantum efficiency (η_Q or QE) as the ratio of the current resulting from photogenerated carriers and the incident photon flux as a function of wavelength, which can be written as:[20]

$$\eta_Q(\lambda) = \frac{J_L(\lambda)}{qF(\lambda)} , \quad (3.13)$$

where $F(\lambda)$ is the incident photon flux and J_L is the photocurrent. If the photon loss due to the reflectance is excluded, the internal quantum efficiency (IQE) can be obtained by dividing the external QE by $(1-R(\lambda))$, where $R(\lambda)$ is the reflectivity of the cell at that wavelength. Also, the quantum efficiency can be calculated by multiplying the spectral response, SR, with the energy of photon (in eV) at each wavelength:

$$\begin{aligned} \eta_Q(\lambda) &= \frac{J_L(\lambda)}{qF(\lambda)} = \frac{q/\text{sec} \cdot \text{cm}^2}{q/\text{sec} \cdot \text{cm}^2} = \frac{\text{Amp}/\text{cm}^2}{q/\text{sec} \cdot \text{cm}^2 (\text{joul}/q)} \text{joul}/q \\ &= \frac{\text{Amp}}{\text{joul}/\text{sec}} \text{eV} = \frac{\text{Amp}}{\text{Watt}} \text{eV} = (\text{SR}) (\text{eV}) . \end{aligned} \quad (3.14)$$

Quantum efficiency measurements at various wavelength can provide useful information about the collection properties at different region of the solar cell structure. In addition, the bias-dependent QE measurement is useful in analyzing polycrystalline solar cells because the photocurrent in these cells is a function of bias voltage. The collection probability $h(V)$ of photon-generated carriers through the junction can be

approximated by Equation (2.2) in Section 2.2. Since the interface recombination velocity S is proportional to the interface defect density, higher defect density will result in poor carrier collection, and thus lower QE. The bias-dependent QE measurement can be utilized to investigate the CdTe/CdS interface quality of the CdTe cells.

The spectral response or quantum efficiency measurements involve measuring J_{sc} of the device as a function of λ , using a monochromator and the appropriate electronics. Since the incident power at each wavelength is known, with the help of a known detector, the external SR and QE can be obtained according to Equations (3.13) and (3.14). The internal SR and QE can also be calculated from the measured reflectance of the device at each wavelength. In this study, the external QE of CdTe solar cells was measured by an Optronics Laboratory model 746 phase-sensitive detection system (Figure 3.8a) in which the sample was illuminated through the glass substrate. The measurement system contains a light source, detector, lock-in amplifier, and monochromator. The automated system using computer control to change incident wavelength, acquire the data, and calculate the results. Monochromator contains a built in light chopper and a single grating. The light chopper modulates the light source to increase the signal to noise ratio of the detected current. Pre-calibrated Si detector with 1cm^2 area is used to measure incident light intensity. The bias- and light-dependent QE measurements were performed by connecting the sample as shown in Figure 3.8b. The purpose of this circuit is to

Figure 3.8 (a) An Optronics Laboratory system for QE measurements. (b) Circuit : diagram for light- and bias-dependent QE measurement.

maintain the dc current flow induced by the light or voltage bias, while filter this dc current before the signal is fed into the pre-amplifier. The bias voltage applied to the device was adjusted by a dc power supply. The external QE measurements on the CdTe/CdS solar cells were performed in the wavelength range of 400-900 nm, both without the light-bias and under 30% AM 1.5 illumination of light-bias.

3.4.4 Reflectance Measurements

The reflectance information $R(\lambda)$ from a solar cell is important in order to get an accurate value of the internal quantum efficiency. In addition, anti-reflection (AR) coating is usually deposited on the cell surface to reduce the reflectivity, therefore, the reflectance measurement is also important to evaluate the effectiveness of the AR coating. An integrating sphere was used for accurate reflectance measurement in order to reduce the errors due to flux losses [21] and the scattered from the polycrystalline cell structure. The scattering results from the rough surface and interfaces due to the polycrystalline structure and textured SnO_2 surface. The reflectance measurements were performed using the Optronics Laboratory model 746 set-up mentioned in the previous section, with attached model 704-70 integrating sphere (Figure 3.9).

In addition to the light input and detector ports, the integrating sphere has a test sample and a comparison sample port. Along with the test device, two samples of BaSO_4

Figure 3.9 Schematic diagram of a integrating sphere for reflectance measurements.

powder pressed into a holder are used for a comparison sample and standard reflectance sample. The reflectance $R(\lambda)$ for BaSO_4 powder is known. When the standard is replaced by the test sample, slight change in the efficiency of the integrating sphere could occur. Any variation in the sphere efficiency can cause error in the overall reflectance measurement. Therefore, four scans, including two calibration and two test sample scans, are performed for the accurate reflectance measurement. Each scan is performed in the wavelength range of 400-900 nm at 10 nm interval. The calibration scans are made with the comparison sample and the standard reflectance sample (both contain BaSO_4 powder), one in each of the two sample ports. The first calibration scan is made with the beam switched to the comparison position such that the input beam is focused on the comparison sample. The second calibration scan is made with the beam switched to the sample position. The ratio of these two scan values, S_{cs} and S_s can be written as:

$$\frac{S_s}{S_{cs}} = \frac{(K_{cs} P_s R_s)}{(K_{cs} P_c R_c)} , \quad (3.15)$$

where K_{cs} represents the sphere efficiency with the comparison and standard samples in place, P_c and P_s are the comparison and sample input beam flux, and R_c and R_s are the reflectance of the comparison and standard samples, respectively. Notice that K_{cs} will be cancelled by taking the ratio of S_{cs} and S_s . The next two scans are made by substituting the test sample (CdTe sample) for the standard sample, with the comparison sample

unchanged. Similar to the first and second scan, the third and fourth scans are made with beam incident on the comparison and test samples, respectively. These two measurements give:

$$\frac{S_t}{S_{ct}} = \frac{(K_{ct}P_sR_t)}{(K_{ct}P_cR_c)} , \quad (3.16)$$

where K_{ct} is the sphere efficiency with the comparison and test samples in place, P_c and P_s are defined in Equation (3.15), and R_c and R_t represents the reflectance of the comparison and test sample, respectively. Combining Equation (3.15) and (3.16), and recognizing that the effect of input beam, P_s and P_c , are cancelled out, the reflectance of the test sample can be obtained by:

$$R_t = R_s \left(\frac{S_{cs}}{S_s} \right) \left(\frac{S_t}{S_{ct}} \right) . \quad (3.17)$$

Since R_s , the reflectance of standard sample (BaSO_4), is known, the reflectance of the CdTe cell (R_t) can be obtained.

CHAPTER IV

ANALYSIS OF PHOTOCURRENT LOSS FROM REFLECTANCE AND ABSORPTION IN CdS AND SnO₂ LAYERS

4.1 Introduction

Current polycrystalline CdTe/CdS thin film solar cell efficiencies are in the range of 10-15%, even though the practically achievable efficiency limit is 18% [1,2]. Unlike Si, GaAs, and InP solar cells, very limited research has been conducted to minimize the reflectance loss in the CdTe/CdS heterojunction devices. Typical CdTe solar cell structure consists of glass/SnO₂/CdS/CdTe/Cu/Au structure in which n-type CdS forms a p-n junction with p-type CdTe, and the SnO₂ coating is used to form ohmic contact to CdS. Since the light enters through the glass surface, CdS/SnO₂ layers between the glass and the CdTe could affect the reflectance of the CdTe cells. Additionally, absorption in the CdS dead layer contributes to loss of photocurrent. Recently, it was shown that the reduction of CdS thickness [3] and the use of anti-reflective coating on glass [4] can result in substantial increase in short circuit current density of the CdTe cells. However, no systematic study or analysis has been conducted to optimize the CdS, SnO₂, and AR coating thicknesses to maximize the CdTe solar cell performance. Therefore, the

objective of this chapter is to tailor and optimize the thickness of CdS, SnO₂, and AR coating on glass to minimize the reflectance and photocurrent loss in the CdTe solar cells by a combination of modelling and selected experiments, which involve cell fabrication and testing.

4.2 Simulation of Current Loss from Reflectance and Absorption

Reflectance measurements were made as a function of wavelength by illuminating the cell from the glass side, using an integrating sphere set-up and an Optronics Laboratory phase-sensitive detection system, described in Section 3.4.4. The reflectance was modeled as a function of wavelength λ by utilizing the CAMS packaged program, written by Optikos Corporation. This program can evaluate and optimize the reflectance of multilayer structures as a function of λ and incident angles. In the simulation, the glass material was assumed to be totally transparent without any interference from the interior of the glass. Therefore, the reflectance from the air/glass interface and glass/SnO₂/CdS/CdTe can be calculated independently. After obtaining the reflectance, $R(\lambda)$, from the simulation, the corresponding photocurrent loss (J_R) was calculated by summation the product of $R(\lambda)$ and global spectrum flux $F(\lambda)$ in the wavelength range of 4000 Å to 9000 Å, assuming 100% internal quantum efficiency and recognizing that the band edge of CdTe corresponds to $\lambda=9000\text{\AA}$:

$$J_{R \text{ loss}} = \sum_{\lambda=4000}^{\lambda=9000} R(\lambda) \times q \times F(\lambda). \quad (4.1)$$

The photocurrent loss due to the absorption (J_A) in the CdS layer was calculated by

$$J_{A \text{ loss}} = \sum_{\lambda=4000}^{\lambda=5100} (1 - e^{-\alpha(\lambda) \times d}) \times q \times F(\lambda), \quad (4.2)$$

where d is the thickness of CdS layer, $\alpha(\lambda)$ is the absorption coefficient of the CdS film [5], and the band edge of CdS corresponds to $\lambda=5100\text{\AA}$.

4.3 Theory and Modeling of Reflectance

For a single film with a refractive index of n_1 and thickness d_1 on a substrate, the minimum reflectance occurs at wavelength λ when $n_1 d_1 = \lambda/4$ and the corresponding minimum reflectance value is given by [6]

$$R_{\min} = \left(\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2} \right)^2, \quad (4.3)$$

where n_s and n_0 represent the refractive index of the substrate and surrounding ambient, respectively.

Two layer AR coating can reduce the reflectance further. This can be accomplished either by a narrow-band, single-minimum (V-coating) or by a broad-band, double-minima (W-coating) in the reflectance curve.

The reflectance of a two layer coating is given by [7]

$$R = \frac{X}{1+X}, \quad (4.4)$$

where

$$X = \frac{n_s}{4n_M} \left\{ \left[\left(\frac{n_M}{n_s} - 1 \right) \cos\phi_1 \cos\phi_2 + \left(\frac{n_1}{n_2} - \frac{n_M n_2}{n_s n_1} \right) \sin\phi_1 \sin\phi_2 \right]^2 + \left[\left(\frac{n_M}{n_1} - \frac{n_1}{n_s} \right) \sin\phi_1 \cos\phi_2 + \left(\frac{n_M}{n_2} - \frac{n_2}{n_s} \right) \cos\phi_1 \sin\phi_2 \right]^2 \right\}, \quad (4.5)$$

and n_1 is the refractive index of the film next to the surrounding medium (n_M), n_2 is the refractive index of the film next to the substrate (n_s), $\phi_1 = 2\pi n_1 d_1 / \lambda$, and $\phi_2 = 2\pi n_2 d_2 / \lambda$.

For the V-coating, the values of R and X are set to zero to realize single minimum, which leads to

$$\tan^2 \phi_1 = n_1^2 \frac{(n_M - n_s)(n_s n_M - n_2^2)}{(n_s n_1^2 - n_M n_2^2)(n_s n_M - n_1^2)}, \quad (4.6)$$

and

$$\tan^2 \phi_2 = n_2^2 \frac{(n_M - n_s)(n_s n_M - n_1^2)}{(n_s n_1^2 - n_M n_2^2)(n_s n_M - n_2^2)}. \quad (4.7)$$

The film thicknesses d_1 and d_2 for zero reflectance at a desired wavelength could be obtained from the above two equations. For the double minima W-type coating, a half

wave thick film ($n_2d_2 = \frac{1}{2}\lambda$) is inserted between a quarter wave thick top layer ($n_1d_1 = \frac{1}{4}\lambda$) and the substrate in order to get broad reflectance spectrum with two minima [8].

4.4 Results and Discussion

4.4.1 Theoretical Optimization of CdS and SnO₂ Thicknesses for Minimum Reflectance

Since CdS and SnO₂ films act as double-layer coating between the glass and CdTe material in the glass/SnO₂/CdS/CdTe cell structure, detailed model calculation was performed to investigate how their thickness affect the reflectance of the device. In order to achieve the single minimum V-type reflectivity, the optimum thicknesses of the CdS and SnO₂ were determined from Equations (4.6) and (4.7) by substituting the appropriate refractive index values, $n_M = 1.5$ (glass), $n_1 = 1.8$ (SnO₂), $n_2 = 2.5$ (CdS), and $n_s = 2.9$ (CdTe) [9,10], which gave

$$\phi_1 = \frac{2\pi n_1 d_1}{\lambda} = 1.519 + \frac{k\pi}{2}, \quad \phi_2 = \frac{2\pi n_2 d_2}{\lambda} = 0.24 + \frac{k\pi}{2}, \quad (4.8)$$

where k is an integer. If 6000 Å is selected to be the target wavelength (near the solar spectrum peak) for the single minimum, the SnO₂ thickness d_1 should be 805.8 Å with the corresponding CdS thickness d_2 of 575.6 Å. As mentioned previously, double minima (W-type) reflectance could be achieved by choosing half wavelength thick CdS ($n_2d_2 =$

$1/2 \lambda$, $d_2=1200 \text{ \AA}$) in conjunction with quarter wavelength thick SnO_2 ($n_1 d_1 = 1/4 \lambda$, $d_2=1666 \text{ \AA}$). However, these theoretically calculated optimum thicknesses of CdS and SnO_2 for minimum reflectance may not be fully compatible with the requirements of high-efficiency solar cells. For example, SnO_2 should be sufficiently thick ($\gg 800 \text{ \AA}$) to prevent power loss associated with series resistance, which can degrade fill factor and cell performance; and the CdS thickness must be sufficient ($\geq 600 \text{ \AA}$) to ensure uniformity and prevent the formation of pin-holes, which can result in low shunt resistance or fill factor. On the other hand, if the CdS film is too thick, then the absorption could lower the J_{sc} and cell efficiency. Therefore, further reflectance simulations and measurements were performed on glass/ SnO_2 /CdS/CdTe cells to determine what combination(s) of the SnO_2 and CdS thicknesses can minimize reflectance and absorption losses, while maintaining the requirements for high-efficiency cells, namely low series resistance and reduced pin-hole density.

4.4.2 Practical Optimization of CdS Thickness Including Reflectance, Absorption, and Other Requirements for High Efficiency Cells

Thick SnO_2 layers are necessary to reduce series resistance of CdTe cells, therefore, simulations were performed by fixing the SnO_2 thickness at $10000 \text{ \AA}$ and varying the CdS thickness in the range of $100 \text{ \AA}$ to $3000 \text{ \AA}$. The corresponding

photocurrent loss resulting from the reflectance (J_R) was calculated for each CdS thickness (Figure 4.1a) by using Equation (4.1) and the simulated reflectance $R(\lambda)$. It is important to recognize that a number of investigators use about 10000 Å SnO₂ to lower R_s and CdS thickness in excess of 1000 Å to avoid pin-hole problems. Figure 4.1a shows that reducing the CdS thickness from 1500 Å to 600 Å reduces photocurrent loss by 0.77 mA/cm² (2.74 mA/cm² as opposed to 1.97 mA/cm²) resulting from reduced reflectance alone, without accounting for the absorption. In order to support the above prediction, CdTe solar cells were fabricated with 650 Å and 1600 Å thick CdS layers and their reflectance was measured. Experimental data in Figure 4.2 clearly indicates that the reflectance of the cell with 1600 Å CdS is much higher than the one with 650 Å CdS. Measured reflectance was utilized to calculate the photocurrent loss by using Equation (4.1). Reflectance-induced current loss in the cell with 1600 Å thick CdS was found to be 0.5 mA/cm² higher than the cell with 650 Å thick CdS.

Figure 4.1a shows that the current loss due to reflectance is more sensitive to the CdS film when the thickness falls below 1500 Å. This is important because generally the CdS thickness is decreased in order to reduce the photon absorption loss but the contribution from the change in reflectance can not be ignored. For example, Figure 4.1 shows that decreasing the CdS thickness to 600 Å reduces reflectance as well as absorption losses. However, the reduction in CdS thickness below 600 Å decreases the

Figure 4.1 Photocurrent loss in CdTe solar cells due to the absorption in CdS window layer and the reflection with varying CdS thicknesses.

Figure 4.2 Measured reflectance for CdTe/CdS solar cells with different CdS thicknesses.

photon absorption in the CdS layer, which should improve J_{sc} , but it also increases the reflectance, which should reduce J_{sc} . In order to understand and quantify the competition between absorption and reflectance losses, the photocurrent loss from the reflectance (Figure 4.1a) and absorption (Figure 4.1b) were calculated for the CdS layer thickness in the range of 100 Å to 3000 Å. It is clear that the current loss from the absorption is dominant and decreases rapidly with the decrease in the CdS thickness. It is interesting to note that the decrease in the CdS thickness from 1500 Å to 600 Å reduces both absorption and reflectance, resulting in a steep reduction in photocurrent loss. However, further decrease in the CdS thickness below 600 Å introduces an additional photocurrent loss from the increased reflectance, which slows down the rate of decrease in the photocurrent loss. Besides, reducing the CdS thickness below 600 Å in a real cell may be risky because of the possibility of pin-holes in very thin CdS films, which can cause low shunt resistance and degrade V_{oc} and fill factor [11,12].

In order to study the effect of the CdS thickness on the CdTe cell performance, CdTe solar cells with 650 Å and 1600 Å thick CdS layers were fabricated and tested (Table 4.1). It was found that when the CdS thickness was lowered from 1600 Å to 650 Å, the J_{sc} increased by about 1.4 mA/cm² resulting from the combination of reduced reflectance (Figure 4.2) and absorption in the CdS layer. Notice that the measured increase in J_{sc} (1.4 mA/cm²) is lower than the predicted value of 3 mA/cm² in Figure 4.1c.

Table 4.1 Solar cell data for the CdTe/CdS cells grown with different CdS thicknesses

CdS thickness	V_{oc} (mV)	J_{sc} (mA/cm ²)	R_s (Ω -cm ²)	R_{sh} (Ω -cm ²)	Fill factor	Eff (%)
650 Å	710	25.01	6.12	556	0.55	9.80
1600 Å	740	23.58	4.17	1108	0.61	10.62

This is because in our cells when we try to thin the CdS layer below 1000 Å, some of the photo-generated carriers are lost because of low shunt resistance or pin-hole induced recombination. The lower values of shunt resistance, fill factor, and V_{oc} of the CdTe cell with 650 Å CdS in Table 4.1 supports the above conclusion. The reduction in the CdS thickness below 600 Å is expected to cause even more pin-holes and non-uniformity problems, and may not result in a significant current gain because of the increased reflectance. Therefore, even though from the theoretical viewpoint, the CdS thickness should be as small as possible, the practical optimum CdS thickness seems to be about 600-700 Å for achieving high J_{sc} and efficiency in the CdTe solar cells. The above guidelines match the structure of the highest efficiency (15.8 %) CdTe solar cell today which consists of about 700 Å thick CdS layer [12]. It should be recognized that the practical optimum CdS thickness could be a function of CdS film quality, because higher pin-hole density will require thicker CdS films.

4.4.3 Effect of SnO_2 Thickness on Photocurrent Loss

Two additional sets of simulations were performed by fixing the CdS thicknesses at 600 and 1200 Å and varying the SnO_2 thickness in the range of 700 Å to 12000 Å. Again, attempts were made to obtain minimum reflectance at $\lambda=6000$ Å, which is close to the peak in the solar spectrum. Notice that the 600 Å thick CdS is close to the

optimum CdS thickness (575.6 Å), determined from Equation (4.8), which provides a local minimum in the reflectance at the desired wavelength. The 1200 Å thick CdS satisfies $n_2 d_2 = 1/2 \lambda$ criteria in conjunction with quarter wavelength thick SnO₂ ($n_1 d_1 = 1/4 \lambda$) to form a double minima (W-shaped) in the reflectance curve. The corresponding reflectance-induced photocurrent loss for the two cases, calculated from the simulated reflectance spectrum, are shown in Figure 4.3. The data clearly indicates that there is about 0.8-0.9 mA/cm² difference in the minimum and maximum values of the photocurrent loss. Figure 4.3 also indicates that the photocurrent loss is lower for the V-shaped reflectance profile (CdS = 600 Å curve) compared to the W-shaped profile (CdS = 1200 Å curve). This is because the W-shaped profile has a local maximum at 6000 Å and the two minimum points are located outside the CdTe cell absorption window (4000-9000 Å). Notice that when the SnO₂ thickness increases beyond 6000 Å, which is generally needed and used in current CdTe solar cells in order to reduce the resistive loss, photocurrent loss resulting from reflectance does not change much with the SnO₂ thickness.

Some absorption measurements were also performed on the SnO₂ films to determine the photocurrent loss from the absorption in the SnO₂. It was found that, on the average, about 15% of incident light is absorbed in a 10000 Å thick SnO₂ layer. Thus, reducing the SnO₂ thickness could indeed reduce the photocurrent loss from

Figure 4.3 Photocurrent loss in CdTe solar cells due to the reflection with varying SnO₂ thicknesses.

absorption, however, the increase in resistive loss because of thinner SnO_2 film could lower the J_{sc} and cell performance. Therefore, because of the competition between the absorption and resistive losses, and the insensitivity of reflectance induced photocurrent loss when the SnO_2 thickness is increased beyond $6000 \text{ \AA}$, we conclude that the CdS film thickness is more critical than the SnO_2 thickness, and SnO_2 thickness in the range of $6000\text{-}10000 \text{ \AA}$ is recommended for achieving higher J_{sc} in the CdTe solar cells.

4.4.4 Minimization of the Front Glass Surface Reflectance

Even if the thicknesses of the CdS and SnO_2 layers were optimized to reduce the reflectance, there is still about four percent of incident light that is reflected from the air/glass interface ($n=1.5$ for glass). This reflectance corresponds to about 1.2 mA/cm^2 current loss in the CdTe solar cells under AM 1.5 illumination. Therefore, an appropriate antireflection (AR) coating layer on the glass substrate should improve the CdTe cell performance. Model calculations showed that in order to obtain zero reflectance, the optimum refractive index n_1 and thickness d_1 should be approximately 1.225 and $1224 \text{ \AA}$, respectively, by using Equation (4.3) with $n_0=1$ for air, $n_2=1.5$ for glass. The corresponding reflectance is calculated and shown in Figure 4.4a, as a function of wavelength. It was found that such a coating could reduce the photocurrent loss from 1.2 mA/cm^2 to 0.13 mA/cm^2 . Since the material with $n_1=1.225$ is not readily available for

Figure 4.4 Calculated reflectance for different AR coatings on glass.

the AR coating application, Magnesium Fluoride, with $n_1 = 1.38$, was deposited on the glass surface. MgF_2 is widely used as an AR coating material for Si solar cells. A combination of modelling and experimental data was utilized to understand how and to what extent the MgF_2 AR coating can improve the short circuit current of the CdTe cells. The simulated reflectance for a single layer MgF_2 coating on glass is also shown in Figure 4.4b. The reflectance curves in Figure 4.4 were calculated to obtain minimum reflectance at $\lambda=6000 \text{ \AA}$, using the guideline $n_1 d_1 = \lambda/4$. This reflectance data was then utilized to calculate (Equation 4.1) the corresponding photocurrent loss (Table 4.2a). These calculations predict that the J_{sc} of a CdS/CdTe cell should increase by about 0.7 mA/cm^2 as a result of $1087 \text{ \AA}$ MgF_2 AR coating. In order to verify the above results experimentally, about $1100 \text{ \AA}$ MgF_2 was evaporated on the glass side of the CdTe solar cells and the reflectance as well as short circuit current density were measured before and after the AR coating (Figure 4.5). These measured spectra were also used to calculate the corresponding photocurrent loss, listed in Table 4.2b. Notice that the shapes of measured and calculated reflectance curves (Figures 4.4 and 4.5) are slightly different because the simulation in this section ignores any interference from $\text{SnO}_2/\text{CdS}/\text{CdTe}$ films below the thick glass plate. However, since such effect should be the same before and after the AR coating, the simulated current gain of 0.7 mA/cm^2 agrees well with the gain calculated from the measured reflectance (Table 4.2). This also agrees well with the

Table 4.2 Photocurrent losses before and after AR coating which were calculated from
 (a) simulated reflectivity spectrum
 (b) measured reflectivity of a practical cell

Conditions	Photocurrent Losses (mA/cm ²)	Current gain from AR
(a) Current loss calculated from the simulated reflectivity spectrum		
Glass only	1.24	-
$t_{\text{MgF}_2} = 1087\text{\AA}$ (min reflectance at 6000\AA)	0.52	0.72
(b) Current loss calculated from the measured reflectivity of a cell		
Before MgF ₂ coating	2.41	-
After MgF ₂ coating	1.75	0.67

Figure 4.5 Measured reflectance for CdTe/CdS solar cells with and without MgF₂ AR coating on glass.

increase in J_{sc} from 23.1 mA/cm² (before AR coating) to 23.6 mA/cm² (after AR coating). The slight difference between the measured and calculated increase in J_{sc} could result from the assumed 100% internal quantum efficiency (IQE) in the simulation.

4.5 Conclusion

Attempts were made to simulate and measure the photocurrent loss in the CdTe solar cells due to the CdS and SnO₂ thickness, before and after an antireflection coating. The effects of CdS thickness on the reflectance and photocurrent loss were investigated and it was found from the simulation that the reduced reflectance could increase J_{sc} by about 1 mA/cm², if the CdS thickness is reduced to 600 Å. These results were verified by fabricating CdTe solar cells with CdS thicknesses of 1600 and 650 Å. It was found that the optimum CdS thickness is about 600-700 Å for achieving high J_{sc} in a practical CdTe solar cell, because at this thickness, it retains the benefit of both reduced absorption and reflectance without the risk of pin-holes formation. Reducing the CdS thickness below 600 Å increases the reflectance losses and may not give a significant increase in J_{sc} due to reduced absorption because pin-holes formation tends to degrade the cell performance. It was found that the control of CdS film thickness is more critical than that of the SnO₂ because the reflectance does not change much when the SnO₂ thickness exceeds 6000 Å, which is used by most investigators today to minimize the series

resistance. Because of the competition between the resistive and absorption losses, SnO_2 thickness in the range of 6000-10000 Å is recommended. Finally, optimum MgF_2 thickness on glass was found to be 1100 Å, which should give about 0.7 mA/cm² additional increase in J_{sc} . Thus, the J_{sc} and efficiency of the CdTe solar cells can be enhanced by the proper control of CdS and SnO_2 thickness and the use of appropriate AR coating on glass.

CHAPTER V

THE IMPACT OF MOCVD GROWTH AMBIENT ON LOSS MECHANISMS ASSOCIATED WITH THE CdTe LAYER AND CdTe/CdS INTERFACE

5.1 Introduction

High-efficiency ($>10\%$) polycrystalline CdTe/CdS solar cells have been made by electrodeposition [1], physical vapor deposition [2], close-space sublimation [3], screen printing [4], atomic-layer epitaxy [5], metalorganic chemical vapor deposition (MOCVD) [6], and molecular beam epitaxy (MBE) [7]. However, cells made by different groups show a significant variation in J_{sc} and V_{oc} , partly because of the lack of understanding of the efficiency-limiting mechanism in the CdTe/CdS cells. For example, some cells show high V_{oc} but low J_{sc} and vice versa (Table 5.1) [8]. It is well known that imperfections, such as native point defects in II-VI compound semiconductors affect the electrical properties of the materials. As mentioned in Section 2.5, cadmium telluride exhibits a significant amount of self-compensation, which limits the type and the range over which it can be doped. Therefore, in order to grow high-quality CdTe films and fabricate high-

Table 5.1 Comparison of cell parameters from various investigators.

Manufacturer	V_{oc} (mV)	J_{sc} (mA/cm ²)	Fill factor	Eff (%)
Univ. of South Florida	843	25.1	0.745	15.8
British Petroleum	819	23.5	0.74	14.2
Photon Energy	790	26.2	0.615	12.7
Georgia Tech	784	23.3	0.657	11.9
Microchemistry Ltd.	810	19.5	0.73	11.5
Matsushita	797	21.1	0.67	11.3
Univ. of Queensland	720	24.0	0.65	11.2
Battelle Europe	750	22.8	0.65	11.0
Institute of Energy Conversion	789	20.1	0.69	11.0

efficiency CdTe solar cells, further efforts are needed to improve the fundamental understanding of defects and loss mechanisms that control V_{oc} and J_{sc} of the CdTe cells. In this chapter, polycrystalline CdTe/CdS solar cells were fabricated by MOCVD to vary the Te/Cd mole ratio in the growth ambient in order to alter and investigate the impact of native defect concentration on the cell parameters. If the effect of growth ambient is translated into the films, then the Cd-rich ambient should introduce Te vacancies and the Te-rich ambient should introduce Cd vacancies in the bulk and at the interface.

5.2 MOCVD Growth and Cell Fabrication

In order to accomplish this task, CdTe films were grown by MOCVD and the Te/Cd mole ratio in the growth ambient was varied in the range of 0.02 to 15 by controlling the temperature of the bottles that contain the metallorganic precursors. This was done in an attempt to alter the native defect concentration in the CdTe films. Diisopropyltelluride $((C_3H_7)_2Te)$ and dimethylcadmium $((CH_3)_2Cd)$ were used as precursors for Te and Cd, respectively. The flow rate of the H_2 carrier gas through the two bottles was varied. The calculation of Te/Cd mole ratio was based on the H_2 carrier gas flow rates and the temperature dependent partial vapor pressures of the metallorganic precursors. The vapor pressure for diisopropyltelluride can be expressed as

$$\log P_{Te} = 8.125 - \frac{2250}{T} , \quad (5.1)$$

and for dimethylcadmium

$$\log P_{Cd} = 7.764 - \frac{1850}{T} , \quad (5.2)$$

where P is the partial pressure in mm-Hg, and T is the temperature in Kelvin.

A series of CdTe films were grown on a CdS/SnO₂/glass substrate by varying the Te/Cd mole ratio in the range of 0.01 to 15 in the MOCVD growth ambient. The flow rates of (C₃H₇)₂Te and (CH₃)₂Cd were calculated for each Te/Cd mole ratios by using the following equation:

$$\frac{v_{Te}}{v_{cd}} = \frac{n_{Te}}{n_{Cd}} \frac{P_{Cd}}{P_{Te}} , \quad (5.3)$$

where n_{Te}/n_{Cd} represents the Te/Cd mole ratio in the growth ambient, v_{Te} and v_{cd} is the H₂ carrier gas flow rate through the (C₃H₇)₂Te and (CH₃)₂Cd sources, respectively, and P_{Cd} and P_{Te} are the partial pressures obtained from Equation (5.1) and (5.2). The flow rates for the Te and Cd sources for various Te/Cd mole ratios used in this study were calculated and listed in Table 5.2. After the CdTe was grown on a CdS/SnO₂/glass substrate, the sample was treated with CdCl₂ and then the Au/Cu contact was formed by using the standard solar cell fabrication procedures described in Section 3.2. The MOCVD growth ambient was found to have a marked effect on the cell parameters. A thorough characterization of the films grown under different conditions was done by using

Table 5.2 The flow rates and temperatures of the Te and Cd sources for various Te/Cd mole ratios used in this study.

Partial pressure P (mm-Hg)	H ₂ flow rate (ml/min)		Te/Cd mole ratio
	(C ₃ H ₇) ₂ Te	(CH ₃) ₂ Cd	
P _{Te} at 20°C = 2.8 P _{Cd} at 37°C = 62.6	90	180	0.02
	180	180	0.05
	360	180	0.09
P _{Te} at 20°C = 2.8 P _{Cd} at 0°C = 9.7	125	160	0.22
	125	40	0.9
	125	20	1.8
	400	20	5.8
P _{Te} at 37°C = 7.3 P _{Cd} at 0°C = 9.7	400	20	15

a variety of electrical and optical measurements. These results are discussed in the following sections.

5.3 Results and Discussions

5.3.1 Effect of Native Defects on CdTe Thin Film Properties

Native point defects have a significant effect on the electrical properties, doping concentration and conductivity type of CdTe material. The highly Te-rich MOCVD growth ambient may produce some Cd vacancies in the as-grown CdTe films, and likewise Te vacancies may form in the CdTe films grown in highly Cd-rich growth conditions. Since Te and Cd vacancies generally behave as n-type and p-type dopants [9], respectively, the conductivity type of the as-grown CdTe films should be a function of the Te/Cd mole ratio in the MOCVD growth ambient if the effect of ambients are translated into the films. The Auger Electron Spectroscopy (AES) measurements performed on the CdTe films could not detect any change in the composition between a commercial single crystal CdTe and the MOCVD-grown polycrystalline CdTe films. The sensitivity of the AES (0.15% atomic) was also unable to resolve any differences between the CdTe films grown with different Te/Cd ratios in the MOCVD ambient (Figure 5.1).

In order to test the hypothesis that the change of Te/Cd ratio in the growth ambient results in the change of native defect concentration in the deposited films, the

Figure 5.1 Auger depth profiles at and near CdTe/CdS interface for cells grown with different Te/Cd mole ratios in MOCVD ambient.

CdTe conductivity type was deduced from the quantum efficiency measurements via front and back illumination of the cell. Figure 5.2 shows the change in spectral response when the light enters from the Au/Cu side rather than from the glass side. The Au/Cu contact is only about 500Å thick, therefore some light can penetrate through the back contact. It is important to note that the Cu/n-CdTe contact is known to be rectifying and the Cu/p-CdTe contact is essentially ohmic. In the case of n-type CdTe or a Au/Cu/n-CdTe/n-CdS structure, when the light enters from the CdS side, the short wavelength radiation is strongly absorbed at the n-CdTe/CdS interface as well as in the CdTe film, away from the Cu/n-CdTe rectifying junction. Therefore most of the carriers generated by the short wavelength will not be collected by the Cu/n-CdTe junction. However, if the light enters from the back or the Au/Cu side, a stronger short wavelength response would be expected since the carriers are generated near the Cu/n-CdTe collecting junction. The QE plots in Figure 5.2a clearly show the above trend for the films grown in the Cd-rich ambient (Te/Cd~0.02) prior to any post-growth treatment. This confirms that the Cd-rich growth ambient produces essentially n-type films. However, in the case of the films grown in the Te-rich ambient (Te/Cd~6.0), the QE over the entire spectrum was much higher for the front side illumination (Figure 5.2b), which suggests that the film grown under Te-rich condition forms p-type CdTe. This is because Cd vacancies give rise to p-type films and most photons are absorbed near the n-CdS/p-CdTe collecting heterojunction. Thus, even

Figure 5.2 QE measurements of cells under different growth and treatment conditions with illumination from glass and Au/Cu sides.

though it is difficult to measure or detect native defect concentration in the films resulting from the change of Te/Cd mole ratio in the growth ambient, the conductivity type or QE measurements clearly suggest that we were able to alter the native defect concentration in the CdTe films. These observations are consistent with Chu et al's work [10] who used the photovoltage spectroscopy signal to determine the conductivity type.

It is necessary to convert the Cd-rich n-type CdTe films into p-type in order to get higher carrier collection and better cell performance since under normal solar cell operation, light enters from the CdS side. Figure 5.2c shows that the 400°C post-growth treatment for 30 minutes in air converts the n-type CdTe films grown under Cd-rich condition into a p-type film because the spectral response becomes uniformly high when the light enters from the front side. It is important to note that the heat treatment in the Ar ambient did not change the conductivity type. Therefore, it is not just the 400°C temperature but the presence of oxygen is responsible for the type conversion, because oxygen is often used as a p-type dopant for CdTe [11]. It was found that even though the conductivity type has been changed, the CdTe cells grown in Cd-rich conditions after the air treatment still show very poor cell performance with efficiency of less than 1% and J_{sc} of only 2-3 mA/cm². The cells fabricated with p-type CdTe films grown in the Te-rich condition also gave poor cell performance with efficiency of 3-4%. After the post-growth CdCl₂ treatment and furnace anneal, the CdTe cells grown in the Te-rich

condition achieved over 11% efficiency, but the cells grown in Cd-rich condition (Te/Cd~0.02) only reached 6-7%. These results show that the use of CdCl₂ during the post-growth treatment, combined with the Te-rich growth ambient, was necessary to achieve high performance cells.

Photoluminescence (PL) measurements were performed at liquid nitrogen temperature to investigate the defects in the CdTe films grown in the different MOCVD ambients. The PL spectra revealed a band at about 905 nm for the as-grown CdTe films in the Cd-rich (Te/Cd~0.02) growth ambient (Figure 5.3a). This band was not observed for the films grown in the Te/Cd~6 condition (Figure 5.3b) and also disappeared in the Cd-rich films after the post-growth CdCl₂ treatment and 400°C annealing. This suggests that the peak at 905 nm could be related to the Te vacancies or its complexes [12].

5.3.2 Correlations between Defects, Interface Quality, and Cell Performance

I-V measurements were performed on the cells fabricated with different Te/Cd mole ratio in the MOCVD growth ambient. Like the change in the conductivity type, the growth ambient had a significant effect on the terminal characteristics of the cells, namely J_{sc} and V_{oc} . The J_{sc} showed a minimum at the Te/Cd ratio of ~0.1 (J_{sc} =16 mA/cm²) and increased on both sides (J_{sc} of 23.95 mA/cm² and 22.4 mA/cm² for Te/Cd ratios of ~6 and 0.02 respectively). In contrast to J_{sc} , V_{oc} was found to be low near the stoichiometric

Figure 5.3 PL spectra of CdTe films under (a) $\text{Te/Cd} \sim 0.02$ growth ambient, (b) $\text{Te/Cd} \sim 6.0$ growth ambient, (c) $\text{Te/Cd} \sim 0.02$ growth ambient after CdCl_2 treatment.

(Te/Cd~1) and Cd-rich growth conditions, but increased monotonically when the Te/Cd ratio was increased to ~6 before saturating (Figure 5.4). These results support the merit of Te-rich growth ambient and suggest that the difference in the parameters of the CdTe cells fabricated by various investigators, using different growth techniques and ambient, could be partly due to the difference in the native defect concentration, because generally no serious attempt is made to measure or control the defect concentration.

Solar cells fabricated with three different Te/Cd mole ratios (Te/Cd~6, 0.1, and 0.02) in the MOCVD growth ambient were selected for detailed analysis because (a) Te/Cd~6 represents the Te-rich condition, which gave the highest V_{oc} and J_{sc} , and there was no appreciable change in V_{oc} and J_{sc} when the ratio was increased to 15; (b) Te/Cd~0.1 condition gave the lowest V_{oc} and J_{sc} ; and (c) Te/Cd~0.02 condition gave low V_{oc} , but fairly high J_{sc} .

Detailed defect and transport analysis was performed to explain the observed positive effects of Te-rich ambient on V_{oc} and the cell performance. V_{oc} is generally quite sensitive to interface quality. This suggests that as we go from the Cd-rich to Te-rich ambient, the interface quality improves, and after Te/Cd ratio of 6, V_{oc} is not dictated by the interface quality. Even though the Auger depth-profile measurements were unable to detect the change in the bulk composition, they did reveal that the atomic interdiffusion at the CdTe/CdS interface is maximum for the CdTe film grown under the Te-rich

Figure 5.4 J_{sc} and V_{oc} of MOCVD CdTe/CdS solar cells grown with different Te/Cd mole ratios in MOCVD ambient.

conditions (Figure 5.1). Table 5.3 shows that the absolute efficiency of the cells grown in the Te-rich condition (Te/Cd~6) was significantly higher (11.54% as opposed to only 4.47%) than the cells grown in the Cd-rich conditions (Te/Cd~0.1). The higher V_{oc} under the Te-rich condition could be attributed to the reduced density of interface states because of the reduced lattice mismatch resulting from the enhanced interdiffusion-induced gradual change in bandgap from CdS to CdTe [13]. It was also found by the AES measurements that the 400°C post-growth furnace anneal had no noticeable effect on the interdiffusion at the CdTe/CdS interface. These results indicate that the extent of interdiffusion at the interface is dictated more strongly by the MOCVD growth ambient than by the post-growth heat treatment.

The exact mechanism for the enhanced interdiffusion is not fully understood at this time. However, it is well known that the diffusion coefficient of chalcogens (Te, S etc.) in II-VI compounds increases with increasing the chalcogen pressure at high temperature, because under excess chalcogen conditions, fast diffusing interstitial form of the chalcogen dominates the diffusion process [14]. On the other hand, under metal (Cd) rich conditions, where the maximum chalcogen vacancy concentration are expected, the slower vacancy-diffusion mechanism for the chalcogen dominates the diffusion process[14]. In addition to that, based on the observed slight decrease in the bandgap of the Te-rich CdTe films, it has been suggested that sulfur diffusion is enhanced in the Te-rich films [15].

Table 5.3. Solar cell data for CdTe/CdS cells grown with different Te/Cd mole ratios in MOCVD growth ambient.

Te/Cd mole ratio	V_{oc} (mV)	J_{sc} (mA/cm ²)	Fill factor	Eff (%)
6.0	740	23.95	0.651	11.54
0.1	593	18.80	0.425	4.47
0.02	635	22.42	0.465	6.63

This is based on the fact that the addition of sulfur reduces the CdTe bandgap [16]. Both these facts explain the observed increase in the interdiffusion at the CdTe/CdS interface grown in the Te-rich conditions.

5.3.3 Light- and Voltage-bias-dependent QE Analysis of CdTe Cells Grown in Cd- and Te-rich Conditions

Since quantum efficiency is a good indicator of J_{sc} , detailed QE measurements were performed to investigate the carrier collection probability in the cells and to explain the observed trend in the J_{sc} (Figure 5.4). QE measurements, without external light bias, on the CdCl₂-treated CdTe films showed no appreciable dependence on the Te/Cd ratio in the growth ambient. However, the light-biased QE response showed much higher carrier collection in the cells grown in the Te-rich and highly Cd-rich (Te/Cd~0.02) conditions, but poor carrier collection in the cells grown with Te/Cd ratio ~0.1 (Figure 5.5). The significant difference between the dark and light QE response suggests that shining light on CdTe solar cells activates some defects that contribute to additional recombination or carrier loss. Thus, the light-biased QE agrees well with the observed trend in the J_{sc} and the combination of light and dark QE measurements indicates that the Te/Cd~0.1 growth condition gives rise to highest light-sensitive defect density.

It is known that the photocurrent in polycrystalline solar cells is a function of bias

Figure 5.5 Light-biased quantum efficiency at zero and 0.6 V forward bias for cells grown with different Te/Cd mole ratios in MOCVD ambient.

voltage [17,18]. Such dependence results in a decrease in collection efficiency as the voltage bias (not the light) is applied, causing a cross-over in the light and dark I-V curves. The collection probability $h(V)$ of photon-generated carriers through the junction can be approximated by [17,18]

$$h(V) = \frac{\mu E_o}{\mu E_o + S}, \quad (5.4)$$

where μ is the electron mobility within the junction region, E_o is the electric field across the junction, and S is the interface recombination velocity. Since the S is proportional to the interface defect density, higher defect density results in poor carrier collection or lower QE. The absolute QE as well as the relative change in QE with 0, 0.3 and 0.6 volt forward biases were measured to investigate the interface quality of the CdTe cells, as shown in Figure 5.6. Notice that the absolute QE at any given bias is higher for the Te-rich samples. This could sometimes be due to factors other than the interface defects. However, the fact that the QE decreases rapidly with the increase in forward bias voltage and the AES profiles show less interdiffusion for the Cd-rich CdTe cells, reinforces the hypothesis that there are fewer defects at the CdTe/CdS interface in the Te-rich films due to the enhanced interdiffusion.

Figure 5.6 Change in quantum efficiency with 0, 0.3 and 0.6 volts forward bias for cells grown in different Te/Cd mole ratios.

5.3.4 Correlation between Carrier Transport Mechanism and Cell Performance

As mentioned in Section 2.4, current transport analysis is the best way to reveal and quantify the recombination mechanisms in CdTe/CdS heterojunction solar cells, and understand the bulk as well as interface properties. Therefore, J-V-T measurements were performed on the CdTe cells with different Te/Cd mole ratios in the MOCVD growth ambient in order to understand the correlations between the native defects, transport mechanisms, and cell performance. The experimental techniques used to obtain and fit the measured J-V-T data are described in Section 3.4 and the relevant theory and analysis of carrier transport is summarized in Section 2.4. The results of the transport analysis are discussed in the following sections.

A. Transport analysis of Cd-rich CdTe solar cells

First, the J-V-T measurements were performed on two Cd-rich CdTe cells (Te/Cd~0.02 and Te/Cd~0.1) which had undergone the CdCl₂ treatment. Ideality factor (A) and J_0 were determined as a function of temperature, using the previously mentioned fitting procedure (Section 2.4). Both A and J_0 were found to be temperature dependent (Table 5.4), indicating that the transport is dominated neither by pure recombination nor by direct tunneling. Therefore, an attempt was made to investigate the possibility of tunneling/interface recombination mechanism [19], which is generally described by the following equations:

Table 5.4 J-V-T parameters (J_0 and A) for MOCVD-grown CdTe/CdS cells, extracted from fit to Equation (3.11).

T (K)	Te/Cd=0.02 with CdCl ₂		Te/Cd=0.1 with CdCl ₂		Te/Cd=6 without CdCl ₂		Te/Cd=6 with CdCl ₂	
	J_0 (A/cm ²)	A	J_0 (A/cm ²)	A	J_0 (A/cm ²)	A	J_0 (A/cm ²)	A
220	7.4×10^{-13}	2.28	8.6×10^{-14}	2.08	--		5.9×10^{-15}	1.84
230	1.7×10^{-12}	2.13	2.8×10^{-13}	2.00	--		6.2×10^{-14}	1.88
240	4.8×10^{-12}	2.02	2.4×10^{-12}	2.02	--		3.8×10^{-13}	1.87
250	3.1×10^{-11}	1.99	1.9×10^{-11}	1.98	8.7×10^{-11}	2.22	2.6×10^{-12}	1.86
260	7.4×10^{-11}	1.89	4.3×10^{-11}	1.88	3.6×10^{-10}	2.18	1.3×10^{-11}	1.89
270	2.2×10^{-10}	1.88	7.2×10^{-11}	1.74	1.6×10^{-9}	2.16	4.8×10^{-11}	1.88
280	5.5×10^{-10}	1.83	2.8×10^{-10}	1.72	6.3×10^{-9}	2.15	2.1×10^{-10}	1.89
290	1.1×10^{-9}	1.75	--		2.3×10^{-8}	2.14	7.6×10^{-10}	1.87
300	2.3×10^{-9}	1.68	--		6.8×10^{-8}	2.09	1.7×10^{-9}	1.81

$$J = J_o [e^{CV_j} - 1] , \quad (5.5)$$

where

$$J_o = J_{oo} e^{\frac{-\Delta E}{kT}} \quad (5.6)$$

and

$$C = (1-f)B + \frac{f}{(\xi kT)} . \quad (5.7)$$

By fitting the experimental data to the above equations, the C value was determined at each temperature and then plotted as a function of $1000/T$ to obtain the values of $(1-f)B$ and f/ξ . As discussed in Section 2.4, f represents the extent of tunneling: $f=0$ represents pure tunneling, and $f=1$ indicates no tunneling but pure interface recombination. The values of $(1-f)B$ and f/ξ were found to be 20.6 V^{-1} and 0.135 , respectively, for the cells grown with Te/Cd mole ratio of ~ 0.02 (Figure 5.7a) and 19.2 V^{-1} and 0.254 , respectively, for the Te/Cd ~ 0.1 growth condition (Figure 5.7b). Thus, the above analysis clearly shows that the current transport in both the cells grown in the Cd-rich ambient is limited by a combination of interface recombination and tunneling, because f is neither 0 nor 1.

B. Transport analysis of Te-rich CdTe solar cells

The J-V-T analysis was also performed on the Te-rich (Te/Cd ~ 6) cells, with and without post-growth CdCl_2 treatment. Without the CdCl_2 treatment, both A and J_o were found to be temperature dependent; however, the A values did not change as much with the temperature as was observed in the case of the Cd-rich cells analyzed above (Table

Figure 5.7 Plot of C-factor vs 1000/T (T/IR model), supporting contention that Cd-rich cells exhibit higher degree of tunneling.

5.4). By fitting the experimental data to Equation (5.7), the values of $(1-f)B$ and f/ξ were found to be 5.54 V^{-1} and 0.766, respectively (Figure 5.7c). Notice that the f/ξ value in the untreated Te-rich cells is higher than the value in the CdCl_2 -treated Cd-rich cells. This result indicates that the Cd-rich cells exhibit a higher degree of tunneling, even after the CdCl_2 treatment, compared with the untreated Te-rich cells. The result again provides strong support for the hypothesis that higher atomic interdiffusion is coupled with lower defect density near the interface of the cells grown in the Te-rich condition. (Recall from Section 5.3.2 that most of the interdiffusion in the Te-rich samples occurs before the CdCl_2 post-growth treatment.) The tunneling probability decreases for the Te-rich cells because the enhanced interdiffusion causes the band edge to change gradually from that of CdS to that of CdTe, which not only enlarges the energy barrier thickness for tunneling but also reduces the defect density of the available tunneling sites (Figure 5.8).

After the CdCl_2 treatment, the cells grown in the Te-rich condition (Te/Cd-6) showed a temperature-independent ideality factor (Table 5.4), which suggests that straight depletion-region or interface recombination controlled the current transport (Section 2.4). Moreover, the slope of $\ln(J_0 T^{-2.5})$ vs $1000/T$ gave an activation energy of 0.76 eV (Figure 5.9), which is approximately equal to half of the CdTe bandgap, indicating that the depletion region recombination [20,21], rather than the interface recombination, dominates the current transport in the CdCl_2 -treated Te-rich cells (Section 2.4). This result also

Figure 5.8 The tunneling probability decreases because the enhanced interdiffusion enlarges the energy barrier thickness for tunneling.

Figure 5.9 Plot of $\ln(J_0 T^{-2.5})$ vs $1000/T$ for CdTe/CdS cells grown in Te-rich ambient (Te/Cd~6) after CdCl_2 post-growth treatment.

indicates that even though the Te-rich cells have lower defect density, the CdCl_2 treatment further reduces the defect density to the extent that the transport mechanism is no longer dominated by the interface, instead, defects in the depletion region become more important. It is quite clear from this analysis that the Te-rich growth ambient combined with the post-growth CdCl_2 treatment gives the lowest defect density, which in turn results in the best cell performance.

5.3.5 Correlations between Carrier Life Time, Interdiffusion, and Cell Efficiency

Photoluminescence (PL) measurements were performed in order to examine the correlations between defects, interdiffusion, and effective lifetime. The CdTe films fabricated under different Te/Cd mole ratios were studied using time-resolved PL measurements at 295 K. Table 5.5 shows the effective lifetimes, τ_e , obtained from the PL measurements on the films grown under different conditions. Note that these are effective lifetime values, which include both bulk and interface recombination. The lifetime data in the table show that both Te-rich ambient and the post-growth CdCl_2 treatment assist in improving the material quality. The Te-rich growth ambient increased τ_e from 0.116 ns to 0.153 ns, and the CdCl_2 treatment increased it further to 0.236 ns. This is entirely consistent with the cell data, because the CdCl_2 -treated Te-rich devices gave the best performance. Notice that after the CdCl_2 treatment, τ_e for the Te/Cd~0.02

Table 5.5 Photoluminescence lifetime in cells processed with and without CdCl_2 treatment and with different Te/Cd mole ratios in MOCVD ambient.

Te/Cd mole ratio	CdCl_2 treatment	Lifetime (nsec)
0.02	No	0.116
0.1	No	0.121
6.0	No	0.153
0.02	Yes	0.210
0.1	Yes	0.201
6.0	Yes	0.236

growth condition is higher than τ_e for the Te/Cd~0.1 growth condition, which agrees well with the observed trend in the J_{sc} . These results clearly indicate that the Te-rich growth condition, combined with the $CdCl_2$ post-growth treatment, reduces the bulk/interface defect density and accounts for the higher τ_e and improved carrier collection.

5.4 Conclusion

In this chapter an attempt was made to identify and understand some of the factors and mechanisms that affect the defects in the bulk as well as at the CdTe/CdS interface of the CdTe solar cells. Even though we were unable to detect the difference in the film composition by the AES measurements, the change of CdTe conductivity type, deduced from the quantum efficiency measurements, confirmed that the change of Te/Cd ratio in the growth ambient alters the native defect concentration in the deposited films. It was found that the Cd-rich growth ambient produces essentially n-type films. However, the film grown under the Te-rich condition forms p-type CdTe. This is because Te vacancies act as n-type dopants while Cd vacancies serve as p-type dopants. The 400°C post-growth anneal in the presence of oxygen converts the n-type CdTe films grown under Cd-rich condition into a p-type film. The MOCVD growth ambient also had a significant effect on the electrical characteristic of the CdTe cells. J_{sc} showed a minimum at a Te/Cd ratio of ~0.1 and increased on both sides of this minimum. The Te-rich growth ambient

(Te/Cd $\geq$ 6) gave an average V_{oc} of 720 mV in this study, and the V_{oc} was found to be about 120 mV lower for the stoichiometric and the Cd-rich growth conditions. It is found that the Te-rich growth ambient allows more interdiffusion at the CdS-CdTe interface, which in turn lowers the interface defect density resulting from stress reduction or gradual transition from CdS to CdTe. The post-growth CdCl₂ treatment helps in further reduction of the defect density, which results in higher τ_e , V_{oc} , J_{sc} , and cell efficiency. Reduction in the interface defect density switches the carrier transport mechanism from interface recombination/tunneling to straight depletion-region recombination in the CdCl₂-treated Te-rich devices. CdCl₂-treated Te-rich cells gave the best performance in this study, with V_{oc} =0.747 V, J_{sc} =24.55 mA/cm², and efficiency =12%. These results demonstrate that process optimization coupled with basic understanding of defects and loss mechanisms is critical for improving the efficiency of CdTe solar cells.

CHAPTER VI

EFFECTS OF CHEMICAL AND HEAT TREATMENTS ON CdTe MICROSTRUCTURE AND CdTe/CdS INTERFACE PROPERTIES

6.1 Introduction

High-efficiency (>10%) polycrystalline CdTe/CdS solar cells have been fabricated using various techniques and growth conditions [1]. CdTe growth parameters including growth ambient, time, and temperature can affect defects, material properties, as well as device performance. That is why cells made by different groups show a significant variation in cell parameters [1], and there is a considerable lack of understanding of the efficiency-limiting defects and loss mechanisms in the CdTe/CdS solar cells. It was shown in the previous chapter that the MOCVD growth ambient had a significant effect on the cell performance. In addition, the post-growth CdCl₂ treatment helped in reducing the defect density, and gave higher τ_e , V_{oc} , J_{sc} , and cell efficiency. We also showed in Chapter V that the reduction in the interface defect density switched the carrier transport mechanism from interface recombination/tunneling to straight depletion-region recombination in the CdCl₂-treated Te-rich devices. Even though we were able to observe and quantify the improvement in the electrical characteristics of solar cells, the exact

reason for the enhanced cell performance resulting from the chemical and heat treatments was not fully understood. Therefore, in this chapter, an attempt is made to increase the fundamental understanding of the role of CdCl_2 treatment by varying the CdCl_2 concentration and anneal conditions.

In addition to the conventional furnace anneal, rapid thermal processing (RTP) is used to improve the fundamental understanding of the role of heat treatment. The advantage of RTP lies in its ability to selectively enhance desirable processes, such as defect removal, dopant activation, grain growth, and compound formation, while minimizing undesirable effects such as re-evaporation, diffusion, and film decomposition [2]. In addition, rapid thermal processing lowers energy consumption and can speed cell fabrication. RTP has been used for homojunction formation in the CdTe, InP, and CuInSe_2 thin film solar cells [3,4], as well as for grain growth in the amorphous/polycrystalline silicon cells [5,6]. However, no research has been conducted on the CdTe/CdS heterojunction cells using RTP. Although the CdCl_2 treatment followed by a furnace anneal is known to enhance grain regrowth and significantly improve cell performance, certain efficiency limiting factors, such as Cl related defects, could be associated with this conventional furnace annealing process (Section 2.5.5). In order to avoid the possible deleterious effects, the use of a low-cost RTP at high temperatures may allow grain regrowth in the CdTe films with lower CdCl_2 concentrations, or no CdCl_2

treatment, thus reducing the chlorine related defects. The controllability of temperature and time of RTP can also be used to tailor the interdiffusion to optimize the CdTe/CdS interface quality, which is critical for the CdTe solar cell performance, as shown in Section 5.3.

Several parameters such as concentration of CdCl_2 in methanol, temperature and duration of RTP anneal, and annealing ambient is investigated in this chapter by complete device fabrication followed by detailed characterization and analysis. In addition, a comparison of the RTP and furnace treated devices is made to understand the role of heat treatments on bulk and interface properties and cell performance.

6.2 Experimental Techniques

Since it was found in the previous chapter that the Te-rich MOCVD growth ambient gave the lowest defect density and the best cell performance, therefore, in the subsequent chapters, all the CdTe layer are grown under Te-rich ($\text{Te}/\text{Cd}=6$) MOCVD ambient. After the CdTe film growth by MOCVD, solar cells were fabricated and characterized in detail, as described in Section 3.2.3.

In order to study the optimum CdCl_2 treatment conditions, the concentration of CdCl_2 solution was varied in the range of 0 to 1 (saturated) by varying the amount of CdCl_2 in the CH_3OH solvent before it was put on the CdTe surface. For example, 0.25

concentrated CdCl_2 solution corresponds to 0.25gm CdCl_2 powder dissolved into 100 ml CH_3OH solvent.

Rapid thermal processing was utilized to replace the CdCl_2 treatment procedure in solar cell fabrication process. RTP was done in an AET Addax computer-interfaced processor. The $\text{CdTe/CdS/SnO}_2/\text{glass}$ samples were placed on a quartz disc, covered by a quartz watch glass, and radiatively heated to the desired temperature with a bank of quartz halogen lamps (Figure 6.1a). The film surface temperature was measured by direct thermal contact using thermocouple wires. The annealing was done in a controlled $\text{O}_2\text{-N}_2$ ambient, with varying percentage of O_2 , as well as in the forming gas ambient. A complete list of process variables for the post-growth treatment includes:

- (a) Concentration of $\text{CdCl}_2\text{-CH}_3\text{OH}$ solution
- (b) RTP temperature (range: 400°C - 750°C)
- (c) RTP time (range: 5 sec -100 sec)
- (d) Ambient gas composition and pressure

A typical annealing profile used in the RTP system is shown in Figure 6.1b.

6.3 The Effects of CdCl_2 Treatment on Morphology and Grain Size

The effects of CdTe growth conditions and CdCl_2 treatment on the surface morphology and grain structure of the polycrystalline CdTe films were studied by SEM

6.3 The Effects of CdCl_2 Treatment on Morphology and Grain Size

Figure 6.1 (a) AET ADDAX Rapid Thermal Processor, (b) Typical annealing profile generated by RTP control.

and quantitative microscopy. The as-grown MOCVD CdTe layer on the CdS/SnO₂/glass substrate showed porous, non-uniform surface morphology and a loose, faceted, random grain structure with a grain size of 1-2 μm (Figure 6.2a). The grain structure was found to be essentially independent of Cd- or Te-rich MOCVD growth conditions. After the CdCl₂ treatment, even though the grain size does not change significantly, Figure 6.2b shows that this treatment tends to densify the film and changes the surface morphology. In fact, the CdCl₂ treatment makes the grains less faceted and flat, and serves as a flux to recrystallize the CdTe structure. Grain boundary surface area per unit volume, S_v , is an important microstructural parameter for polycrystalline material. Large S_v value implies more grain boundary conduits for impurity and metal to diffuse to the CdTe bulk and CdTe/CdS interface during the metallization and subsequent anneal, which may create more recombination centers or shunt paths to degrade the cell performance. The S_v value for a polycrystalline structure can be obtained by quantitative microscopy using the following equation [7]:

$$S_v = 2P_L \quad , \quad (6.1)$$

where P_L is the average number of intersections of a randomly oriented test line of unit length with the observed grain boundaries. The S_v value for the as-grown CdTe layer was found to be 1.66 μm^{-1} , which remained essentially the same after the CdCl₂ treatment. Even though the overall S_v value did not change, a loose and faceted structure of the

Figure 6.2 SEM Microstructure of CdTe (a) as-grown film, (b) after CdCl_2 treatment.

CdTe before CdCl₂ treatment is expected to provide more voids and conduits for the impurity migration. In order to take this factor into account, an S_{v1} parameter was defined as an effective grain boundary surface area by calculating the average number of intersections of a test line with the selected grain boundaries which form voids of diameter greater than 0.3 μm (Figure 6.2). The S_{v1} value for the as-grown CdTe layer was found to be 0.56 μm^{-1} , which reduced to 0.05 μm^{-1} after the CdCl₂ treatment. Thus, we conclude that because of the reduction of the conduits for impurity migration, CdCl₂ treatment reduces defect density and improves the cell performance. Notice that several investigators have found that the CdCl₂ treatment promotes the grain growth [8,9,10], which should reduce S_v and enhance the film quality and cell efficiency. In this study, we did not observe a significant change in the CdTe grain size, instead we saw a change in the S_{v1} value. This could be due to the differences in the CdTe growth techniques and the grain size and structure of the as-grown CdTe films. We found that the grain size is not the only factor that affects the film quality, the densification and microstructure of the CdTe films also plays an important role in the cell performance. A low effective grain boundary surface area per unit volume, which reduces the grain boundary conduits for impurity migration and metal diffusion, plays an important role in limiting the cell performance.

As mentioned in Section 2.5.5, even though CdCl₂ treatment is critical for high

efficiency CdTe cells, but it could also place an upper limit on the practically achievable efficiency. Ringel et al. [12] showed by DLTS measurements a large density of deep acceptor-like states at $E_v + 0.64$ eV after the CdCl₂ treatment. They attributed this defect to V_{Cd} and V_{Cd}-Cl related complexes, and showed that the V_{oc} is inversely proportional to the trap density while there is no apparent correlation between the J_{sc} and trap density [12]. In order to understand the role of chlorine-related defects in the CdTe/CdS cells and find the optimum CdCl₂ treatment conditions, the concentration of CdCl₂ was varied in the range of 0 to 1 (saturated) in this study. Light I-V measurements were performed on the finished devices to monitor the device performance and correlate it with the defects. Table 6.1 shows the CdTe/CdS solar cell parameters measured after the fabrication of the cells treated with different CdCl₂ concentrations. It is clear from the table that the V_{oc} and fill factor are a strong function of the CdCl₂ concentration. The data in Table 6.1 also show that the CdCl₂ treatment is important for the high cell efficiency, but the saturated CdCl₂ solution, used by most investigators [13], was not optimum for our MOCVD cells. Instead, a concentration of 50% to 75% gave the best results. The degradation in cell performance for saturated CdCl₂ concentration also supports the hypothesis that it could place an upper limit on the practically achievable efficiency unless the CdCl₂ process is modified.

PL measurements were performed on finished devices to investigate the defects

Table 6.1 Cell data with varying CdCl₂ concentration.

CdCl ₂ Concentration	V _{oc} (mV)	J _{sc} (mA/cm ²)	Fill factor	Eff (%)
0	385	10.5	0.32	1.30
0.25	694	24.4	0.528	8.89
0.50	708	25.5	0.599	10.82
0.75	702	25.8	0.581	10.56
1.0	665	22.9	0.483	7.38

produced by different CdCl₂ concentrations. The PL spectra of CdTe/CdS devices treated with different CdCl₂ concentration in Figure 6.3 show two common features: a peak around 7900 Å and a broad band centered around 8400 Å. The peak at 7900 Å is attributed to Cd vacancies [17]. The intensity or the peak amplitude of the broad band at 8400 Å is directly proportional to the defect concentration in the sample. In CdTe, the broad band centered around 8400 Å is generally attributed to structural defects, native defects or V_{Cd}-Cl defect complexes [14-16]. Several investigators have studied the effects of chlorine in single crystal CdTe by PL [14-17]. Chlorine is a donor in CdTe and is also known to form defect complexes with Cd vacancies, which are produced during the heat treatment. Chlorine-cadmium vacancy complexes are acceptor type and give rise to shallow and deep energy levels depending on the type of defect complex. According to the literature [14-17] the chlorine-cadmium defect complexes have energies in the range $E_v + 0.15 - E_v + 0.9$ eV. The fact that the PL broad band around 8400 Å has been attributed to V_{Cd}-Cl complex in the literature [17], and the intensity of this PL band in Figure 6.3 is inversely proportional to V_{oc}, suggests that these defects are probably chlorine related complexes formed during the CdCl₂ treatment. Notice that the cell treated with the saturated CdCl₂ solution gave the strongest broad band (Figure 6.3) and the lowest V_{oc} value. This result indicates that the saturated CdCl₂ treatment gives rise to higher chlorine related complex density, which degrades the cell performance. Thus,

Figure 6.3 PL spectra for CdTe treated with different CdCl_2 concentration, (a) saturated, (b) 0.5, (c) 0.25, (d) 0.75. The corresponding V_{oc} are also shown.

on one hand CdCl₂ treatment is critical to high efficiency CdTe cells but on the other hand it could place an upper limit on the practically achievable efficiency unless the CdCl₂ process is modified or optimized.

6.4 Rapid Thermal Processing of CdTe Solar Cells

Rapid thermal processing (RTP) is a promising technique for solar cells because of the low energy consumption and reduced cell processing time. In an attempt to eliminate the above Cl-related defects in CdTe resulting from the conventional CdCl₂ treatment, RTP was performed on CdS/CdTe structures to achieve grain regrowth in the CdTe films treated with dilute CdCl₂ solution, or with no CdCl₂ treatment at all. The controllability of temperature and time of RTP can also tailor the interdiffusion at the CdTe/CdS interface which was found (in Section 5.3) to be critical for the CdTe solar cell performance.

6.4.1 Investigation of RTP Solar Cell Performance

Different RTP conditions were investigated to study the effect of RTP parameters, such as time, temperature, ambient gas, and CdCl₂ concentration, on the solar cell efficiency. It was found that RTP conditions had a significant impact on the CdTe cell parameters, as shown in Table 6.2. It is important to note that the conventional furnace

Table 6.2 Cell results for different post-growth treatment conditions.

Annealing condition		V_{oc} (mV)	J_{sc} (mA/cm ²)	Fill factor	Eff (%)
Furnace Air	CdCl ₂ 400°C	781	23.26	0.657	11.9
RTP Forming gas	CdCl ₂ 600°C	547	7.09	0.478	1.94
RTP O ₂ +N ₂	CdCl ₂ 600°C	690	20.76	0.539	7.73
	No CdCl ₂ 600°C	704	18.51	0.535	6.97
	No CdCl ₂ 700°C	711	19.40	0.595	8.22
	No CdCl ₂ 700°C	746	22.24	0.644	10.7

anneal at 400°C for 30 minutes, without the CdCl₂ treatment, gave less than 3% efficient cells. However, a 400°C conventional furnace anneal with CdCl₂ treatment gave 11.9% efficient cells. In the conventional process, few drops of 50% CdCl₂ solution are poured onto the sample and allowed to dry in a few minutes. RTP at 600°C for 5 sec with 50% CdCl₂ solution treatment gave cells with less than 1% efficiency, suggesting that it may be necessary to reduce the CdCl₂ concentration or the CdCl₂ soak time for the RTP cells. The CdCl₂ soak time was reduced by a quick (7 seconds) dip in the CdCl₂ solution followed by a blow dry. RTP at 600°C for 5 sec with reduced CdCl₂ soak time in a forming gas ambient gave 1.9% efficient cells. However, when the ambient was switched to nitrogen with less than 7% oxygen, a fairly respectable efficiency of 7.7% was achieved. This result indicates that some oxygen is necessary for high efficiency [18]. Eliminating the CdCl₂ treatment altogether gave somewhat lower cell efficiency (6.9%), suggesting that some CdCl₂ treatment may be desirable before RTP. Increasing the RTP temperature from 600°C to 700°C without any CdCl₂ treatment, but with some oxygen, raised the efficiency from 6.9% to 8.2% (Table 6.2). In another run, a cell with 10.7% efficiency was achieved by 700°C, 5 second RTP, without any CdCl₂ treatment. This represents the highest CdTe cell efficiency achieved by the RTP process. However, results are not so reproducible because similar process conditions sometimes gave only 6% efficiency. Thus, on one hand the above results prove the potential of RTP for CdTe

cells, but on the other hand they indicate the need for further optimization of the RTP conditions and CdCl_2 treatment to achieve high yield and efficiency of the RTP CdTe cells.

SIMS measurements were performed to investigate the incorporation of Cl in the CdTe film with RTP (700°C , 5sec without CdCl_2) and CdCl_2 furnace anneal (Figure 6.4). The Cl concentration was found to be high in the CdTe films treated with CdCl_2 in furnace. However, the amount of Cl in the RTP CdTe film without the CdCl_2 treatment was found to be relatively low. The small traces of Cl found in the RTP CdTe films compared to the film without any anneal is attributed to the CdCl_2 treatment of the CdS film. The large Cl signal near the surface of all of samples is due to the difference in the detection sensitivity in the CdTe and Au/Cu matrices. The fact that the RTP can give high efficiency cells with no CdCl_2 treatment, suggests the possibility of reduction in the efficiency limiting Cl-related defect in the RTP cells.

In order to study the impact of chemical and heat treatment on the bulk and interface properties, Electron Beam Induced Current (EBIC) measurements were performed on the cells without treatment or anneal, CdCl_2 treatment with furnace anneal, and RTP anneal with no CdCl_2 treatment. The diffusion length of the carriers in each device can be obtained by comparing the EBIC line scan profiles across the CdTe and CdS layers. The results in Figure 6.5 indicate that the diffusion length in the as-grown

Figure 6.4 SIMS data shows a relatively low Cl content in the RTP CdTe films.

Figure 6.5 EBIC signals in CdTe films, (a) as-grown CdTe, (b) CdCl₂ furnace anneal at 400°C 30 min, (c) RTP anneal at 700°C 5 sec (Signal level not same).

CdTe is low, while the diffusion lengths in the RTP and furnace annealed cells are higher and comparable because both the EBIC line scans show longer decay profiles.

We showed in Section 6.3 that the 400°C furnace CdCl₂ treatment tends to densify the CdTe film and makes the grains less faceted and flat. The reduction in the effective grain boundary surface area per unit volume due to the change in the CdTe microstructure enhances the cell performance. In order to investigate the microstructure of the RTP annealed CdTe, SEM measurements were performed on (a) as-grown CdTe, and CdTe films after (b) furnace anneal at 400°C with CdCl₂, (c) RTP at 550°C, 5 sec, with a rapid (7 second) dip in the CdCl₂ prior to the RTP, and (d) RTP at 700°C for 5 sec, without CdCl₂. Figure 6.6c shows that RTP at 550°C tends to densify the film and changes the surface morphology, even though the grain size does not change significantly compared to the as-grown CdTe (Figure 6.6a). Therefore, this RTP anneal with a short CdCl₂ treatment tends to recrystallize the CdTe structure which is similar to the CdCl₂ furnace anneal (Figure 6.6b). RTP anneal at higher temperature (700°C) further promotes the recrystallization process and causes some fusion between grains (Figure 6.6d). Therefore, like the furnace anneal, the RTP anneal changes the CdTe microstructure and causes a reduction in the effective grain boundary surface area per unit volume, which improves the cell efficiency.

Figure 6.6 SEM Microstructure of CdTe (a) as-grown film, (b) after furnace 400°C, 30min, (c) after RTP 550°C, 5 sec, (d) after RTP 700°C, 5 sec.

6.4.2 Correlations Between Interface Diffusion and Post-growth Treatment Using Non-destructive XRD Technique

It was shown in Section 5.3 that the CdTe cell performance improves because of the higher degree of interdiffusion at the CdTe/CdS interface. Therefore, an attempt was made to investigate the interface quality of the cells fabricated with different anneal conditions. The CdTe films in all these samples were grown under the Te-rich MOCVD growth ambients which results in appreciable interdiffusion at the CdTe/CdS interface without any anneal (Section 5.3). Auger depth profiles showed no significant difference in the extent of interdiffusion at the CdTe/CdS interface after the conventional furnace or RTP anneal of the CdCl₂ treated CdTe films. Thus, annealing of Te-rich films either do not show further interdiffusion or the sensitivity of AES is unable to detect the change.

Therefore, an alternate method to detect the interdiffusion was investigated by comparing the peak location at a specific orientation angle in the X-ray diffraction (XRD) scan spectrum [19]. If S atoms diffuse into the CdTe layer and form a CdTe_{1-x}S_x interlayer, the lattice constant would change and cause a peak shift in the X-ray spectrum. In order to support the correlation between the interdiffusion and XRD peak shift, the XRD measurements were performed on the CdTe/CdS films with CdTe layers grown with Te/Cd ratios of 0.02, 0.1 and 6. Figure 6.7 clearly shows that a {220} peak located at 39.4° for the Cd-rich CdTe films (Te/Cd = 0.02 and 0.1), shifted to 39.47° for the Te-rich

Figure 6.7 XRD scan on the CdTe/CdS films with CdTe layer grown at Te/Cd ratio of 0.02, 0.1 and 6.

CdTe films. The lattice constant a was calculated by using the Bragg's diffraction equation:

$$2d\sin\theta = n\lambda \quad (6.2)$$

and

$$a = d\sqrt{h^2+k^2+l^2}, \quad (6.3)$$

where n is the order of diffraction, λ is the X-ray wavelength, and d is the spacing between (h,k,l) planes. The calculated lattice constant is 6.463Å for the CdTe films with Te/Cd=0.02, and 6.452Å for the CdTe films grown with Te/Cd ratio of 6. Since single crystal CdTe has a lattice constant of 6.481Å, this corresponds to a 0.28% shift in the lattice constant for the Te/Cd=0.02 condition, and 0.45% for Te/Cd ratio of 6. Since the AES measurements in Section 5.3.1 showed much higher interdiffusion for the Te-rich films, therefore, we conclude that the extent of the interdiffusion at the interface can also be observed from the peak shift in the XRD spectrum.

In order to observe the possible enhanced interdiffusion during the post-growth treatment, the XRD measurements were performed on the Te-rich CdTe/CdS films before and after different annealing. Figure 6.8 shows that after the 30 min, 400°C CdCl₂ furnace anneal, the interdiffusion increased, indicated by the peak shift. However, the peak position did not shift for the samples annealed at 400°C, 30 min without the CdCl₂ treatment. This indicates that the CdCl₂ treatment plays an important role in promoting the interdiffusion during the anneal process.

Figure 6.8 XRD scan on the CdTe/CdS films before annealing and after different annealing conditions.

XRD measurements were also performed on the samples treated with different RTP conditions. Figure 6.9 shows that the RTP treatment at 700°C for 5 sec, without CdCl₂ treatment produces less interdiffusion than the sample treated in furnace at 400°C for 30 min after the CdCl₂ treatment. An attempt was made to enhance the interdiffusion by a rapid (7 second) dip in the CdCl₂ prior to an RTP at 550°C, 5 sec. XRD measurements again showed less interdiffusion compared to the 400°C/30 min furnace anneal (Figure 6.9). This suggests that a short annealing time during the RTP process does not enhance interdiffusion at the CdTe/CdS interface even after the CdCl₂ treatment. Therefore, reduced interdiffusion at the interface may be one of the reasons for the lower RTP cell efficiency to date compared to the furnace annealed cells, even though the S_{v1} value and the diffusion length in the CdTe after the RTP is comparable to the concentrated CdCl₂ treated furnace annealed cells (Figures 6.5 and 6.6). Thus, interdiffusion, grain boundary area per unit volume, bulk life time and interface defect density, all tend to influence the CdTe cell efficiency.

6.5 Conclusion

In this chapter, an attempt was made to increase the fundamental understanding of the chemical and heat treatments by varying the CdCl₂ concentration and annealing conditions. It was found that the CdCl₂ treatment tends to densify the film, changes the

Figure 6.9 XRD scan on the CdTe/CdS films with RTP or furnace anneal.

surface morphology, makes the grains flat and less faceted, and serves as a flux to recrystallize the CdTe structure. This reduces the effective grain boundary surface area per unit volume or decreases the grain boundary conduits for impurity or metal migration, which enhances the cell performance. Light I-V and PL measurements revealed optimum CdCl₂ concentration in the range of 50% to 75% for our MOCVD cells. This is because higher CdCl₂ concentration gives rise to higher Cl-related defect density and degrades the cell performance. Therefore, even though CdCl₂ treatment is essential for high efficiency CdTe cells, it could place an upper limit on the practically achievable cell efficiency. Rapid thermal processing was performed on the CdS/CdTe structure to achieve grain regrowth in the CdTe films with lower CdCl₂ concentrations, or no CdCl₂ treatment. It was found that the change in RTP conditions produces significant variation in the CdTe cell parameters. A cell with 10.7% efficiency was achieved using 700°C, 5 second RTP condition without any CdCl₂ treatment. However, this efficiency was not very reproducible. Conventional CdCl₂ treated and furnace annealed cells gave efficiency in excess of 11.5%, which were more reproducible than the RTP cells. SEM and EBIC measurements showed that the CdTe microstructure and the diffusion length in the CdTe after the RTP is comparable to the regular CdCl₂ treatment. However, reduced interdiffusion at the CdTe/CdS interface in the RTP cells may be responsible for lower RTP cell efficiency to date compared to the CdCl₂ treated and furnace annealed cells.

CHAPTER VII

MULTIPLE EFFECTS OF Cu ON CONTACT PROPERTIES AND CELL PERFORMANCE

7.1 Introduction

In Chapter IV, V, and VI, we investigated the efficiency limiting defects and loss mechanisms associated with the photocurrent loss in CdS/SnO₂ layers, native defects in CdTe and at CdTe/CdS interface, and the post-growth anneal and heat treatment. In this chapter, we will show that even though the CdS and CdTe film quality can be optimized, the resistive and/or unstable ohmic contact to p-type CdTe [1] could limit the CdTe cell performance. The contact related difficulties come from the high degree of self-compensation in II-VI semiconductors and the large work function of p-type CdTe [2]. Several investigators have obtained reasonable cell efficiencies by utilizing Au/Cu metal films [3] or graphite paste doped with Cu or Hg [4] to form ohmic contacts on CdTe. It is generally believed that copper plays an important role by acting as a substitutional acceptor for Cd [5], thus increasing the doping concentration near the surface of p-type CdTe to form a good ohmic contact. On the other hand, Cu may also diffuse into the bulk and form interstitials or Cu-defect complexes [6] which can act as recombination

centers. Cu can diffuse through CdTe into the underlying CdS layer, causing shunting at the junction to decrease the cell performance [7]. However, no systematic study of the effect of Cu on CdTe/CdS device performance has been conducted. In order to achieve a better and reliable contact to CdTe solar cells, further efforts are needed to improve the fundamental understanding of the effects of Cu on those defects and loss mechanisms that control the CdTe solar cell performance. In this chapter, polycrystalline CdTe/CdS solar cells were fabricated with varying amount of Cu and with changing Cu deposition rates, in an attempt to alter and correlate the Cu-related defects with the cell performance. Detailed material and cell characterization was performed by dark and light I-V measurements, determination of contact resistance and cell parameters, C-V measurements, SIMS depth profiling, and carrier transport analysis.

7.2 Experimental Techniques

CdS films were first deposited on a textured SnO_2 /glass substrate by the solution growth technique and treated with a $\text{CdCl}_2:\text{CH}_3\text{OH}$ solution and annealed in a furnace at 450°C in N_2 ambient, as described in Section 3.2. Polycrystalline CdTe films with a thickness of $\sim 2.6\ \mu\text{m}$ were grown on the annealed CdS/ SnO_2 /glass substrates by MOCVD under the optimum Te/Cd=6 growth ambient. After the CdTe deposition, CdTe/CdS structures were treated in the optimum 50% concentrated $\text{CdCl}_2:\text{CH}_3\text{OH}$ solution (Section

6.3) to enhance the grain re-growth and to improve the CdTe film quality. Ohmic back contacts were formed on the CdTe surface by sequentially evaporating Cu and Au. The thickness of the Cu layer was varied in the range of 0 to 300 Å, and the Cu deposition rate was changed from 0.1 Å/sec to 1 Å/sec. After the metallization, the cells were annealed at 150°C in Ar ambient for 90 min. Cell fabrication was completed by etching the CdTe surface in 0.1% Br₂:CH₃OH, followed by a DI water rinse and N₂ blow-dry. The Br₂:CH₃OH etch after the metallization and 150°C anneal gave us more reproducible results. Surface oxide formation during the annealing process at times degrades cell performance, if the Br₂:CH₃OH etching is performed before the metallization. The Br₂:CH₃OH treatment removes the residual surface oxides underneath the Au/Cu region and increases V_{oc} by a chemical interaction at the grain boundaries [8].

Several techniques were utilized to determine the atomic distribution of Cu, Te, and Cd and characterize the defects, doping concentration, electrical properties, and carrier transport mechanism in the finished devices. C-V measurements were made on the cells with a 1 MHz Boonton capacitance meter. The acceptor density corresponding to each bias voltage was obtained by determining the slope of $\Delta(1/C^2)$ vs ΔV with $\Delta V = 0.2$ Volt at each bias point. The J-V-T data was measured in the temperature range of 230-310 K at 10 K intervals. A multivariable regression analysis was used to obtain J₀, A (diode ideality factor), R_s and R_{sh} at each temperature, as mentioned in Section 3.4. The

temperature dependence of the above parameters was used to determine the current transport mechanisms in devices fabricated with varying Cu thickness in the Au/Cu contact. The carrier transport theory and analysis are summarized in Section 2.4. The J-V-T measurements were performed in the temperature range of 230-310 K because below 230 K, it was difficult to fit the data to a single exponential diode model.

Depth distribution of Cu, Au, Cd, and Te through the various cell layers was monitored by depth profiling with an ATOMIKA-ADIDA 3500 SIMS system. Profiling was done with a 40 nA, 12 keV O_2^+ beam. The beam was generally rastered over a 600 micron square area when profiling through the region of Cu/CdTe interface and then the raster area was reduced to 200 micron square for a faster profile through the much thicker CdTe/CdS layers. Signals of the monoatomic positive ions were recorded. Detection was only from the central 30% of the rastered area in order to avoid crater edge effects. Profiles are terminated when the eroded crater penetrated through the CdTe/CdS layers to the SnO_2 /glass interface.

There are a number of well known complexities in the interpretation of SIMS depth profiles. The technique provides a reliable relative indication of impurity concentration when the impurity is dilute and the matrix is homogeneous. In the present case, analysis is performed through a series of layers, Au/Cu/CdTe/CdS, in each the detection sensitivity of a species is unknown. Moreover, the detection sensitivity for each

species will vary from one layer to the next and where concentration is high, a signal may not linearly relate to atomic concentration. In drawing conclusions from the SIMS analysis, we used only the relative variation of a particular signal with depth through a single layer of the structure to represent relative variation of concentration. In addition, we used ratios of signals from different samples to represent ratios of atomic concentrations. These analyses do not involve any assumptions concerning detection sensitivity nor how such sensitivity might vary as an interface is crossed. Further complications arise in the establishment of the positions of interfaces in the SIMS profile. The first concern is that, with the TENCOR profileometer, the surface of the solar cells was found to be "rough", with topographical irregularities of the order of 200 nm. This is perhaps not surprising since the samples are polycrystalline and grown on glass. But it does mean that the record of buried interfaces will be "smeared" by this amount. Moreover, it is well known that collisional mixing will further distort the indication of an interface. A rough indication of distortion in the metallic layers can be extrapolated from the measurements of King and Webb [9] on an interface between silver isotopes, which results in an interface width of 10 nm for the conditions of the present experiment. The inherent roughness of the samples will thus limit any attempt to establish an interface position. Another complexity stems from possible interference from doubly ionized Te with the Cu^+ ions at mass 63 and 65. To correct for this, the signal of mass 128 Te^{2+}

(mass to charge ratio of 64) was monitored and the Te^{2+} signals at masses 126 and 130 were calculated using the well known isotope ratios; these were then subtracted from the signals at mass to charge ratios 63 and 65 to give the true signals from Cu^+ . The resulting copper signals were consistent with generally accepted isotope ratios.

7.3 Results and Discussion

A systematic study was conducted by changing Cu thickness and deposition rate to understand the correlations between Cu diffusion, doping concentration, CdTe surface stoichiometry, carrier transport mechanisms and cell performance. All the cells were subjected to the same contact formation scheme involving Au/Cu deposition, 150°C annealing in Ar ambient, followed by a $\text{Br}_2:\text{CH}_3\text{OH}$ etch.

7.3.1 The Effects of Cu on CdTe Cell Performance

In order to study the effects of copper on CdTe/CdS solar cell performance, CdTe cells were fabricated with 500Å Au, 400Å Au/100Å Cu, and 200Å Au/300Å Cu contacts and the cell parameters were measured. Notice that total contact metal thickness was 500 Å in each case and the Cu deposition rate was fixed at 0.3 Å/sec. The cell data in Table 7.1 show that the addition of 100 Å Cu in the CdTe cell contact reduces the series resistance significantly (2.8 as opposed to 20.46 $\Omega\text{-cm}^2$). However, excess Cu (300 Å

Table 7.1 CdTe solar cell parameters with different Au/Cu contact

	500 Å Au	400 Å Au 100 Å Cu	200 Å Au 300 Å Cu
V_{oc} (mV)	707.5	709.1	All cells are shorted
J_{sc} (mA/cm ²)	22.846	23.465	
R_s (Ω -cm ²)	20.46	2.80	
R_{sh} (Ω -cm ²)	530.5	395.06	
Fill factor	0.576	0.604	
Eff (%)	9.32	10.06	

as opposed to 100 Å) shorted the cell: Thus, the use of Cu forms a better ohmic contact to CdTe, but excess Cu may diffuse into the CdTe film and short the device. As pointed out before, Cu diffusion could form shunt paths or recombination centers to degrade the cell performance.

The SIMS records were used to monitor the penetration of Cu into the CdTe layers. Figure 7.1a shows the SIMS record of Cu^+ ions as a function of depth through the CdTe layer for a sample with a 400 Å Au and 100 Å Cu metallization on CdTe with the Cu deposited at a rate of 0.3 Å/sec. The background signals for the copper ion from the as-grown CdTe (i.e. without the Au/Cu films) was substantially less than unity on the same scale and therefore negligible (Figure 7.1b). The Cu signal drops from its peak at the Cu/CdTe interface by an order of magnitude in an eroded depth of about 1 μm which is substantially greater than any distortions related to original surface irregularities (estimated at 200 nm) or collisional mixing (estimated as 10 nm). The study was repeated on a sample which had been annealed at 150°C for 90 minutes and surprisingly no significant change in the profile was observed (Figure 7.1c). It is clear that Cu has penetrated into the CdTe, exhibiting a diffusion-like profile, and retains a significant concentration even at a depth of 2.6 μm where the CdTe/CdS interface is located. Moreover, the penetration is not affected by contact anneal which leads us to conclude that the Cu observed in the CdTe arrives by diffusion during the metallization process and

Figure 7.1 SIMS record of Cu^+ ions through the CdTe layer for a Au/Cu/CdTe/CdS cell structure. The detection limit for Cu is shown by dotted line. The statistical error for each data point is the square root of the SIMS signal.

not as a result of heat treatment. Cu diffusion into the CdTe has been reported on a Au-Cu alloy contact with single crystal CdTe [10]. For polycrystalline CdTe solar cells, the penetration of the Cu into the CdTe might be enhanced by diffusing along grain boundaries. The ionic radius of Cu^+ is close to that of Cd^{2+} , making substitution for Cd easy [11]. Diffusion along a grain boundary is also easier because of the small radius of Cu^+ . These mechanisms explain how Cu could get incorporated into the bulk of the device during the Au/Cu metallization. At this time, there is no satisfactory explanation of why the penetration of Cu is not further affected by the annealing process. Even though the 150°C heat treatment does not change the Cu profile, it may form Cu_xTe to reduce the contact resistance [8] and help some Cu interstitials occupy Cd site (Cu_{Cd}) [5] to increase the doping concentration.

The SIMS records were also used to study the distribution of Cd and Te at the Cu/CdTe interface. Figure 7.2 shows the ratio of Cd to Te SIMS signals in the region near Cu/CdTe interface. The ratio has been normalized to unity, deep in the sample (at a depth of 1600 Å), where the composition of the CdTe is expected to be stoichiometric. In the neighborhood of the interface, the efficiency with which ions are created may vary with composition; but this will influence all species in roughly the same manner. Thus, the ratio of two signals is a useful qualitative indicator of the ratio of the elemental density of the two species. We observe that the ratio exceeds unity close to the interface

Figure 7.2 The Cd/Te ratio of SIMS signals near the Cu/CdTe interface.

indicating that there is an excess of Cd over the stoichiometric ratio in this region. For completeness, the same ratio was measured for as-grown CdTe without metallization and the signal ratio is constant with erosion depth (Figure 7.2). Notice that the as-grown CdTe sample in Figure 7.2 was not etched by $\text{Br}_2\cdot\text{CH}_3\text{OH}$, but the finished cell was. This etching process can leave a Cd deficient surface [8], and yet we observe a Cd pile-up in the cell, therefore, it is reasonable to conclude that the metallization process tends to enhance the Cd/Te ratio near the Cu/CdTe interface. This increase in the Cd/Te ratio suggests a Cd out-diffusion or Te depletion near the interface. Cd out-diffusion and segregation at the grain boundaries near the Cu/CdTe interface is a more likely mechanism for this behavior because the self-diffusion coefficient of Cd in CdTe is much higher than that of Te [12]. Other investigators have also observed a similar Cd out-diffusion effect and a thin AuTe_x interlayer formation when a Au contact is formed in a gold ion solution [1]. Because of the observed Cd segregation at the surface, Cd vacancy concentration below the surface is expected to be higher after the Au/Cu deposition.

Since Cu can act as an acceptor in the CdTe films, C-V measurements were performed on the CdTe cells to investigate any changes in the doping concentration in the CdTe because of the Cu incorporation in the film. Figure 7.3 shows the acceptor concentration in CdTe cells with 500Å Au and 400Å Au/100Å Cu metal contacts. The estimated depletion width in these devices is about 2.0 μm at 1 volt reverse bias. The

Figure 7.3 The acceptor concentration in the CdTe layer by C-V measurement with different metal contact on CdTe solar cells.

variation of the junction capacitance value due to the uncertainty in contact area and parasitic capacitance causes difficulty in converting bias voltage to exact depletion width. However, the acceptor concentration values, determined from the slope, are reliable. Figure 7.3a shows that, consistent with the SIMS profile of Cu, the acceptor concentration decreases monotonically from the CdTe surface toward the CdTe/CdS interface for the cell with 400Å Au/100Å Cu contact. It was also found that, unlike the cells with Au/Cu contact, acceptor concentration was lower and nearly flat for the cell with only Au contact (Figure 7.3b). Therefore, the acceptor profiles obtained from the C-V measurements must result from a fraction of Cu atoms occupying the substitutional Cd-site [10]. This result supports and provides the evidence of Cu diffusion into CdTe during the Au/Cu deposition coupled with enhanced acceptor concentration and improved ohmic contact.

Notice that the measured acceptor concentration is in the range of 10^{15} to 10^{16} cm^{-3} . For comparison we have estimated the number density of the copper by a SIMS profile performed with a Cs^+ probing beam and with monitoring of the CsCu^+ and CsTe^+ signals. As indicated by Gnaser and Oechsner [13], diatomic CsX^+ signals exhibit less matrix dependent effects and can be reliably related to relative densities in the substrate through the polarizability of the species X. On this basis, the relative magnitudes of CsCu^+ and CsTe^+ signals suggest a Cu density of a few times 10^{19} cm^{-3} at a depth of about 1 micron, several orders of magnitude greater than the acceptor concentration. This

result suggests the possibility of the self-compensation [14] in the CdTe and the formation of Cu interstitials or Cu-defect complexes, which may not act as acceptors but do contribute to shunt and recombination centers. The observation that carrier density from Cu doping is substantially less than the copper density has previously been reported by several investigators [6,15]. In addition to the effect of excess Cu, the high Cd vacancy concentration below the surface resulting from the Au/Cu deposition may also affect the cell performance, because trap centers in the vicinity of $E_v+0.6$ eV have been attributed to Cd vacancy or its related complexes [16].

7.3.2 Effects of Cu Thicknesses on Cell Performance

The above results indicate that the thickness of Cu plays a critical role on the CdTe solar cell performance with Au/Cu contacts. In order to study the optimum Cu thickness for this contact system, a series of experiments were carried out by varying the Cu thickness in the range of 0 to 150 Å. Au thickness was maintained at 400 Å, Cu deposition rate was kept at 0.3 Å/sec. Detailed light and dark I-V measurements were performed to study the changes in R_s , R_{sh} and cell performance. Cell parameters in Figure 7.4 show that both R_s and R_{sh} decrease with the increase in Cu thickness beyond 25 Å. This is probably because the increase in Cu thickness results in a better ohmic contact which reduces the R_s , but the excess Cu causes shunt paths or recombination centers,

Figure 7.4 R_s and R_{sh} of the CdTe solar cells with different Cu thickness in the Au/Cu contact.

which tend to lower the R_{sh} and cell performance. These results further support the dual role of Cu on the CdTe cell performance. For the deposition temperature and rate used in this study, it was also found that Cu thickness of 75 to 100 Å was optimum for the contact because it gives reasonable series and shunt resistance as well as cell performance (Figures 7.4 and 7.5).

SIMS measurements were performed on the cells with 50 Å and 150 Å Cu contacts to investigate the correlation between Cu thickness and Cu distribution and incorporation in the CdTe films. Figure 7.6 shows the SIMS profiles of Cu in the CdTe films of these two cells, with the profiles normalized to constant beam current density. At all depths, the density of Cu for the 150 Å Cu overlayer is significantly higher than that for the 50 Å layer. Thus, increased Cu thickness increases Cu density in the cell, reduces R_{sh} and leads to degradation in cell performance.

7.3.3 Effect of Cu Thickness on Carrier Transport Mechanism in the CdTe/CdS Solar Cells

In order to understand the effects of Cu on the carrier transport mechanism in CdTe solar cells, J-V-T measurements were performed on the cells with 50 Å, 100 Å, and 150 Å Cu contacts, deposited at 0.3 Å/sec with Au thickness of 400 Å. Ideality factor (A) and reverse saturation current density (J_0) were determined as a function of temperature,

Figure 7.5 CdTe solar cell efficiency with different Cu thickness in the Au/Cu contact.

Figure 7.6 Cu depth profiles from SIMS measurement on the cells with 50Å and 150Å Cu contact. The detection limit for Cu is shown by dotted line. The statistical error for each data point is the square root of the SIMS signal.

using a multivariable regression analysis by fitting the measured J-V data to Equation (3.11) at each temperature. It was found that the cells with different Cu thickness show a temperature-independent ideality factor (Table 7.2) which indicates that either straight depletion-region recombination or interface recombination controls the current transport [17,18]. Moreover, the slope of $\ln(J_0 T^{-2.5})$ vs $1000/T$ gave an activation energy of 0.767eV, 0.744eV, 0.839eV for the cells with 50 Å, 100 Å, and 150 Å Cu contact, respectively (Figure 7.7), which is approximately equal to half of the CdTe bandgap. This indicates that the depletion region recombination, rather than the interface recombination, dominates the current transport [19]. Therefore, it is concluded that even though Cu affects the shunt and series resistance, it does not introduce tunneling or interface recombination, and the current transport mechanisms remains essentially unaffected.

7.3.4 Effect of Cu Deposition Rate on Cell Performance

The above results indicate that the optimization of Au/Cu metallization process is critical in order to reduce the diffusion of Cu in CdTe/CdS solar cells without sacrificing good ohmic contact. Based on the above finding, Cu layer thickness was fixed at 100 Å to preserve low R_s (Figure 7.4) in the following experiments. Since it was found that Cu diffusion occurs during the Cu deposition process, rather than during the subsequent heat

Table 7.2 J-V-T parameters for CdTe cells with different Cu thicknesses in the contact

T (K)	50 Å Cu		100 Å Cu		150 Å Cu	
	$J_0(\text{A/cm}^2)$	A	$J_0(\text{A/cm}^2)$	A	$J_0(\text{A/cm}^2)$	A
230	1.01E-13	1.83	7.05E-14	1.86	2.10E-14	1.56
240	3.31E-13	1.79	1.70E-13	1.77	5.19E-14	1.50
250	1.47E-12	1.78	8.86E-13	1.78	3.00E-13	1.52
260	8.29E-12	1.82	3.48E-12	1.76	1.88E-12	1.56
270	3.01E-11	1.81	1.43E-11	1.74	1.28E-11	1.62
280	1.04E-10	1.80	5.80E-11	1.75	3.90E-11	1.57
290	4.13E-10	1.83	1.58E-10	1.70	1.70E-10	1.59
300	1.22E-09	1.83	5.86E-10	1.71	4.71E-10	1.55
310	3.50E-09	1.83	1.75E-09	1.69	1.26E-09	1.51

Figure 7.7 Plot of $\ln(J_0 T^{2.5})$ vs $1000/T$ for CdTe/CdS cells with 50 Å, 100 Å, and 150 Å Cu contact.

treatment, attempts were made to reduce Cu diffusion by changing the Au/Cu deposition rate.

Table 7.3 shows the electrical parameters of the CdTe solar cells fabricated with three different deposition rates during Au/Cu metallization. The data in Table 7.3 clearly show that the fast Au/Cu deposition rate ($1.7 \text{ \AA/sec}$ for Au and $1 \text{ \AA/sec}$ for Cu) degraded the cell performance compared to the slower Au/Cu deposition rate ($0.2 \text{ \AA/sec}$ for Au and $0.1 \text{ \AA/sec}$ for Cu). The fact that R_{sh} increases as the deposition rate slows down (Table 7.3), suggests that the density of the shunt paths or recombination centers have been reduced. The above hypothesis was further verified by the dark I-V measurements, which revealed a lower reverse saturation current density (J_0) for the cell fabricated with the lower Cu deposition rate (Table 7.3). In the CdTe/CdS solar cells, the decrease in J_0 usually represents a reduction in the bulk defect and interface state density, and results in better cell performance.

In order to improve the fundamental understanding of the effect of Cu deposition rate further, C-V measurements were performed on the cells to investigate the change in dopant concentration. Figure 7.8 shows that the acceptor concentration was larger for the cell fabricated with higher Au/Cu deposition rate. This result suggests that higher deposition rate seems to enhance the acceptor concentration in the CdTe. SIMS analysis was also performed on these samples. The Cu distribution in the CdTe film was found

Table 7.3 CdTe solar cell parameters with different Au/Cu deposition rates

Au/Cu deposit rate	1.7Å/1Å/sec	0.6Å/0.3Å/sec	0.2Å/0.1Å/sec
V_{oc} (mV)	687.6	726.2	714.6
J_{sc} (mA/cm ²)	20.776	21.673	21.356
R_s (Ω-cm ²)	3.94	4.49	3.44
R_{sh} (Ω-cm ²)	1283.83	1584.61	2007
Fill factor	0.61	0.621	0.65
Eff (%)	8.71	9.78	9.93
J_0 (A/cm ²)	2.42×10^{-10}	1.6×10^{-10}	4.71×10^{-11}

Figure 7.8 The acceptor concentration in the CdTe layer by C-V measurement with different Au/Cu deposition rate for contact on CdTe solar cells.

to be independent of Cu deposition rate. However, the excess Cd/Te ratio at and near the Cu/CdTe interface increased with Au/Cu deposition rate (Figure 7.9). The precise mechanism responsible for the higher deposition rate enhancing the Cd out-diffusion toward the surface is not understood at this time. It could be related to the microstructure of the Cu film. The Cu layer deposited at a fast rate is expected to have smaller grain size. Therefore, the out-diffusion of Cd atoms from the CdTe film underneath could be enhanced because of more available grain boundaries. Because of the observed excess Cd at the surface, Cd vacancy concentration below the surface may be higher for the fast Au/Cu deposition rate. Since the Cu atoms could go into the vacant Cd sites and become electrically-active, the amount of electrically-active Cu atoms should be higher for the fast Cu deposition rate, even though the total amount of Cu in the films does not change much with Cu deposition rate. This could explain why the C-V measurement gave a larger acceptor concentration for the cell fabricated with a higher Au/Cu deposition rate (Figure 7.8). In addition, an increase in the V_{oc} -related trap density [16] near the surface, degrades the cell performance.

7.4 Conclusion

Cu plays a dual role in the CdTe/CdS solar cells with Au/Cu contact. On one hand it helps in the formation of better ohmic contact to CdTe and increases the acceptor

Figure 7.9 The Cd/Te ratio of SIMS signals near the Cu/CdTe interface for the cells with different Au/Cu deposition rate on the contact.

doping concentration, but on the other hand, excess Cu diffuses all the way to the CdTe/CdS interface, forms recombination centers and shunt paths, and degrades the cell performance. Both SIMS and C-V measurements confirm the incorporation of Cu into the bulk of the CdTe films. Monotonically decreasing Cu concentration toward the CdTe/CdS interface suggests that diffusion is the most probable mechanism for Cu incorporation. It was found that the Cu thickness and Cu deposition rate during the Cu deposition process, rather than the subsequent heat treatment, influences the Cu incorporation. It was found that both R_s and R_{sh} decrease with the increase in Cu thickness. Depletion region recombination was found to dominate the current transport in the CdTe solar cells. The transport mechanism remains the same in spite of Cu incorporation into the bulk and interface. Higher Au/Cu deposition rate results in Cd pile-up or out-diffusion toward the CdTe surface, leaving more Cd vacant sites below the surface. This causes an increase in dopant concentration but could also result in higher defect density and reduced cell performance. Finally, a combination of optimum thickness and a slower deposition rate of Cu was used to achieve high efficiency CdTe solar cells.

CHAPTER VIII

DEVELOPMENT OF LARGE GRAIN AND SINGLE CRYSTAL CdTe THIN FILM SOLAR CELLS

8.1 Introduction

One of the principal barriers to obtaining higher efficiency CdTe solar cells is the resistive and/or unstable contact to p-type CdTe [1]. The difficulties come from the dopant compensation mechanisms in II-VI semiconductors and the large work function for p-type CdTe [2]. It was shown in Chapter VII that copper plays a dual role in the CdTe/CdS solar cells fabricated with a Au/Cu contact. On one hand it helps in the formation of better ohmic contact to CdTe and increases the acceptor doping concentration, but on the other hand, excess Cu diffuses all the way to the CdTe/CdS interface, forms recombination centers and shunt paths, and degrades the cell performance. However, the source and magnitude of Cu migration need to be understood in order to control the Cu incorporation into the CdTe films and to enhance the solar cell performance intelligently. In this chapter, an attempt was made to understand the correlation between the CdTe grain size and the Cu distribution in the CdTe films. CdTe thin films with different degrees of crystallinity and grain sizes were grown by varying

substrates and growth conditions. CdTe solar cells were then fabricated on these CdTe films by lift-off/etch-back and film transfer techniques in an attempt to understand the effect of crystallinity and grain boundaries on Cu incorporation in the CdTe films and its impact on the CdTe cell performance. Detailed material and cell characterization was performed by scanning electron microscopy (SEM), X-ray diffraction (XRD), photoluminescence (PL), and secondary ion mass spectroscopy (SIMS).

8.2 Growth of CdTe Films with Different Degrees of Crystallinity

In order to understand the role of grain boundary on Cu incorporation, CdTe films with different degrees of crystallinity and grain sizes were grown by selecting different substrates and growth conditions. The CdTe layer grown on a CdS/GaAs substrate is expected to have higher degree of crystallinity (due to the single crystal GaAs substrate) than the CdTe film grown on a CdS/SnO₂/glass or SnO₂/glass amorphous substrate. However, because of the inferior crystallinity of the CdS layer, which is formed by a low-temperature solution growth process, the crystallinity of the CdTe on CdS/GaAs was not as good as the CdTe grown directly on the GaAs substrate. CdTe/CdS/SnO₂/glass, CdTe/CdS/GaAs, and CdTe/GaAs structures were grown to achieve different degrees of crystallinity in the CdTe films. A 600 Å thick CdS layer was first grown on a (100) GaAs substrate by solution growth, followed by the growth of a 2.6 μm thick CdTe layer

by MOCVD to complete the CdTe/CdS/GaAs structure. For the CdTe/GaAs structure, CdTe layer was directly grown by MOCVD on a (100) with 10° off to (110) GaAs substrate.

SEM and XRD measurements were performed to assess the crystallinity of the CdTe films grown on different substrates and under different growth conditions. X-ray diffraction measurements were first performed to study the orientation and crystallinity of the CdTe films (Figure. 8.1). For the CdTe/CdS/SnO₂/glass structure, which was used to fabricate CdTe cells, the XRD data revealed a polycrystalline structure with various grain orientations (Figure. 8.1a). In contrast to the CdTe/CdS/SnO₂/glass structure, the XRD patterns for the CdTe/CdS/GaAs structure showed a very intense {400} peak located at $2\theta=56.75^\circ$ with full-width at half-maximum (FWHM) of 986 arc sec, together with some smaller peaks of other orientations (Figure. 8.1b). This indicates a polycrystalline CdTe layer in the CdTe/CdS/GaAs structure with preferential (100) orientation. XRD patterns could not be obtained for the CdTe/GaAs structure by using the Phillips PW 1800 diffractometer because of the orientation of the GaAs substrate, which was (100) with 10° off to (110). In order to investigate the quality of the CdTe layer, Double Crystal Rocking Curve (DCRC) X-ray diffraction measurements were performed on the CdTe/GaAs structure. A Bede Scientific QC2a diffractometer with a 400 Si monochromator and Cu K $_{\alpha}$ radiation was used to measure the {400} CdTe rocking curve.

Figure 8.1 XRD patterns for the CdTe in the CdTe/CdS/SnO₂/glass(a), and in the CdTe/CdS/GaAs(b). DCRC pattern for the CdTe in the CdTe/GaAs(c).

The FWHM value for the CdTe grown on GaAs substrate was 211 arc sec (Figure. 8.1c), compared to a 986 arc sec for the CdTe grown on CdS/GaAs substrate. This indicates a highly oriented, high quality CdTe layer in the CdTe/GaAs structure.

SEM measurements were performed in order to investigate the microstructure of various CdTe layers grown in this study. The CdTe layer grown on CdS/SnO₂/glass substrate showed a loose, random grain structure with much smaller grain size (about 1-2 μm), implying a larger grain boundary surface area per unit volume, S_v (Figure 8.2a). The S_v value can be obtained by[3]

$$S_v = 2P_L \quad , \quad (8.1)$$

where P_L is the average number of intersections of a randomly oriented test line of unit length with the observed grain boundaries. The S_v value for the CdTe layer grown on CdS/SnO₂/glass substrate was found to be about 1.66 μm⁻¹. In contrast, the average grain size of the CdTe layer on CdS/GaAs was approximately 10 μm, along with some smaller grains (Figure. 8.2b). By using equation (8.1), the S_v value was estimated to be about 0.24 μm⁻¹ for the CdTe film grown on CdS/GaAs substrate. SEM measurements on the CdTe grown directly on a GaAs substrate showed a smooth, mirror like surface morphology with no grain boundaries (Figure 8.2c), indicating a single crystal CdTe structure. Thus, SEM measurements are consistent with the XRD measurements, supporting the successful growth of CdTe films with different degrees of crystallinity.

(a) CdTe/CdS/SnO₂/glass 3 μ m

(b) CdTe/CdS/GaAs 12 μ m

(c) CdTe/GaAs 10 μ m

Figure 8.2 SEM measurements on the CdTe layers for (a) CdTe/CdS/SnO₂/glass, (b) CdTe/CdS/GaAs, and (c) CdTe/GaAs structures.

8.3 Investigation of Selective Etch for CdTe, CdS, and GaAs

In order to investigate the loss mechanisms and intricacies of polycrystalline CdTe/CdS cells, attempts are made to fabricate CdTe solar cells from the CdTe films of different degrees of crystallinity grown in the previous section. In Section 7.3 we showed that Cu from the Au/Cu contact can diffuse along the grain boundaries all the way to the CdS/CdTe interface, causing a decrease in cell performance. By utilizing the single crystal CdTe or large grain polycrystalline CdTe/CdS thin film cell structure, the role of Cu can be better understood because there are less or no grain boundaries for Cu diffusion into the CdTe layer. A comparison of single and polycrystalline CdTe films and cells can significantly enhance the understanding of the role of grain boundaries and provide guidelines toward high-efficiency CdTe solar cells.

In order to accomplish the task of fabricating single crystal or large grain polycrystalline thin-film CdTe solar cell structure, an epitaxial lift-off (ELO)/etch-back process was utilized to separate good quality CdTe or CdTe/CdS films from the GaAs growth substrate. For the thin film separation, an etchant was discovered that selectively etches GaAs rapidly but does not attack CdTe/CdS films. We investigated H_3PO_4 , citric acid, H_2SO_4 , and NaOH in order to develop the selective etch for GaAs and CdTe/CdS. The experimental results are summarized below:

- (a) $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2$ solution etched GaAs substrate as well as CdTe films, therefore, it is

not suitable as a selective etchant.

- (b) Citric acid:H₂O₂ etched GaAs substrate as well as CdTe films, therefore, it is also not suitable for selective etch of GaAs and CdTe. However, it was found that this solution did not attack the CdS film and could be used to selectively etch CdTe without affecting CdS layers.
- (c) H₂SO₄:H₂O solution etched GaAs at an etch rate of 0.017 mil/hour, and reacted with CdS slowly, peeling off the CdTe film. Therefore, this solution can not be used for selectively etching the GaAs and CdTe/CdS devices, but it can be used to selectively etch CdS without affecting CdTe layers.
- (d) NaOH:H₂O₂ dissolved GaAs substrate in 24 hours without reacting with CdTe/CdS films, therefore, it is the best candidate for selective etch.

Leech et al. [4] reported that KI:I:HBr solution etches CdTe thin film without affecting the GaAs substrate, however, this is the first time an etchant is found which can etch GaAs substrate without reacting with CdTe or CdS material. In addition, we also found that the citric acid and sulfuric acid could preferentially etch CdTe and CdS, respectively.

8.4 Development of Large Grain CdTe/CdS and Single Crystal CdTe Thin Film Structures by Selective Etching

Attempts were made to fabricate large grain polycrystalline and single crystal CdTe/CdS cells by lift-off/etch-back process based on the NaOH:H₂O₂ selective etchant. Single-layer CdTe, two-layer CdTe/CdS, and three-layer CdTe/CdS/ITO were successfully lifted off from GaAs substrate for the first time. A 2000 Å thick ITO was deposited on the GaAs substrate, followed by the selective etch, and then transferred to a SnO₂/glass substrate to measure the resistance between the ITO and SnO₂ layers in order to assure a good conducting path between them. The I-V characteristic was found to be linear (ohmic), with a contact resistance $< 10 \Omega\text{-cm}^2$, between ITO and the SnO₂ layers. This is the first time a 2000 Å thick conductive film of ITO has been bonded to a SnO₂/glass substrate with such a good ohmic contact.

8.4.1 Two-step Transfer Process

Several different approaches were pursued to achieve large grain CdTe/CdS and single crystal thin-film CdTe solar cells. The first design was based on a two-step film transfer method [5] to achieve a Au/Cu/CdTe/CdS/(ITO or SnO₂)/glass cell scheme which is identical to the polycrystalline CdTe cell structure. In order to complete this cell structure, a two-step film transfer procedure (first to the diaphragm, then to the host

substrate) was developed. Fabrication process for this cell is shown in Figure 8.3. Unfortunately, this process was not very successful because of the difficulties in double transfer. When the CdTe/CdS/ITO/black wax structures were brought to the diaphragm and the black wax was removed, the thin films stuck on the diaphragm and could not be transferred to the host substrate probably because of the larger sticking coefficient between the CdTe and diaphragm. Another attempt was made by using a filter paper instead of a diaphragm as a transfer medium. Even though the lift-off thin film was successfully transferred to the host substrate, it peeled off, probably because of the surface roughness of the CdTe/CdS/ITO structure. Since the Van der Waals forces hold the thin film and substrate together in this scheme, both contacting surfaces need to be very smooth and flat. Therefore, no device using the two-step transfer method could be completed because of the above problems.

8.4.2 One-step Transfer Process

The two-step film transfer procedure was not successful, therefore, a one-step film transfer method was developed to achieve the device fabrication. This procedure is described in Figure 8.4. The thin film CdTe solar cell devices formed by this method showed a diode I-V characteristic consistent with the photovoltaic effect. However, these devices showed high series resistance because of the high contact resistance between the

8.4 Development of Large Grain and Single Crystal CdTe Thin Film Structures by Selective Etching

Figure 8.3 Large grain thin-film CdTe/CdS solar cell fabrication procedures with two-step film transfer.

8.4 Development of Large Grain and Single Crystal CdTe Thin Film Structures by Selective Etching

Figure 8.4 Large grain thin-film CdTe/CdS solar cell fabrication procedures with one-step film transfer.

CdS film and SnO_2 /glass substrate.

Next, we attempted the lift-off process by utilizing a bonding technique to achieve a better contact and device performance. As shown in Figure 8.5, a $400\text{\AA}$ Au/ $100\text{\AA}$ Cu metal contact was first deposited on the CdTe/CdS/GaAs structures and then the structure was inverted and bonded to a glass substrate with an In/Au solder or Ag-epoxy. The thin films were then separated from the GaAs substrate by selectively etching the GaAs with $\text{NaOH}:\text{H}_2\text{O}_2$ solution. After the GaAs substrate removal, an ITO film was deposited to complete the fabrication of ITO/CdS/CdTe/Cu/Au/glass cell structures. Large grain thin-film CdTe/CdS solar cells were successfully fabricated by lift-off process with Ag-epoxy and In/Au solder bonding. The best cell efficiency was 3.4% for Ag-epoxy bond and 2.9% for In/Au bond.

Finally, an attempt was made to fabricate an ITO/CdTe Schottky junction solar cell on the single crystal CdTe layer. After the Au/Cu/CdTe structure was lifted off and bonded onto the SnO_2 /glass substrate, the CdTe surface was subjected to Ar ion-milling before the ITO deposition. This removes the oxide and impurities from the CdTe surface, resulting in a better ITO/CdTe Schottky junction. The best cell efficiency achieved for the single crystal Schottky junction solar cells was 5.1%. Higher cell performance can be achieved by optimizing the process conditions and parameters.

The separation of epitaxial CdTe has been demonstrated for CdTe grown onto a

8.4 Development of Large Grain and Single Crystal CdTe Thin Film Structures by Selective Etching

Figure 8.5 Large grain thin-film CdTe/CdS solar cell fabrication procedures with a metal bonding technique.

Si substrate [6]. In this work, we successfully separated CdTe and CdTe/CdS layers grown on GaAs to complete the fabrication of ITO/CdS/CdTe/Cu/Au/glass (p-n heterojunction), and ITO/CdTe/Cu/Au/glass (Schottky junction) cell structures, in which the incident sun light enters through the ITO layer. This is the first time a single crystal and a large grain polycrystalline thin-film CdTe solar cell structure has been fabricated by selective etch and substrate transfer. Exact reason(s) for the low cell efficiency of the lift-off structure is not fully understood at this time, some of the probable culprits for the low efficiency, such as contact bonding, lift-off film quality, and Ga diffusion from the GaAs substrate, are investigated in the following sections.

8.5 Investigation of the Quality of the ELO Surface and Structures

In order to investigate the ELO thin film quality after the selective etch and substrate transfer, Double Crystal Rocking Curve (DCRC) X-ray diffraction measurements were performed on the CdTe/CdS layers before and after the separation process. A Bede Scientific QC2a diffractometer with a 400 Si monochromator and Cu K α radiation was used to measure the {400} CdTe rocking curve. The full-width at half-maximum (FWHM) value for the as-grown CdTe/CdS on the GaAs substrate was 986 arc sec and remained unchanged after the separation (Figure 8.6). This result suggests that the quality of double layer ELO films does not change during the lift-off process. Unlike the case

Figure 8.6 Rocking curves for the 400 CdTe on CdS/GaAs substrate before and after the separation from GaAs substrate.

of CdTe/CdS, DCRC X-ray measurements on the single layer CdTe on GaAs gave a FWHM value of 211 arc sec, which increased to 320 arc sec after the lift-off (Figure 8.7). Thus, the presence of CdS layer between the GaAs and CdTe seems to reduce the quality of CdTe.

Rocking Curves were also recorded for the CdTe surface selectively etched from the GaAs substrate. Due to the large lattice mismatch at the GaAs/CdTe interface (lattice constant $a=5.653 \text{ \AA}$ for GaAs, while $a=6.481 \text{ \AA}$ for the CdTe bulk), the CdTe material at the CdTe/GaAs interface is expected to be more highly strained than the CdTe material at the free interface. This could result in smaller lattice spacing in this CdTe film compared to the bulk CdTe, in order to release the lattice mismatch [7,8]. The Bragg angles θ for the $\{400\}$ peaks should be 33.014° for GaAs and 28.375° for CdTe, a difference of 4.639° . A spacing of 5.228° was observed between the $\{400\}$ peaks of CdTe and GaAs, which is close to the ideal lattice separation for the two materials. The top CdTe surface of the sample was then bonded to the glass substrate, and the GaAs substrate was etched away from one half of the sample to reveal the CdTe layer underneath. X-ray scans were then performed on both halves. The difference in the $\{400\}$ peak locations was reduced from 5.228° to 3.857° . Using GaAs as the reference lattice parameter, the corresponding CdTe lattice constant near the CdTe/GaAs interface was calculated to be $6.317 \text{ \AA}$, which is smaller than the ideal CdTe lattice parameter of

Figure 8.7 Rocking curves for the 400 CdTe near the CdTe/air interface and near the CdTe/GaAs interface.

6.481 Å. Therefore, the above results confirm the lattice distortion near the GaAs/CdTe interface and suggest that the broadening of the CdTe rocking curve after the lift-off (i.e. near the original CdTe/GaAs interface) is probably due to lattice mismatch. Notice that this assumes that the Ag-epoxy held the CdTe rigidly in place and that the change in Bragg angle was not due to bending of the CdTe thin film.

Room temperature PL measurements were performed on the CdTe before and after the ELO process. Since the absorption coefficient of CdTe at 600 nm (wavelength of the incident laser beam) is 10^5 cm^{-1} , over 90 % of incident beam is absorbed within 250 nm region near the tested CdTe surface. Therefore, the PL spectrum measures the material at the CdTe/air interface before the lift-off process and at the CdTe/GaAs interface after the lift-off process. Figure 8.8 shows that the CdTe/GaAs interface has three additional PL peaks observed around 838, 852, and 870 nm, in contrast to the CdTe/air interface. This result is consistent with the XRD measurements of the lattice distortion and suggests that the additional peaks are related to defect states near the CdTe/GaAs interface. Time-resolved PL measurements were performed in order to study the effective lifetime (τ_e) of the two interfaces. The effective lifetime includes contributions from bulk and surface recombination. The effective lifetime at the CdTe/GaAs interface is 55 ps, and at the CdTe/air interface is 75 ps. This is primarily due to some degradation of the CdTe surface quality near the CdTe/GaAs interface.

Figure 8.8 PL spectrum of CdTe near the CdTe/air interface before lift-off and near the CdTe/GaAs interface after lift-off.

8.6 Cu Migration in the CdTe Solar Cells with Varying Degree of CdTe Crystallinity

After the fabrication of single crystal and large and small grain polycrystalline thin-film CdTe solar cells, SIMS measurements were performed on the thin film single crystal CdTe cells (ITO/CdTe/Cu/Au/glass), CdTe/CdS cells (ITO/CdS/CdTe/Cu/Au/glass) with large CdTe grains, and the conventional small grain polycrystalline Au/Cu/CdTe/CdS/SnO₂/glass cells. Cu depth profiles in Figure 8.9 clearly show that the Cu concentration in the CdTe/CdS cell structure with a 10 μ m grain size is more than an order of magnitude less than the Cu in the conventional small grain polycrystalline CdTe/CdS solar cell structure with a 1-2 μ m grain size. The Cu concentration in the single crystal CdTe structure is much lower and is in fact below the detection limit of our SIMS system. This suggests that the grain boundaries in the CdTe films are the main conduits for Cu diffusion and are responsible for Cu-induced cell degradation. Therefore, large CdTe grains or less grain boundary surface area per unit volume can mitigate the adverse effect of Cu on the cell performance.

A crude attempt was made to estimate the diffusion coefficient of Cu in the polycrystalline CdTe films from the limited SIMS data. In Section 7.3 we showed that Cu diffusion takes place during the Cu evaporation when the sample temperature is about 80°C. If the Cu diffusion is assumed to be from an infinite source, it will show a

Figure 8.9 Comparison of Cu SIMS profiles in the CdTe layers with different degrees of crystallinity. The detection limit for Cu is shown by dotted line. The statistical error for each data point is the square root of the SIMS signal.

complementary error function profile. The ratio of Cu concentration N_1 and N_2 at the depth x_1 and x_2 in CdTe, respectively, can then be expressed as:[9]

$$\frac{N_1}{N_2} = \frac{\operatorname{erfc}\left(\frac{x_1}{2\sqrt{Dt}}\right)}{\operatorname{erfc}\left(\frac{x_2}{2\sqrt{Dt}}\right)}, \quad (8.2)$$

where D is the diffusion coefficient and t is the diffusion time. The diffusion time is assumed to be equal to the time during the Cu evaporation, since we found in Section 7.3 that Cu diffuses into CdTe during the metallization. D coefficient can be obtained from Equation (8.2) according to[9]

$$D = \frac{1}{4t} \frac{x_1^2 - x_2^2}{\ln\left(\frac{N_2 x_1}{N_1 x_2}\right)}. \quad (8.3)$$

By choosing the two data points at 0.2 μm and 0.4 μm in Figure 8.9 and assuming the ratio of Cu concentration at two different depths is equal to the ratio of SIMS signal, the calculated diffusion coefficient value is found to be $1.5 \times 10^{-12} \text{ cm}^2/\text{sec}$ for Cu diffusion in the 2 μm grain size CdTe. Similarly, the Cu diffusion coefficient is found to be $6.2 \times 10^{-13} \text{ cm}^2/\text{sec}$ in the 10 μm grain size CdTe, which is about three times smaller than the value for small grain CdTe. It is important to recognize that the sample temperature is about 80°C during the evaporation, therefore, the about D values represent Cu diffusion coefficient in polycrystalline CdTe at ~80°C.

Even though we were able to reduce the Cu incorporation in the cells with large grain structure, the cell efficiency was only 3.4% for the large grain CdTe/CdS cell and 5.1% for the ITO/CdTe single crystal cell structure. One possible reason may be that the fast diffusers, such as Ga from the GaAs substrate, get into the CdTe film and degrade the cell performance. This hypothesis was supported by the SIMS measurement on the finished large grain CdTe/CdS devices (Figure 8.10), which showed a significant amount of Ga in the CdS and CdTe layers. Ga out-diffusion during the CdTe growth or the subsequent heat treatment may be responsible for the large amount of Ga observed in the CdTe and CdS layers. Growing a thicker CdS layer to reduce the Ga diffusion is not an acceptable solution for the problem, because CdS film acts as a window layer (Section 4.4) and, therefore, can not be too thick. Contact bonding, which was not perfected or optimized, may also contribute to lower efficiency. Therefore, even though the Cu incorporation in the CdTe was reduced in the large grain CdTe film, a higher defect density because of lattice mismatch and Ga diffusion near the CdTe/CdS interface cause recombination and shunt paths to degrade the cell performance.

8.7 Conclusion

An attempt was made to understand the correlation between the CdTe grain size and the Cu incorporation in the CdTe films. CdTe films with varying degree of

Figure 8.10 SIMS record of Ga, S, and Cd ions near the CdTe/CdS region.

crystallinity were grown in the CdTe/CdS/SnO₂/glass, CdTe/CdS/GaAs, and CdTe/GaAs structures. CdTe/CdS/SnO₂/glass had a CdTe grain size of 1-2 μm , CdTe/CdS/GaAs thin film structure had a CdTe grain size of 10 μm , while the CdTe/GaAs structure had single crystal CdTe. Large grain and single crystal thin film solar cell structures were achieved for the first time in this research by a combination of etch back and film transfer techniques. X-ray diffraction measurements showed that the CdTe/CdS lattice structure and quality does not change appreciably after the lift-off process. A new methodology was developed, using XRD and the selective-etch-process/film-transfer technique, to investigate the CdTe properties near the CdTe/GaAs interface, and assess the lattice mismatch-induced strain, defects, and change in lattice constant. The lattice constant of CdTe at the CdTe/GaAs interface was 6.317 $\text{\AA}$, which is smaller than the ideal lattice constant of 6.481 $\text{\AA}$ for the bulk CdTe. SIMS measurement showed that the Cu concentration in the CdTe/CdS cell structure with large grain size was about two orders of magnitude less than the conventional small grain polycrystalline CdTe/CdS/SnO₂/glass solar cell structure. The Cu concentration in the single crystal CdTe structure was even lower, below the detection limit of SIMS. Even though larger CdTe grains in the CdTe/CdS/GaAs structure reduced the adverse effects of Cu, higher defect density due to Ga diffusion into the CdS and CdTe layers resulted in a lower cell efficiency.

CHAPTER IX

CONCLUSIONS AND FUTURE DIRECTIONS

The overall goal of this research was to bring the polycrystalline CdTe cell efficiency a step closer to the practically achievable efficiency of 18% through fundamental understanding of defects and loss mechanisms, the role of chemical and heat treatments, and investigation of new process techniques. This was accomplished by a combination of in-depth characterization, modeling, material growth, device fabrication, and carrier transport analysis of Au/Cu/CdTe/CdS/SnO₂/glass front wall heterojunction solar cells. Attempts were made to understand the defects and loss mechanisms in each layer and interface.

The first step was to understand, quantify, and reduce the reflectance and photocurrent loss in polycrystalline CdTe solar cells. Model calculations were performed to determine the optimum thicknesses of CdS and SnO₂ films along with appropriate refractive index and thickness of antireflection (AR) coating on glass that can minimize the reflectance and enhance the performance of CdTe/CdS/SnO₂/glass solar cells. Photocurrent loss resulting from absorption in the CdS film was calculated as a function of CdS thickness. It was found that the current loss from reflectance and absorption is

quite sensitive to the CdS film thickness below 1500 Å. Model calculations also showed that reducing the CdS thickness from 1500 Å to 600 Å can increase the short-circuit current density (J_{sc}) of the cell by 3 mA/cm² because of reduced reflectance and absorption. It was found that the decrease in the CdS thickness below 600 Å increases the reflectance loss but still results in higher J_{sc} , because the current gain resulting from reduced absorption in thin CdS offsets the current loss resulting from higher reflectance. Practical optimum thickness is 600 Å, provided the CdS film can be grown without pin holes at this thickness. Model calculations showed that photocurrent loss from reflectance is not sensitive to SnO₂ thickness above 4000 Å. However, because of the competition between the resistive and absorption losses, SnO₂ thickness in the range of 6000-10000 Å is recommended. Finally, the practical optimum thickness and refractive index for a single layer AR coating on glass was found to be 1100 Å and 1.38, respectively, which provided an additional increase of 0.7 mA/cm² in J_{sc} .

The second phase of this research involved the investigation of defects and loss mechanisms associated with the CdTe layer and the CdTe/CdS interface. Attempts were made to investigate the role of native defects in CdTe on the cell performance. It was shown for the first time that native defect concentration in the polycrystalline CdTe films can be altered by changing the MOCVD growth ambient. For example, Films grown in highly Cd-rich ambient produced n-type CdTe, while the films grown in highly Te-rich

ambient were p-type. This is because Cd vacancies act as acceptors, while the Te vacancies give rise to donors. CdTe cells were fabricated by depositing CdTe films on CdS/SnO₂/glass substrates in different metalorganic chemical vapor deposition (MOCVD) growth ambients with varying Te/Cd mole ratio in the range of 0.02 to 15 in order to alter native defect concentration in the CdTe film, which also had significant effects on the CdTe cell parameters. The short-circuit current (J_{sc}) showed a minimum at the Te/Cd ratio of 0.1. The open-circuit voltage V_{oc} increased monotonically from Cd-rich ambient to Te-rich ambient and then leveled off after Te/Cd ratio of 6. These trends resulted in highest cell efficiency (~12%) on the Te-rich CdTe films. Since V_{oc} is quite sensitive to interface quality, the trend in V_{oc} suggests better interface quality in the Te-rich cells. In order to verify this hypothesis, Auger electron spectroscopy (AES) and carrier transport measurements were performed. AES measurements revealed a high degree of atomic interdiffusion at the CdS/CdTe interface when the CdTe films were grown in the Te-rich conditions. It was found that the current transport in the cells grown in the Cd-rich ambient was controlled by the tunneling/interface recombination mechanism, but the depletion region recombination became dominant in the Te-rich cells. These observations suggest that the enhanced interdiffusion reduces interface states due to stress reduction or gradual transition from CdS to CdTe. The hypothesis of reduced defect density in the CdTe cells grown in the Te-rich conditions was further supported by the high effective

carrier lifetime, measured by time-resolved photoluminescence and the reduced sensitivity of quantum efficiency to forward/light bias.

The third major objective of this research was to investigate the effect of chemical and heat treatments on CdTe films and cells. To accomplish this task, the CdCl₂ concentration and annealing conditions were varied. It was found that CdCl₂ treatment of CdTe films tends to densify the film, changes the surface morphology, makes the grains flat and less faceted, and serves as a flux to recrystallize the CdTe structure. This reduces the effective grain boundary surface area per unit volume (S_{v1}) or decreases the grain boundary conduits for impurity or metal migration, which results in enhanced cell performance. Light I-V and PL measurements revealed optimum CdCl₂ concentration in the range of 50% to 75% for our MOCVD cells, because higher CdCl₂ concentration gives rise to higher Cl-related defect density and degrades the cell performance. Therefore, even though CdCl₂ treatment is essential for high efficiency CdTe cells, it could place an upper limit on the practically achievable cell efficiency. Rapid thermal processing was performed on CdS/CdTe structure to achieve grain regrowth in the CdTe films with lower CdCl₂ concentrations, or even without any CdCl₂ treatment. It was found that RTP conditions produced significant changes in the CdTe cell parameters. A cell with 10.7% efficiency was achieved using the 700°C, 5 second RTP without any CdCl₂ treatment. SEM and EBIC measurements showed that the microstructure and the

diffusion length in the CdTe after the RTP were similar to the CdTe cell with conventional CdCl₂ treatment, which involves 400°C/30min furnace anneal. However, reduced interdiffusion at the CdTe/CdS interface in the RTP cells was probably responsible for the lower RTP cell efficiency compared with the CdCl₂ treated and furnace annealed cells.

The fourth major objective of the research was to achieve a better and reliable contact to CdTe solar cells by improving the fundamental understanding of the effects of Cu on cell efficiency. CdTe solar cells were fabricated by depositing Au/Cu contacts with varying thicknesses and deposition conditions on the polycrystalline CdTe/CdS/SnO₂/glass structures. It was found that Cu plays a dual role on the cell performance; on one hand it helps the formation of better ohmic contact and increases the acceptor doping concentration, but on the other hand, excess Cu diffuses all the way to the CdTe/CdS interface to form recombination centers and shunt paths to degrade the cell performance. Both SIMS and C-V measurements confirmed the incorporation of Cu into the bulk of the CdTe films. Cd out-diffusion toward the surface of the CdTe was also observed during the Au/Cu deposition. It was found that the thickness of Cu plays a critical role in dictating the CdTe solar cell performance because both series and shunt resistances decrease with the increase in Cu thickness. Carrier transport analysis showed that the depletion region recombination dominates the current transport in the CdTe solar

cells with Au/Cu contact, regardless of the amount of Cu incorporation in the bulk and near the CdTe/CdS interface. SIMS measurement showed that higher Au/Cu deposition rates resulted in a greater pile-up of Cd near the CdTe surface, generating more Cd vacant sites below the surface and causing a reduction in the cell performance.

The final phase of the research involved the investigation of the effect of crystallinity and grain boundaries on Cu incorporation in the CdTe films, including the fabrication of CdTe solar cells with larger CdTe grain size. Three different CdTe structures, CdTe/CdS/SnO₂/glass, CdTe/CdS/GaAs, and CdTe/GaAs, were prepared to achieve CdTe films with different degrees of crystallinity and grain size. The CdTe/CdS/GaAs structure gave large CdTe grains (~10 μm) which was used to fabricate a large grain polycrystalline CdTe thin film solar cell structure for the first time in this study by a combination of selective etching of the GaAs substrate and the film transfer onto a glass substrate. X-ray diffraction measurements on the CdTe films, before and after the transfer, were used to assess lattice mismatch-induced changes in the CdTe lattice constant near the CdTe/GaAs interface. SIMS measurement showed that poor crystallinity and smaller grain size (~2 μm) of the CdTe film in the conventional polycrystalline CdTe/CdS/SnO₂/glass structure promotes Cu diffusion from the contact and decreases cell performance. In the large grain (~10 μm) CdTe film, Cu concentration was about a factor of 2 lower than the small grain CdTe film, while in the single crystal CdTe

film, Cu was virtually undetectable. Therefore, we concluded that grain boundaries are the main conduits for Cu migration, and larger CdTe grain size or an alternate method of contact formation needs to be developed to mitigate the adverse effect of Cu and improve the CdTe cell performance.

Through a combination of fundamental understanding of the loss mechanisms associated with different layers and interfaces in the cell structure and process optimization, we were able to increase the CdTe cell efficiency systematically (Figure 9.1). Solar cells fabricated without any material and process optimization gave an efficiency of less than 2%. After the optimized CdCl_2 treatment and 400°C furnace anneal, which reduces grain boundary area per unit volume and makes CdTe more p-type, the cell efficiency went up to 6.6%. Solar cell efficiency increased to 9.3% when the CdTe film was grown under the Te-rich MOCVD growth ambient, which reduced the defect density in the CdTe and at the CdTe/CdS interface by promoting interdiffusion. Contact optimization resulted in additional increase in cell efficiency. A combination of optimized Au/Cu contact thickness and deposition rate, Te-rich MOCVD growth of CdTe, and optimized CdCl_2 treatment and furnace anneal, resulted in approximately 12% efficient CdTe solar cells with $V_{oc}=781.4$ mV, $J_{sc}=23.26$ mA/cm² and fill factor=0.657 (Figure 9.2). This represents the highest efficiency achieved for the MOCVD grown CdTe solar cells to date. In addition to the fundamental understanding of the efficiency

Figure 9.1 The increase in the CdTe cell efficiency by understanding the loss mechanisms in the cell structure in this study.

Figure 9.2 A 11.9% efficient CdTe solar cell was accomplished by the fundamental understanding of loss mechanisms.

limiting defects and loss mechanisms and fabrication of high efficiency CdTe cells, the following guidelines are provided to raise the cell efficiency beyond 12% (Figure 9.3):

- (a) In our cells, CdS thickness was kept to be $\sim 2000 \text{ \AA}$ to obtain pin-hole free CdS. If the CdS thickness of $600 \text{ \AA}$ can be achieved in cell structure without pin-hole problems then, according to Figure 4.1, a 3 mA/cm^2 increase in photocurrent can be obtained due to reduced absorption and reflectance losses. This would increase the J_{sc} value to 26 mA/cm^2 , which corresponds to an increase in cell efficiency from 11.9% to 13.34%.
- (b) If the Cu migration in the CdTe can be reduced, Cu thickness could be increased to reduce R_s without sacrificing R_{sh} , which would improve the fill factor and cell performance. For example, if the R_s value of $4 \text{ } \Omega\text{-cm}^2$ for a $100 \text{ \AA}$ thick Cu contact can be reduce to $1 \text{ } \Omega\text{-cm}^2$, the reduction in I^2R power loss [1] can increase the fill factor from 0.657 to 0.756. The fill factor, in conjunction with $V_{oc}=781.4 \text{ mV}$ and $J_{sc}=26 \text{ mA/cm}^2$, would give cell efficiency of 15.37%.
- (c) Chapters V and VI showed that even though the CdCl_2 treated Te-rich CdTe cells gave the lowest defect density, carrier transport was still dominated by depletion region recombination. The recombination centers in the depletion region are probably due to the Cl-related defects from CdCl_2 treatment. If the recombination centers in the bulk can be eliminated by using other chemicals to enhance the

Figure 9.3 Future guidelines to raise the cell efficiency beyond 12%.

grain structure, over 900 mV open-circuit voltage can be attained for a 1.44 eV bandgap CdTe material [2,3]. The combination of $V_{oc}=900$ mV, $J_{sc}=26$ mA/cm², and fill factor of 0.756, would then produce a 17.7% efficient CdTe solar cell.

- (d) Due to the excellent lattice match between CdTe and InSb (lattice constant of 6.481Å and 6.46Å respectively), CdTe grown on an InSb substrate is expected to have the best film quality. After a high quality CdTe growth on InSb substrate, CdS can be grown on top of the CdTe to form a p-n junction. An ITO layer can then be deposited on the CdS film to form the top contact. InSb would also serve as a back contact to CdTe because of its narrow bandgap (0.18 eV). Therefore an ITO/CdS/CdTe/InSb structure is expected to give better cell performance because of higher CdTe quality and the absence of Cu in the contact material.

APPENDIX

PUBLICATIONS

1. A. Rohatgi, S.A. Ringel, R. Sudharsanan, and H.C. Chou, "An Improved Understanding of Efficiency Limiting Defects in Polycrystalline CdTe/CdS Solar Cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, 1991, pp. 962-966.
2. A. Rohatgi, "An Study of Efficiency Limiting Defects in Polycrystalline CdTe/CdS Solar Cells," *International J. of Solar Energy*, vol. 12, pp. 37-49, 1992.
3. A. Rohatgi and R. Sudharsanan, "MOCVD of Compound Semiconductors for Photovoltaics," in *Proc. 6th international Photovolt. Science and Engineering Conf.*, New Delhi, india., 1992, pp. 835-842.
4. A. Rohatgi, H.C. Chou, A. Bhat, and R. Sudharsanan, "An Improved Understanding of Efficiency Limiting Defects in Polycrystalline CdTe/CdS Solar Cells," in *AIP Conf. Proc. 268: Photovoltaic Advanced Research and Development Project*, AIP, New York, 1992, pp. 243-248.
5. H.C. Chou, A.K. Bhat, S. Kamra, A. Rohatgi, R.R. Arya, L. Russel, and R.K. Ahrenkiel, "The Effects of Cd/Te Mole Ratio in the MOCVD Growth Ambient on CdTe Solar Cells," in *Proc. 23rd IEEE Photovolt. Spec. Conf.*, 1993, pp.481-485. (Poster Award)
6. A. Rohatgi, H.C. Chou, S. Kamra, and A. Bhat, "Investigation of Efficiency Limiting Defects and Rapid Thermal Processing of MOCVD Grown CdTe Solar Cells," in *AIP Conf. Proc. 306: 12th NREL Photovoltaic program review*, AIP, New York, 1993, pp. 354-363.
7. H.C. Chou and A. Rohatgi, "The Impact of MOCVD Growth Ambient on Carrier Transport, Defects, and Performance of CdTe/CdS Heterojunction Solar Cells," *J. Electron. Mater.* vol. 23, pp. 31-37, 1994.
8. H.C. Chou, A. Rohatgi, S. Kamra, and A.K. Bhat, "An Investigation of Photocurrent Loss due to Reflectance and Absorption in CdTe/CdS Heterojunction

- Solar Cells," *J. Electron. Mater.* vol. 23, pp. 681-686, 1994.
9. H.C. Chou, A. Rohatgi, N.M. Jokerst, S. Kamra, S.R. Stock, S.L. Lowrie, R.K. Ahrenkiel, and D.H. Levi, "Approach Toward High Efficiency CdTe/CdS Heterojunction Solar Cells," in *Proc. International Conf. on Electron. Mater.*, vol.3, Material Research Society, Taiwan, 1994, pp. 263-268.
 10. H.C. Chou, A. Rohatgi, E.W. Thomas, S. Kamra and A.K. Bhat, "Effects of Cu on CdTe/CdS Heterojunction Solar Cells with Au/Cu Contact," *J. Electrochem. Soc.*, vol. 142, pp. 254-259, 1995.
 11. A. Rohatgi, H.C. Chou, N.M. Jokerst, E.W. Thomas, C. Ferekides, S. Kamra, Z.C. Feng, and K.M. Dugan, "Effects of CdTe Growth Conditions and Techniques on the Efficiency Limiting Defects and Mechanisms in CdTe Solar Cells," to be published in *AIP Conf. Proc.*, 13th NREL Photovoltaic program review, AIP, New York, 1995.
 12. H.C. Chou, A. Rohatgi, N.M. Jokerst, S. Kamra, S.R. Stock, S.L. Lowrie, R.K. Ahrenkiel, and D.H. Levi, "Approach Toward High Efficiency CdTe/CdS Heterojunction Solar Cells," accepted for publication in *J. Mater. Chemistry Phys.*, 1995.
 13. Z.C. Feng, G.K. Lim, H.C. Chou, A.T.S. Wee, A. Rohatgi, and K.L. Tan, "Correlations Between the MOCVD-grown CdTe/CdS/SnO₂/glass Solar Cell Efficiencies and the Interface/Surface Properties," accepted for publication in *J. Appl. Phys.*
 14. H.C. Chou, A. Rohatgi, N.M. Jokerst, E.W. Thomas, and S. Kamra, "Copper Migration in CdTe Solar Cells," submitted to *IEEE Trans. Electron Dev.* for publication.
 15. Z.C. Feng, G.K. Lim, H.C. Chou, A.T.S. Wee, A. Rohatgi, K.L. Tan, and S. Perkowitz, "A Multi-Technique Study of Effects of CdCl₂ Treatments and Annealing on CdS/SnO₂/glass Heterostructures for Solar Cells," to be submitted to *J. Appl. Phys* for publication.

REFERENCES

Chapter I

1. K. Zweibel, H.S. Ullal, R.L. Mitchel, "The DOE/SERI polycrystalline thin film subcontract program," in *Proc. 20th IEEE Photovolt. Spec. Conf.*, pp. 1469-1476, 1988.
2. N.G. Dhere, "Present status of the development of thin-film solar cells," *Vacuum*, vol. 39, pp. 743-748, 1989.
3. C. Ferekides, J. Britt, Y. Ma and L. Killian, "High efficiency CdTe solar cells by close spaced sublimation," in *Proc. 23rd IEEE Photovolt. Spec. Conf.*, pp. 389-393, 1993.
4. J. R. Sites, "Role of Polycrystallinity in CdTe and CdInSe₂ Photovoltaic Cells," Colorado State Univ. Annual Report to NREL, 1992.
5. R. Frerichs, "The Photo-conductivity of 'incomplete phosphors'," *Phys. Rev.*, vol. 72, pp. 594-601, 1947.
6. R.H. Bube, "Cadmium telluride solar cells," in *Proc. Symp. Mater. and New Proc. Technol. for Photovolt.*, vol. 83, pp. 359-376, 1983.
7. P. Rappaport, "The photovoltaic effect and its utilization," *RCA Review*, vol. 20, pp. 373-397, 1959.
8. A.L. Fahrenbruch, Fundamental of Solar Cells, Academic Press, New York, 1983.
9. C.M. Wolfe, Physical Properties of Semiconductors, Prentice-Hall, New Jersey, 1989.
10. T.L. Chu, S.S. Chu, C. Ferekides, J. Britt and C.Q. Wu, "Thin-film junctions of cadmium telluride by metalorganic chemical vapor deposition," *J. Appl. Phys.*, vol. 71, pp. 3870-3876, 1992.
11. D. Rajavel, "Molecular beam epitaxial and chemical beam epitaxial growth and doping of (001) CdTe," Ph.D. Thesis, Georgia Institute of Technology, 1991.

12. R.H. Bube, "CdTe junction phenomena," *Solar Cells*, vol. 23, pp. 1-17, 1988.
13. T.L. Chu, "Thin film cadmium telluride solar cells by two chemical vapor deposition techniques," *Solar Cells*, vol. 23, pp. 31-48, 1988.
14. R.H. Bube, A.L. Fahrenbruch, R. Sinclair, T.C. Anthony, C. Fortmann, W. Huber, C.T. Lee, T. Thorpe and T. Yamashita, "Cadmium telluride films and solar cells," *IEEE Trans. Electron. Dev.*, vol. ED-31, pp. 528-538, 1984.
15. Y.S. Tyan, "Topics on thin film CdS/CdTe solar cells," *Solar Cells*, vol. 23, pp. 19-29, 1988.
16. P. Sharps, A.L. Fahrenbruch, A. Lopez-Otero and R.H. Bube, "Ion-assisted doping of p-CdTe films," *J. Appl. Phys.*, vol. 68, pp. 6406-6414, 1990.
17. T.L. Chu and S.S. Chu, "Recent progress in thin-film cadmium telluride solar cells," *Process in Photovoltaics: Research and Applications*, vol. 1, pp.31-42, 1993.
18. M. Barbe, F. Bailly, D. Lincot and G. Cohen-Solal, "13% conversion efficiency in cadmium telluride shallow homojunction solar cell. effects of temperature and intensity," in *Proc. 16th IEEE Photovolt. Spec. Conf.*, pp. 1133-1137, 1982.
19. B.M. Basol, "Thin film CdTe solar cells-a review," in *Proc. 21st IEEE Photovolt. Spec. Conf.*, pp. 588-594, 1990.
20. T. Nakazawa, K. Takamizawa and K. Ito, "High efficiency indium oxide/cadmium telluride solar cells," *Appl. Phys. Lett.*, vol. 50, pp. 279-280, 1986.
21. K. W. Mitchell, C. Eberspacher, F. Cohen, J. Avery, "Progress towards high efficiency, thin film CdTe solar cells," in *Proc. 18th IEEE Photovolt. Spec. Conf.*, pp. 1359-1364, 1985.
22. J.A. Aranovich, D. Golmayo, A.L. Fahrenbruch and R.H. Bube, "Photovoltaic properties of ZnO/CdTe heterojunctions prepared by spray pyrolysis," *J. Appl. Phys.*, vol. 51, pp. 4260-4268, 1980.
23. T.L. Chu, S.S. Chu, G. Chen, C. Ferekides, J. Britt and C.Q. Wu, "Zinc selenide film and heterojunctions," *J. Appl. Phys.*, vol. 71, pp. 3865-3869, 1992.

24. T.L. Chu, S.S. Chu, C. Ferekides, J. Britt and C.Q. Wu and C. Wang, "13.4% efficient thin-film CdS/CdTe solar cells," *J. Appl. Phys.*, vol. 70, pp. 7608-7612, 1991.
25. N. Romeo, A. Bosio and V. Canevari, "Large crystalline grain CdTe thin films for photovoltaic application," *International J. Solar Energy*, vol. 12, pp. 183-186, 1992.
26. P.V. Meyers, "Advances in CdTe n-i-p photovoltaics," *Solar Cells*, vol. 27, pp. 91-98, 1989.
27. J.M. Woodcock, A.K. Turner, M.E. Ozsan, and J.G. Summers, "Thin film solar cells based on electrodeposited CdTe," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 842-847, 1991.
28. Y.S. Seol and H.B. Im, "Photovoltaic properties of sintered $\text{Cd}_{1-x}\text{Zn}_x\text{S}/\text{CdTe}$ solar cells," in *Proc. 9th E.C. Photovolt. Solar Energy Conf.*, pp.294-297, 1989.
29. N. Suyama, T. Arita, Y. Nishiyama, N. Ueno, S. Kitamura, and M. Murozono, "CdS/CdTe solar cells by the screen-printing-sintering technique," in *Proc. 21st IEEE Photovolt. Spec. Conf.*, pp.498-503, 1990.
30. T. Arita, A. Hanafusa, S. Kitamura, T. Takakura, and M. Murozono, "Large area CdS/CdTe solar cells," in *Proc. 21st IEEE Photovolt. Spec. Conf.*, pp. 946-951, 1990.
31. J.F. Jordan and S.P. Albright, "Large area photovoltaic cells," *Solar Cells*, vol 23, pp. 107-113, 1988.
32. S.P. Albright, B. Acketman, and J.F. Jordan, "Efficient CdTe/CdS solar cells and modules by spray processing," *IEEE Trans. Electron Dev.*, vol. ED-37, pp. 434-437, 1990.
33. C. Ferekides, "Thin films and solar cells of cadmium telluride and cadmium zinc telluride," Ph.D. Thesis, University of South Florida, 1991.
34. H.C. Chou and A. Rohatgi, "The impact of MOCVD growth ambient on carrier transport, defects, and performance of CdTe/CdS heterojunction solar cells," *J. Electron. Mater.* vol. 23, pp. 31-37, 1994.

Chapter II

1. A.L. Fahrenbruch and R.H. Bube, Fundamentals of Solar Cells, New York: Academic Press, 1983.
2. S.J. Fonash, Solar Cell Device Physics, New York: Academic Press, 1981.
3. M.A. Green, Solar Cells: Operating Principles, Technology, and System Applications, Englewood Cliffs, NJ: Prentice-Hall, 1982.
4. A.L. Fahrenbruch and R.H. Bube, "Heat treatment effects in Cu_2S -CdS heterojunction photovoltaic cells," *J. Appl. Phys.*, vol. 45, pp. 1264-1275, 1974.
5. R.R. Potter, C. Eberspacher and L.B. Fabick, "Device analysis of $\text{CuInSe}_2/(\text{Cd,Zn})\text{S}/\text{ZnO}$ solar cells," in *Proc. 18th IEEE Photovolt. Spec. Conf.*, pp. 1659-1664, 1985.
6. M. Eron and A. Rothwarf, "Interface charging and solar-cell characteristics: $\text{CuInSe}_2/\text{CdS}$," *J. Appl. Phys.*, vol. 57, pp. 2275-2279, 1985.
7. S.M. Sze, Physics of Semiconductor Devices, New York: Wiley and Sons, 1981.
8. A.G. Milnes and D.L. Feucht, Heterojunctions and Metal-Semiconductor Junctions, New York: Academic Press, 1972.
9. R.L. Anderson, "Experiments on Ge-GaAs heterojunctions," *Solid-State Electron.*, vol. 5, pp. 341-351, 1962.
10. W. Shockley and W.T. Read, Jr., "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835-842, 1952.
11. C.T. Sah, R. Noyce and W. Shockley, "Carrier generation and recombination in p-n junctions and p-n junction characteristics," *Proc. IRE*, vol. 45, pp. 1228-1243, 1957.
12. M. Roy, S. Damaskinos, and J.E. Phillips, "The diode current mechanism in $\text{CuInSe}_2/(\text{CdZn})\text{S}$ Heterojunctions," in *Proc. 19th IEEE Photovolt. Spec. Conf.*, pp. 1618-1623, 1988.

13. A. Rothwarf, "A p-i-n model for the thin film $\text{CuInSe}_2/\text{CdS}$ solar cell," *IEEE Trans. Electron Dev.*, vol. ED-29, pp. 1513-1515, 1982.
14. S.J. Fonash, "General formulation of the current-voltage characteristic of a p-n heterojunction solar cell," *J. Appl. Phys.*, vol. 51, pp. 2115-2118, 1980.
15. K.W. Mitchell, A.L. Fahrenbruch and R.H. Bube, "Evaluation of the CdS/CdTe heterojunction solar cell," *J. Appl. Phys.*, vol. 48, pp. 4365-4371, 1977.
16. B.G. Streetman, Solid State Electronic Devices, Englewood Cliffs, NJ: Prentice-Hall, 1980.
17. A.R. Riben and D.L. Feucht, "n Ge - p GaAs heterojunctions," *Solid-State Electron.*, vol. 9, pp. 1055-1065, 1966.
18. A.R. Riben and D.L. Feucht, "Electrical transport in n Ge - p GaAs heterojunctions," *Int. J. Electron.*, vol. 20, pp. 583-599, 1966.
19. W.A. Miller and L.C. Olsen, "Current transport in Boeing $(\text{Cd,Zn})\text{S}/\text{CuInSe}_2$ solar cells," *IEEE Trans. Electron. Dev.*, vol. ED-31, pp. 654-661, 1984.
20. J.B. Yoo, A.L. Fahrenbruch and R.H. Bube, "Transport mechanisms in $\text{ZnO}/\text{CdS}/\text{CuInSe}_2$ solar cells," *J. Appl. Phys.* vol. 68, pp. 4694-4699, 1990.
21. J. R. Sites, "Role of Polycrystallinity in CdTe and CdInSe_2 Photovoltaic Cells," Colorado State Univ. Annual Report to NREL, 1992.
22. P.V. Meyers, "Advances in CdTe n-i-p photovoltaics," *Solar Cells*, vol. 27, pp. 91-98, 1989.
23. A.L. Fahrenbruch, V. Vasilchenko, F. Buch, K. Mitchell, R.H. Bube, "II-VI photovoltaic heterojunctions for solar energy conversion," *Appl. Phys. Lett.*, vol. 25, pp. 605-608, 1974.
24. K. Yamaguchi, N. Nakayama, H. Matsumoto and S. Ikegami, " $\text{CdS}-\text{CdTe}$ solar cell prepared by vapor phase epitaxy," *Japan. J. Appl. Phys.*, vol. 16, pp. 1203-1211, 1977.
25. K. Zanio, Semiconductor and Semimetals: vol. 13 CdTe , New York: Academic

Press, 1978.

26. C. Ferekides, "Thin films and solar cells of cadmium telluride and cadmium zinc telluride," Ph.D. Thesis, University of South Florida, 1991.
27. G. Mandel, "Self-compensation limited conductivity in binary semiconductors. I. theory," *Phys. Rev.*, vol. 134, pp. A1073-A1079, 1964.
28. J.Y.W. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, pp. 5247-5254, 1975.
29. R.H. Bube and K.W. Mitchell, "Research opportunities in polycrystalline compound solar cells," *J. Electron. Mater.*, vol. 22, pp. 17-25, 1993.
30. I. Clemminck, M. Burgelman, M. Casteleyn, J. De Poorter and A. Vervaeke, "Interdiffusion of CdS and CdTe in screen printed and sintered CdS-CdTe solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 1114-1119, 1991.
31. J. Skarp, Y. Koskinen, S. Lindfors, A. Rautiainen and T. Suntola, "Development and evaluation of CdS/CdTe thin film PV cells," in *10th E.C. Photovolt. Solar Energy Conf.*, pp. 567-569, 1991.
32. K.W. Mitchell, A.L. Fahrenbruch and R.H. Bube, "Evaluation of the CdS/CdTe heterojunction solar cell," *J. Appl. Phys.*, vol. 48, pp. 4365-4371, 1977.
33. T.L. Chu, S.S. Chu, C. Wang, C. Ferekides, J. Britt, C.Q. Wu and H.S. Ullal, "14.6% Efficient thin film cadmium telluride heterojunction solar cells," *IEEE Electron. Dev. Lett.*, vol. 13, pp. 303-304, 1992.
34. M. Eron and A. Rothwarf, "Effects of a voltage-dependent light-generated current on solar cell measurements: CuInSe₂/Cd(Zn)S," *Appl. Phys. Lett.*, vol. 44, pp. 131-133, 1984.
35. K. Ohata, J. Saraie, and T. Tanaka, "Optical energy gap of the mixed crystal CdS_xTe_{1-x}," *Japan. J. Appl. Phys.* vol. 12, pp. 1641-1642, 1973.
36. A. Rohatgi, R. Sudharsanan, S.A. Ringel and M.H. MacDougall, "Growth and process optimization of CdTe and CdZnTe polycrystalline films for high efficiency solar cells," *Solar Cells*, vol. 30, pp. 109-122, 1991.

37. I.J. Ferrer and P. Salvador, "Photoluminescence and electroluminescence mechanisms at polycrystalline CdS in air and in contact with aqueous electrolytes," *J. Appl. Phys.*, vol. 66, pp.2568-2577, 1989.
38. T.L. chu, S.S. Chu, S.T. Ang, "Electrical properties of CdS/CdTe heterojunctions," *J. Appl. Phys.*, vol. 64, pp. 1233-1237, 1988.
39. A. Rohatgi, S.A. Ringel, R. Sudharsanan and H.C. Chou, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 962-966, 1991.
40. T. Arita, A. Hanafusa, N. Ueno, Y. Nishiyama, S. Kitamura, "CdS/CdTe solar cells with improved CdS films fabricated by the writing method," *Solar Energy Materials*, vol. 23, pp. 371-379, 1991.
41. P.O. Vaccaro, G. Meyer, and J. Saura, "Effects of CdCl₂ on the growth of CdTe on CdS films for solar cells by isothermal close-spaced vapor transport," *J. Phys. D.: Appl. Phys.*, vol. 24, pp. 1886-1889, 1991.
42. J.T. Moon, K.C. Park and H.B. Im, "Photovoltaic properties of CdS/CdTe solar cells sintered with CdCl₂," *Solar Energy Materials*, vol. 18, pp. 53-60, 1988.
43. N. Romeo, A. Bosio, and V. Canevari, "Crystallization of CdTe thin films by CdCl₂ treatment at high temperature," in *12th E.C. Photovolt. Solar Energy Conf.*, pp. 662-663, 1994.
44. S.A. Ringel, A.W. Smith, M.H. MacDougal and A. Rohatgi, "The effects of CdCl₂ on the electronic properties of molecular-beam-epitaxially grown CdTe/CdS heterojunction solar cells," *J. Appl. Phys.*, vol. 70, pp. 881-889, 1991.
45. D.K. Schroder and D.L. Meier, "Solar cell contact resistance-a review," *IEEE Trans. Electron Dev.*, vol. ED-31, pp. 637-653, 1984.
46. A.L. Fahrenbruch, "Ohmic Contacts and Doping of CdTe," *Solar Cells*, vol. 21, pp. 399-412, 1987.
47. B.L. Crowder and W.N. Hammer, "Shallow acceptor states in ZnTe and CdTe," *Phys. Rev.*, vol. 150, pp. 541-545, 1966.

- 48. A.Y.C. Yu, "Electron tunneling and contact resistance of metal-silicon contact barriers," *Solid-State Electron.*, vol. 13, pp. 239-247, 1970.
- 49. J.P. Ponpon, "A review of ohmic and rectifying contacts on cadmium telluride," *Solid-State Electron.*, vol. 28, pp. 689-706, 1985.
- 50. T. C. Anthony, A. L. Fahrenbruch, and R. H. Bube, "Low resistance contact to p-type cadmium telluride," *J. Electron. Mater.*, vol. 11, pp. 89-109, 1982.
- 51. K. Kuribayashi, H. Matsumoto, H. Uda, Y. Komatsu, A. Nakano, and S. Ikegami, "Preparation of low resistance contact electrode in screen printed CdS/CdTe solar cell," *Japan. J. Appl. Phys.* vol. 22, pp. 1828-1831, 1983.
- 52. T. Yoshida, "Analysis of photocurrent in screen-printed CdS/CdTe solar cells," *J. Electrochem. Soc.*, vol. 139, pp. 2353-2357, 1992.

Chapter III

1. N.R. Pavaskar, C.A. Menezes, and A.P.B. Sinha, "Photoconductive films by a chemical bath deposition process," *J. Electrochem. Soc.*, vol. 124, pp. 743-748, 1977.
2. I. Kaur, D.K. Pandya, and K.L. Chopra, "Growth kinetics and polymorphism of chemically deposited CdS films," *J. Electrochem. Soc.*, vol. 127, pp. 943-948, 1980.
3. W.J. Danaher, L.E. Lyons, and G.C. Morris, "Some properties of thin films of chemically deposited CdS films," *Solar Energy Materials*, vol. 12, pp. 137-148, 1985.
4. S.M. Sze, *VLSI Technology*, New York: McGraw-Hill, 1983.
5. K.K. Schuegraf, Handbook of Thin-film Deposition Processes and Techniques: Principles, Methods, Equipment, and Applications, Park Ridge, NJ: Noyes, 1988.
6. I.J. Ferrer and P. Salvador, "Photoluminescence and electroluminescence mechanisms at polycrystalline CdS in air and in contact with aqueous electrolytes," *J. Appl. Phys.*, vol. 66, pp.2568-2577, 1989.
7. S.A. Ringel, A.W. Smith, M.H. MacDougall and A. Rohatgi, "The effects of CdCl₂ on the electronic properties of molecular-beam-epitaxially grown CdTe/CdS heterojunction solar cells," *J. Appl. Phys.*, vol. 70, pp. 881-889, 1991.
8. B.E. McCandless and R.W. Birkmire, "Analysis of post deposition processing for CdTe/CdS thin film solar cell," *Solar Cells*, vol. 31, pp. 527-535, 1991.
9. D.J. O'Connor, B.A. Sexton, and R.St.C. Smart, Surface Analysis Methods in Materials Science, Berlin: Springer-Verlag, 1992.
10. M.A. Hayat, Principles and Techniques of Scanning Electron Microscopy, New York: van Nostrand Reinhold, 1974.
11. D. Brigg and M.P. Seah, Practical Surface Analysis, New York: Wiley and Sons, 1990.

12. M. Prutton, Surface Physics, Oxford: Clarendon Press, 1975.
13. Joseph I. Goldstein, Scanning Electron Microscopy and X-ray Microanalysis, New York: Plenum Press, 1981.
14. John C. Vickerman, Secondary Ion Mass Spectrometry Principles and Applications, Oxford: Clarendon Press, 1989.
15. R.G. Wilson, Secondary Ion Mass Spectrometry, New York: John Wiley & Sons, 1989.
16. L.E. Davis, N.C. MacDonald, P.W. Palmberg, G.E. Riach, R.E. Weber, Handbook of Auger Electron Spectroscopy, Eden Prairie: Physical Electronics Inc.
17. P.H. Dawson, Quadrupole Mass Spectrometry and Its Application, Amsterdam: Elsevier, 1976.
18. B.D. Cullity, Elements of X-ray Diffraction, Reading, MA: Addison-Wesley, 1956.
19. J.V. Smith, Powder Diffraction File, Philadelphia: American Soc. for Testing and Material, 1991.
20. M.A. Green, Solar Cells: Operating Principles, Technology, and System Applications, Englewood Cliffs, NJ: Prentice-Hall, 1982.
21. D.G. Goebel, "Generalized integrating-sphere theory," *Applied Optics*, vol. 6, pp. 125-128, 1967.

Chapter IV

1. R.H. Bube and K.W. Mitchell, "Research opportunities in polycrystalline compound solar cells," *J. Electron. Mater.*, vol. 22, pp. 17-25, 1993.
2. P.V. Meyers, "Advances in CdTe n-i-p photovoltaics," *Solar Cells*, vol. 27, pp. 91-98, 1989.
3. A. Rohatgi, S.A. Ringel, R. Sudharsanan and H.C. Chou, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 962-966, 1991.
4. T.L. Chu, S.S. Chu, C. Wang, C. Ferekides, J. Britt, C.Q. Wu and H.S. Ullal, "14.6% Efficient thin film cadmium telluride heterojunction solar cells," *IEEE Electro. Dev. Lett.*, vol. 13, pp. 303-304, 1992.
5. A. K. Bhat, "Thin film preparation using pulsed laser deposition," Ph.D. Thesis, University of Toledo, pp. 61, 1991.
6. M. A. Green, *Solar Cells*, Englewood Cliffs, NJ: Prentice-Hall, 1982, pp. 162.
7. A. Thelen, "Beitrage zur theorie der reflexverminderung mit mehrfachschichten," *Optik*, vol. 13, pp. 537-542, 1956.
8. O.S. Heavens, *Optical Properties of Thin Solid Films*, London: Butterworths, 1955.
9. B.H. Billings, Ed., *American Institute of Physics Handbook*, 2nd ed. New York: McGraw-Hill, 1963, pp. 9-50.
10. SD Series Ellipsometers User Manual, Thin Film Measurement Systems, Munich, Germany: PLASMOS GmbH, 1990.
11. T. Arita, A. Hanafusa, N. Ueno, Y. Nishiyama, S. Kitamura, "CdS/CdTe solar cells with improved CdS films fabricated by the wetting method," *Solar Energy Materials*, vol. 23, pp. 371-379, 1991.
12. C. Ferekides, J. Britt, Y. Ma and L. Killian, "High efficiency CdTe solar cells by close spaced sublimation," in *Proc. 23rd IEEE Photovolt. Spec. Conf.*, pp. 389-393, 1993.

Chapter V

1. P.V. Meyers, "Ametek's CdTe solar module development program," *Solar Cells* vol. 24, pp. 35-42, 1988.
2. R.W. Birkmire, B.E. McCandless, and J.E. Phillips, "Post processing treatments and contacts for thin film CdS/CdTe devices," in *Proc. Polycryst. Thin Film Program Review Meeting*, pp. 77-84, 1989.
3. T.L. Chu, S.S. Chu, S.T. Ang, "Electrical properties of CdS/CdTe heterojunctions," *J. Appl. Phys.*, vol. 64, pp. 1233-1237, 1988.
4. N. Suyama, T. Arita, Y. Nishiyama, N. Ueno, S. Kitamura, and M. Murozono, "CdS/CdTe solar cells by the screen-printing-sintering technique," in *Proc. 21st IEEE Photovolt. Spec. Conf.*, pp.498-503, 1990.
5. J. Skarp, Y. Koskinen, S. Lindfors, A. Rautiainen and T. Suntola, "Development and evaluation of CdS/CdTe thin film PV cells," in *10th E.C. Photovolt. Solar Energy Conf.*, pp. 567-569, 1991.
6. A. Rohatgi, H. C. Chou, A. Bhat, and R. Sudharsanan, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," *AIP Conf. Proc. 268: Photovoltaic Advanced Research and Development Project*, pp. 243-248, 1992.
7. S.A. Ringel, A.W. Smith, M.H. MacDougall and A. Rohatgi, "The effects of CdCl₂ on the electronic properties of molecular-beam-epitaxially grown CdTe/CdS heterojunction solar cells," *J. Appl. Phys.*, vol. 70, pp. 881-889, 1991.
8. J. R. Sites, "Role of polycrystallinity in CdTe and CdInSe₂ photovoltaic cells," Colorado State Univ. Annual Report to NREL, pp.6, 1992.
9. J.L. Pautrat, J.M. Francou, N. Magnea, E. Molva, and K. Saminadayar, "Donors and acceptors in tellurium compounds; the problem of doping and self compensation", *J. Crystal Growth*, vol. 72, pp. 194-204, 1985.
10. T.L. Chu, S.S. Chu, C. Ferekides, J. Britt and C.Q. Wu, "Thin-film Junctions of cadmium telluride by metalorganic chemical vapor deposition", *J. Appl. Phys.* vol. 71, pp. 3870-3876, 1992.

11. T.M. Hsu, R.J. Jih, P.C. Lin, H.Y. Ueng, Y.J. Hsu, and H.L. Hwang, "Oxygen doping in close-spaced-sublimed CdTe thin films for photovoltaic cells", *Appl. Phys. Lett.*, vol. 59, pp. 3607-3609, 1986.
12. T.L. Chu, "Thin film cadmium telluride, zinc telluride, and mercury zinc telluride solar cells", Technical Report to NREL, 1988-1991, pp 28-29.
13. I. Clemminck, M. Burgelman, M. Casteleyn, J. De Poorter and A. Vervaet, "Interdiffusion of CdS and CdTe in screen printed and sintered CdS-CdTe solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 1114-1119, 1991.
14. M. Aven and J. S. Prener, Physics and Chemistry of II-VI Compounds, New York: Wiley, 1967, pp. 254.
15. A. Rohatgi, S.A. Ringel, R. Sudharsanan and H.C. Chou, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 962-966, 1991.
16. R. W. Birkmire, S. S. Hegedus, B. E. McCandless, J. E. Phillips, T. W. F. Russell, W. N. Shafarman, S. Verma, and S. Yamanaka, "Polycrystalline heterojunction solar cells: processing perspective," *AIP Conf. Proc. 268: Photovoltaic Advanced Research and Development Project*, pp. 212-216, 1992.
17. R.R. Potter, C. Eberspacher and L.B. Fabick, "Device analysis of CuInSe₂/(Cd,Zn)S/ZnO solar cells," in *Proc. 18th IEEE Photovolt. Spec. Conf.*, pp.1659-1664, 1985.
18. M. Eron and A. Rothwarf, "Interface charging and solar-cell characteristics: CuInSe₂/CdS," *J. Appl. Phys.*, vol. 57, pp. 2275-2279, 1985.
19. W.A. Miller and L.C. Olsen, "Current transport in Boeing (Cd,Zn)S/CuInSe₂ solar cells," *IEEE Trans. Electron. Dev.*, vol. ED-31, pp. 654-661, 1984.
20. J.B. Yoo, A.L. Fahrenbruch and R.H. Bube, "Transport mechanisms in ZnO/CdS/CuInSe₂ solar cells," *J. Appl. Phys.* vol. 68, pp. 4694-4699, 1990.
21. S. A. Ringel, "Growth and process induced defects and recombination mechanisms in AlGaAs/GaAs and CdZnTe/CdS photovoltaic device structures," Ph.D. Thesis, Georgia Institute of Technology, pp. 38, 1991.

Chapter VI

1. J. R. Sites, Colorado State Univ. Annual Report to NREL: Role of Polycrystallinity in CdTe and CdInSe₂ Photovoltaic Cells, pp. 6, 1992.
2. D.S. Albin, G.D. Mooney, A. Duca. J. Tu "Enhanced grain growth on polycrystalline CuInSe₂ using rapid thermal processing," *Solar Cells*, vol. 30, pp. 47-52, 1991.
3. R. Singh, F. Radpour, S. Anandakugan and P. Chou, "Rapid isothermal processing of bulk and thin film solar cells," in *Proc. 19th IEEE Photovolt. Spec. Conf.*, pp. 1279-1284, 1987.
4. R. Singh, F. Radpour, P. Chou, Q. Nguyen, S.P. Joshi, H.S. Ullal, R.J. Matson and S. Asher, "Junction and ohmic contact formation in compound semiconductors by rapid isothermal processing," *J. Vac. Sci. Technol.*, vol. A5, pp. 1819-1823, 1987.
5. A. Gat, L. Gerzberg and J.F. Gibbons, "CW laser anneal of polycrystalline silicone: crystalline structure, electrical properties," *Appl. Phys. Lett.*, vol. 33, pp. 775-778, 1978.
6. J.F. Gibbons and K.F. Lee, "CW laser recrystallization of (100) Si on amorphous substrates," *Appl. Phys. Lett.*, vol. 34, pp. 831-833, 1979.
7. C.S. Smith and L. Guttman, "Measurement of internal boundaries in three-dimensional structures by random sectioning," *Trans. American Inst. Mining Metallurgical Eng.*, vol. 192, pp. 81-87, 1953.
8. P.O. Vaccaro, G. Meyer, and J. Saura, "Effects of CdCl₂ on the growth of CdTe on CdS films for solar cells by isothermal close-spaced vapor transport," *J. Phys. D.: Appl. Phys.*, vol. 24, pp. 1886-1889, 1991.
9. J.T. Moon, K.C. Park and H.B. Im, "Photovoltaic properties of CdS/CdTe solar cells sintered with CdCl₂," *Solar Energy Materials*, vol. 18, pp. 53-60, 1988.
10. S.A. Ringel, A.W. Smith, M.H. MacDougall and A. Rohatgi, "The effects of CdCl₂ on the electronic properties of molecular-beam-epitaxially grown CdTe/CdS heterojunction solar cells," *J. Appl. Phys.*, vol. 70, pp. 881-889, 1991.

11. R.J. Matson, F.S. Hasoon, K.M. Jones, M.M. Al-Jassim, and R.D. Tomlinson, "Microcharacterization of CdTe films deposited by closed-spaced sublimation," *Progress in Photovoltaic Research and Application*, vol. 2, pp. 203-209, 1994.
12. A. Rohatgi, S.A. Ringel, R. Sudharsanan and H.C. Chou, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 962-966, 1991.
13. R.W. Birkmire, B.E. McCandless, and J.E. Phillips, "Post processing treatments and contacts for thin film CdS/CdTe devices," in *Proc. Polycrystalline Thin Film Program Meet.*, pp. 77-84, Lakewood, Colorado, 1989.
14. S.R. Das, J.G. Cook, N.L. Rowell, and M.S. Aouadi, "Photoluminescence spectroscopy of CdTe epilayers grown by rf magnetron sputtering," *J. Appl. Phys.*, vol. 68, pp. 5796-5803, 1990.
15. H.L. Cotal, A.C. Lewandowski, B.G. Markey, S.W. S. McKeever, E. Cantwell, and J. Alridge, "1.4-eV photoluminescence and thermally stimulated conductivity in cadmium telluride," *J. Appl. Phys.*, vol. 67, pp. 975-982, 1990.
16. N.V. Agrinskaya and O.A. Mateev, "Interaction of defects in CdTe-crystals heavily doped with chlorine," *Revue de Physique Appliquee*, vol. 12, pp. 235-237, 1977.
17. J.M. Figueroa, F. Sanchez-Sinencio, J.G. Mendoza, O. Zelaya, C. Vazquez-Lopez, and J. S. Helman, "Influence of Cd vacancies on the photoluminescence of CdTe," *J. Appl. Phys.*, vol. 60, pp. 452-454 1986.
18. M. Barbe, F. Bailly, D. Lincot and G. Cohen-Solal, "13% conversion efficiency in cadmium telluride shallow homojunction solar cell. effects of temperature and intensity," in *Proc. 16th IEEE Photovolt. Spec. Conf.*, pp. 1133-1137, 1982.
19. B.E. McCandless and R.W. Birkmire, "Analysis of post deposition processing for CdTe/CdS thin film solar cells," *Solar Cells*, vol. 31, pp. 527-535, 1991.

Chapter VII

1. A.L. Fahrenbruch, "Ohmic contacts and doping of CdTe," *Solar Cells*, vol. 21, pp. 399-412, 1987.
2. J.P. Ponpon, "A review of ohmic and rectifying contacts on cadmium telluride," *Solid-State Electron.*, vol. 28, pp. 689-706, 1985.
3. S. K. Das and G. C. Morris, "Influence of growth and microstructure of electrodeposited cadmium telluride films on the properties of n-CdS/p-CdTe thin-film solar cells," *J. Appl. Phys.*, vol.72, pp. 4940-4945, 1992.
4. J. Britt and C. Ferekides, "Thin-film CdS/CdTe solar cell with 15.8% efficiency," *Appl. Phys. Lett.*, vol.62, pp.2851-2852, 1993.
5. J. P. Laurenti, G. Bastide, and M. Rouzeyre, "Localized defects in p-CdTe:Cu doped by copper incorporation during Bridgman growth," *Solid State Commun.*, vol.67, pp.1127-1130, 1988.
6. K. Zanio, Semiconductor and Semimetals: vol. 13 CdTe, Academic Press, New York, 1978.
7. J.W. Park, B.T. Ahn and H.B. Im, "Photovoltaic properties of sintered CdS/CdTe solar cells doped with Cu," *J. Electrochem. Soc.* vol. 139, pp. 3351-3356, 1992.
8. B. E. McCandless and R. W. Birkmire, "Analysis of post deposition processing for CdTe/CdS thin film solar cells," *Solar Cells*, vol. 31, pp. 527-535, 1991.
9. B.V. King and R.P. Webb, "SIMS measurements of ion beam mixing in silver," in *Proceedings of the 8th International Conference on Secondary Ion Mass Spectrometry*, Sep., 1992, pp. 363-366.
10. T. C. Anthony, A. L. Fahrenbruch, and R. H. Bube, "Low resistance contact to p-type cadmium telluride," *J. Electron. Mater.*, vol. 11, pp. 89-109, 1982.
11. K. Kuribayashi, H. Matsumoto, H. Uda, Y. Komatsu, A. Nakano, and S. Ikegami, "Preparation of low resistance contact electrode in screen printed CdS/CdTe solar cell," *Japan. J. Appl. Phys.* vol. 22, pp. 1828-1831, 1983.

12. M. G. Astles and G. Blackmore, "The use of secondary ion mass spectrometry in the study of matrix atom diffusion in epitaxial CdTe," *J. Electron. Mater.*, vol. 15, pp. 287-290, 1986.
13. H. Gnaser and H. Oechsner, "The influence of polarizability on the emission of sputtered molecular ions," *Surface Science Letters*, vol.302, pp.L289-292, 1994.
14. G. Mandel, "Self-compensation limited conductivity in binary semiconductors. I. theory," *Phys. Rev.*, vol. 134, pp. A1073-A1079, 1964.
15. J. A. von Windheim and M. Cocivera, "Variation of resistivity of copper-doped cadmium telluride prepared by electrodeposition," *J. Phys. D: Appl. Phys.*, vol.23, pp.581-586, 1990.
16. A. Rohatgi, S.A. Ringel, R. Sudharsanan and H.C. Chou, "An improved understanding of efficiency limiting defects in polycrystalline CdTe/CdS solar cells," in *Proc. 22nd IEEE Photovolt. Spec. Conf.*, pp. 962-966, 1991.
17. A. Rothwarf, "A p-i-n model for the thin film CuInSe₂/CdS solar cell," *IEEE Trans. Electron Dev.*, vol. ED-29, pp. 1513-1515, 1982.
18. J.B. Yoo, A.L. Fahrenbruch and R.H. Bube, "Transport mechanisms in ZnO/CdS/CuInSe₂ solar cells," *J. Appl. Phys.* vol. 68, pp. 4694-4699, 1990.
19. S. A. Ringel, "Growth and process induced defects and recombination mechanisms in AlGaAs/GaAs and CdZnTe/CdS photovoltaic device structures," Ph.D. Thesis, Georgia Institute of Technology, pp. 38, 1991.

Chapter VIII

1. A.L. Fahrenbruch, "Ohmic contacts and doping of CdTe," *Solar Cells*, vol. 21, pp. 399-412, 1987.
2. J.P. Ponpon, "A review of ohmic and rectifying contacts on cadmium telluride," *Solid-State Electron.*, vol. 28, pp. 689-706, 1985.
3. C.S. Smith and L. Guttman, "Measurement of internal boundaries in three-dimensional structures by random sectioning," *Trans. American Inst. Mining Metallurgical Eng.*, vol. 192, pp. 81-87, 1953.
4. P.W. Leech, and P.J. Gwynn, and M.H. Kibel, "A selective etchant for $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$, CdTe and HgTe on GaAs," *Appl. Surface Sci.*, vol.37, pp. 291-298, 1989.
5. C. Camperi-Ginestet, M. Hargis, N. Jokerst, M. Allen, "Alignable epitaxial liftoff of GaAs materials with selective deposition using polyimide diaphragms," *IEEE Trans. Photonics Technol. Lett.*, vol. 3, pp. 1123-1126, 1991.
6. M.Y. Simmons, H.M. Al-Allak, K. Durose, and A.W. Brinkman, "Epitaxial CdTe-based solar cells," *Int. J. Solar Energy*, vol. 12, pp. 233-245, 1992.
7. G. Patrat, E. Soyz, M. Brunel, J. Cibert, S. Tatarenko, and K. Saminadayar, "Early stage of growth for (001) ZnTe and (111) CdTe on (001)GaAs: a structural study of the interface using conventional and grazing-incidence X-ray diffraction," *Solid State Commun.*, vol. 74, pp. 433-437, 1990.
8. H.C. Chou and A. Rohatgi, "The impact of MOCVD growth ambient on carrier transport, defects, and performance of CdTe/CdS heterojunction solar cells," *J. Electron. Mater.* vol. 23, pp. 31-37, 1994.
9. S.K. Ghandhi, VLSI Fabrication Principles, Wiley, New York, 1994, pp. 816.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE January 1996		3. REPORT TYPE AND DATES COVERED Final Subcontract Report, 1 February 1992 - 30 November 1995	
4. TITLE AND SUBTITLE Development of High-Efficiency, Thin-Film CdTe Solar Cells				5. FUNDING NUMBERS C: XG-2-11036-3 TA: PV631101	
6. AUTHOR(S) A. Rohatgi, H. C. Chou, S. Kamra, A. Bhat					
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Georgia Institute of Technology School of Electrical Engineering Atlanta, Georgia				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393				10. SPONSORING/MONITORING AGENCY REPORT NUMBER TP-451-20688 DE96000516	
11. SUPPLEMENTARY NOTES NREL Technical Monitor: B. von Roedern					
12a. DISTRIBUTION/AVAILABILITY STATEMENT				12b. DISTRIBUTION CODE UC-1263	
13. ABSTRACT (Maximum 200 words) This report describes work performed by the Georgia Institute of Technology (GIT) to bring the polycrystalline CdTe cell efficiency a step closer to the practically achievable efficiency of 18% through fundamental understanding of defects and loss mechanisms, the role of chemical and heat treatments, and investigation of new process techniques. This objective was addressed by a combination of in-depth characterization, modeling, materials growth, device fabrication, and carrier transport analyses of Au/Cu/CdTe/CdS/SnO ₂ /glass front-wall heterojunction solar cells. GIT attempted to understand the loss mechanism(s) in each layer and interface by a step-by-step investigation of this multilayer cell structure. The first step was to understand, quantify, and reduce the reflectance and photocurrent loss in polycrystalline CdTe solar cells. The second step involved the investigation of defects and loss mechanisms associated with the CdTe layer and the CdTe/CdS interface. The third step was to investigate the effect of chemical and heat treatments on CdTe films and cells. The fourth step was to achieve a better and reliable contact to CdTe solar cells by improving the fundamental understanding of the effects of Cu on cell efficiency. Finally, the research involved the investigation of the effect of crystallinity and grain boundaries on Cu incorporation in the CdTe films, including the fabrication of CdTe solar cells with larger CdTe grain size.					
14. SUBJECT TERMS high efficiency ; thin films ; cadmium telluride ; photovoltaics ; solar cells ; polycrystalline ; heterojunctions				15. NUMBER OF PAGES 306	
				16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL		

Chapter IX

1. P.V. Meyers, "Advances in CdTe n-i-p photovoltaics," *Solar Cells*, vol. 27, pp. 91-98, 1989.
2. A.L. Fahrenbruch, V. Vasilchenko, F. Buch, K. Mitchell, R.H. Bube, "II-VI photovoltaic heterojunctions for solar energy conversion," *Appl. Phys. Lett.*, vol. 25, pp. 605-608, 1974.
3. K. Yamaguchi, N. Nakayama, H. Matsumoto and S. Ikegami, "CdS-CdTe solar cell prepared by vapor phase epitaxy," *Japan. J. Appl. Phys.*, vol. 16, pp. 1203-1211, 1977.