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Appendix to the Report from the Low-Residue Soldering Task Force: Phase II Results

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Executive Summary

Background

The LRSTF report for Phase I of its evaluation of low-residue soldering was issued in June 1995. This Appendix summarizes the results of follow-on testing performed in Phase II and compares electrical test results for both phases.

Deliberate decisions were made by the LRSTF in Phase I to challenge the design guideline limits in MIL-STD-275, *Printed Wiring for Electronic Equipment*. The LRSTF considered this approach to produce a "worst case" design and provide useful information about the robustness of LR soldering processes. As such, good design practices were sometimes deliberately violated (see Section 2.4) in designing the LRSTF board. This approach created some anomalies for both LR boards and RMA/cleaned controls (see Sections 4.7 and 4.9). Phase II testing verified that problems that affected both RMA/cleaned and LR boards in Phase I were design related.

Processing

Some of the processing categories used in Phase I (see Figure 3.1) were dropped in Phase II. For example, polyimide substrates were dropped since there was no appreciable difference in the electrical performance of polyimide and FR-4 epoxy substrates in Phase I. FR-4 was selected for Phase II as a "worst case" because it produced higher ionics in Phase I. Similarly, no differences in electrical performance were identified between the cleaned and not cleaned LR boards in Phase I, so Phase II eliminated cleaning of LR boards (all RMA controls were cleaned).

LRSTF boards were processed at two sites in Phase II: LR boards at Texas Instruments and RMA/cleaned boards at the EMPF (rather than at AlliedSignal). Both sites processed 25 boards, five of which were used for process setup and the remaining 20 boards (10 with conformal coating and 10 without) were subjected to environmental testing at Sandia. In Phase I, only five boards were used per process category. TI applied the conformal coating to both the LR and RMA boards.

Test Conditions

Electrical measurements were recorded at pre-test and after one, two, and three weeks of environmental conditioning (ESS). Planned environmental test conditions for Phase II were identical to those for Phase I — three weeks of conditioning at 85° C and 85% relative humidity. However, an automatic controller failed to perform as programmed during ramp down at the end

of the first week of ESS and again at the start of week 2. This failure created extreme temperature and humidity profiles, which resulted in a *more stressful testing environment* than would be experienced under normal testing conditions (see Section A.4).

In spite of these extreme temperature and humidity excursions, Phase II LR and RMA boards performed as good as, or better than, those in Phase I. The only exception was current leakage for the PGA socket for both LR and RMA boards and for the 10-mil pads and gull wing for RMA. These leakages were due to the condensation caused by the malfunction of the test chamber controller (see Section A.10). Electrical test results are now summarized by type of circuitry.

High Current Low Voltage

All HCLV test results were well within the test criterion and slightly lower (better) than in Phase I due to the elimination of common mode noise. RMA controls and LR boards gave similar results.

High Voltage Low Current

HVLC results for RMA and LR were similar and well within the test criterion. The high voltage flashovers observed in Phase I did not occur in Phase II, corroborating the HVLC design modifications.

High Speed Digital

Rise and fall time measurements were made on PTH and SMT HSD circuits at each testing time in Phase II. Unlike Phase I, all measurements for RMA and LR were well below the upper limit of 7 ns. The redesign of the LRSTF board to eliminate parasitic capacitance (see Figure 4.20) is the likely reason for this improvement.

High Frequency Low-Pass Filters

Performance of the HF LPFs for LR was comparable to that for RMA and all measurements were well within the stated test criterion. Two anomalies were attributed to an open circuit on an RMA board and to a component failure on a LR board, neither of which was related to the soldering processes.

High Frequency Transmission Line Coupler

The 50 MHz forward coupling measurements were all less than the test plan criterion of -33 dB and are all slightly lower (better) than the corresponding Phase I measurements. The variability in the Phase II RMA

measurements increased from Phase I, but was similar to the variability of LR in Phase II.

Reverse coupling null measurements were also all less than -33 dB. LR measurements were all slightly lower (better) in Phase II and slightly lower than those for RMA, which are about the same as in Phase I.

Other Circuits

PGA. Prior to the chamber controller failure (see above), 1520 leakage measurements on PGA-A and PGA-B for all of Phase I and Phase II pre-test were all in the "noise level" and far below the upper limit test criterion of 1 μ A. After week 1 of ESS in Phase II (after the failure of the chamber controller), some RMA and LR leakage measurements were erratic, inconsistent, and well above the 1 μ A criterion. At the end of week 3 of ESS, two RMA boards and four LR boards exhibited excessive leakage measurements.

The 1520 consecutive leakage measurements mentioned above were on boards that did not experience condensation or applied bias. The heavy condensation on the PWBs due to the controller failure (see Section A.4), in conjunction with the applied bias, likely created leakage paths through the formation of dendritic filaments. Thus, the six boards with high leakage were sent to Texas Instruments for further examination to determine the source of the leakage.

The TI investigation determined that the electrical leakage at the PGA test patterns was likely due to electrochemical migration (ECM) of the constituent metals on the PWB. ECM requires surface moisture (such as was created when the test chamber controller failed to operate properly), absorbed or condensed, and the application of an electrical (DC) bias.

Gull Wing. A nonfunctional gull wing device was planned to be soldered to the LRSTF board in Phase I. As explained in Section A.2, the GW device was not used due to a mismatch between the actual spacing of the GW device (25.6 mils) and the lands on the PWB (25 mils). The board layout was modified in Phase II to allow the GW device to be soldered and total leakage measurements were made on adjacent lands.

At the end of week 2 of ESS, three RMA boards and one LR board exceeded the test criterion. At the conclusion of ESS, the LR board returned to a normal reading while three RMA boards remained considerably above the test criterion. Of these three RMA boards, two were repeats from week 2 and one was on a new board. These leakages are also likely due to the formation of dendritic filaments.

10-Mil Pads. The 10-mil pads were laid out in two rows of five pads each and the pads within each row were connected on the bottom layer of the board. The 720 leakage measurements for Phase I were previously shown in boxplots in Figure 4.31. These measurements were all in the "noise level" and well below the test plan upper limit of 1 μ A. Figure A.22 shows all Phase II leakage measurements within the test criterion at pre-test and the end of week 1 of ESS. One LR board had a leakage current equal to the test criterion at the end of week 2. At the conclusion of ESS, this LR board had a reading near zero, while two RMA boards exceeded the test criterion. In addition, one other RMA board produced an unstable reading. These leakages are also likely due to the formation of dendritic filaments as previously discussed.

Stranded Wires. Two 22-gauge stranded wires were hand soldered as previously shown in Figure 2.20. Stranded wire 1 was soldered directly into plated through holes and stranded wire 2 was soldered to two terminals. Voltage measurements for stranded wires 1 and 2 were quite similar for both RMA and LR processing and the week-to-week changes were well within the 35 mV test criterion.

Summary of Phase II Test Results

Phase II testing verified that problems that affected both RMA and LR boards in Phase I were design, not process, related. These problems arose as the result of deliberate decisions by the LRSTF to challenge MIL-STD-275 design guidelines in order to evaluate the robustness of LR processing. Not only were guidelines challenged, but in some cases good design practices were deliberately violated (see Section 2.4). In normal manufacturing environments, good design practices would not be challenged and problems such as were encountered in Phase I would be discovered and corrected prior to actual production runs. However, the short time schedule for Phase I did not allow for these normal procedures.

Phase II testing was successful in verifying that problems that affected both RMA and LR boards in Phase I were design related. Overall, Phase II performance was as good as or better than that observed in Phase I. The only problem area encountered in Phase II was due to formation of dendritic filaments resulting from applied bias and heavy condensation (formed when the test chamber controller malfunctioned). The dendrites caused high current leakages at the PGA socket, gull wing, and 10-mil pads on RMA/cleaned boards and at the PGA socket on LR boards.

Appendix: Phase II Results

(Evaluation of Low-Residue Soldering for Military and Commercial Applications: A Report from the Low-Residue Soldering Task Force)

A.1 Background

The LRSTF made deliberate decisions to challenge the design guideline limits in MIL-STD-275, *Printed Wiring for Electronic Equipment*, in its Phase I evaluation. The LRSTF felt that a "worst case" design would provide useful information about the robustness of LR soldering processes. As such, good design practices were sometimes deliberately violated (see Section 2.4) in designing the LRSTF board. This approach created some anomalies for both LR boards and RMA controls

(see Sections 4.7 and 4.9). The primary purpose of the LRSTF's Phase II testing program was to verify that problems that affected both RMA and LR boards in Phase I were design related. This Appendix summarizes design modifications, discusses processing for Phase II, compares Phase II test conditions with those used in Phase I, and compares electrical test results for Phases I and II.

A.2 Design Changes in the LRSTF Board

HCLV and HVLC SMT Capacitor Land Spacing

The original design spacing between the lands for C08 to C14 and C26 to C30 (see Figure 2.2) was based on the nominal dimensions of the capacitors. This spacing was slightly too large, so it was decreased by 10 mils to make the assembly of the board easier.

HVLC Vias through the Ground Plane

The ground plane metallization on layer 3 was removed from under the high voltage section to eliminate shorts that occurred during Phase I testing. In addition, all SMT high-voltage traces are now only on the top layer (layer 1) and the PTH high-voltage traces are only on the bottom layer (layer 4). These changes eliminated the possibility of via to ground plane short circuits such as occurred during Phase I. These changes ensure that the circuit board laminate material is not exposed to stress from high voltages.

HSD/SMT Output Trace

The output trace of the HSD/SMT IC was rerouted to avoid passing under the two VCC bypass capacitors. This change eliminated the parasitic capacitance that influenced rise and fall time measurements.

Gull Wing Pattern

The land pattern for the gull-wing device was increased from 25 mils to 25.6 mils to match the leads on the gull wing (the gull wing was not mounted in Phase I due to this mismatch with the land spacing).

Electrical Measuring Points for Stranded Wires

The HCLV test setup and the section circuits were reconfigured to improve voltage measurement accuracy on the stranded wires.

A.3 Processing of LRSTF Test Boards

Figure 3.1 summarizes processing categories for Phase I. Some of these categories were dropped in Phase II. For example, the electrical performance of the FR-4 epoxy boards did not differ appreciably from the polyimide boards in Phase I, so only FR-4 was used in Phase II. It was selected as a worst case because it produced higher ionics in Phase I. Similarly, no differences in electrical performance occurred for the cleaned and not cleaned LR boards in Phase I, so Phase II eliminated cleaning of LR boards. The LRSTF LR boards were processed only at Texas Instruments and the RMA boards were processed at the EMPF (rather than at AlliedSignal as in Phase I).

Without the substrate and cleaning categories, each site processed 25 boards. Five of these boards were used for process setup and the remaining 20 boards (10 with conformal coating and 10 without) were subjected to environmental testing at Sandia. For Phase I, only five boards were used per process category. In Phase II, TI used Kester R-244 paste for reflow, Almit KR-19 Superflow flux for hand soldering (see Figure 3.2 for previous materials), a Zevatech PPM9 for component placement, and an Electrovert Omniflow Forced Convection for SMT reflow (see Figure 3.3 for previous equipment). TI applied the conformal coating to both the LR and RMA boards.

A.4 Test Conditions

Planned environmental test conditions for Phase II were identical to those for Phase I — three weeks of conditioning at 85° C and 85% relative humidity. Electrical measurements were recorded at pre-test and after one, two, and three weeks of environmental conditioning. Due to the unavailability of the test chamber used for Phase I, a different test chamber was used. This chamber was scheduled for replacement, but its life was extended long enough to cover this test. This chamber had an automatic controller, which performed as programmed during the first week of testing, including a scheduled shut down at 7pm at the end of week 1. However, the automatic controller malfunctioned at 9pm (when no one was available to monitor the chamber), which caused the temperature to fall rapidly. By 12am the temperature reached -40° C, which sounded an alarm. Security personnel responded to the alarm at 1am. They called the individual responsible for the chamber, who instructed them to turn the power off and open the door slightly. The warmer outside air entering the chamber quickly condensed and the test boards were *completely soaked* when the door was completely opened at 8am.

The profiles of the extreme temperature and humidity excursions are shown in Figure A.1. These excursions created a *more stressful testing environment* than would be experienced under normal testing conditions.

The chamber controller was checked and put back in use at the start of the second week of environmental conditioning. The controller performed normally for the first 24 hours of environmental conditioning and then again malfunctioned at 9pm. This malfunction caused the temperature to lower, but only down to 20° C. When the problem was discovered the next morning, the individual responsible for the chamber turned the temperature back up to 85° C and put the chamber on manual control for the remainder of the test.

Under normal conditions, a staggered ramp up of temperature followed by humidity is used to avoid condensation. During ramp down the order is reversed. Since the temperature was lowered and then raised while the humidity remained at the 85% test condition, condensation was created, which again produced a *more stressful testing environment*. The temperature and humidity profile for the start of the second week of environmental conditioning is shown in Figure A.2.

In spite of these extreme temperature and humidity excursions, the LR and RMA boards performed as well as or better than in Phase I. The only exception was current leakage for the PGA socket for both LR and RMA boards and for the 10-mil pads and gull wing for RMA. These leakages were due to the condensation caused by the malfunction of the test chamber controller (see Section A.10).

A.5 Test Results for High Current Low Voltage

Electrical measurements were made on the LRSTF boards before environmental conditioning and after one, two, and three weeks of ESS. As explained in Section 4.4, the magnitude of the increase in voltage over pre-test conditions is of interest, so the pre-test voltage measurements were subtracted from those following weeks 1, 2, and 3. These measurements were denoted as Δ_1 , Δ_2 , and Δ_3 , respectively. As given in Equation 4.6, the voltage increase should not exceed 0.356 V (voltage decreases are not of concern). This upper limit included the effect of common mode noise, which was eliminated by the Phase II design changes. The elimination of common mode noise lowered the upper limit for voltage increase in Phase II to 0.13 V. Figure A.3 gives boxplots of Δ_1 for the PTH circuits for both phases of testing with their respective upper limits for voltage change. Results in Figure A.3 for Phase I can be compared directly with those in Figure 4.8 using the following correspondences — the label LR under

Phase I in Figure A.3 corresponds to the results shown in Figure 4.8 for Texas Instruments — recall that TI was the only low-residue site used in Phase II. The RMA results in Phase I were obtained from PWBs processed by AlliedSignal. In Phase II, the RMA PWBs were processed by the EMPF. These correspondences hold for all graphs in this appendix. Results for HCLV SMT are not given for Phase II due to the unavailability of functional SMT components.

Figure A.3 shows that Δ_1 is just above 0.0 V and is smaller in Phase II due to increased test measurement fidelity. Both LR and RMA are well below the new upper limit of 0.13 V. Figure A.4 shows boxplots for Δ_3 , which can be compared with those given in Figure 4.9 for PTH. These values are also well below the 0.13 V upper limit. Results for Δ_2 (not shown) were similar to those for Δ_3 . Figure A.5 gives boxplots of Δ_3 grouped by conformal coating for both phases. All results are close to zero and are similar for both phases.

Figure A.1 Temperature and Humidity Profiles Caused by a Faulty Controller at the End of Week 1 of Environmental Conditioning

Figure A.2 Temperature and Humidity Profiles Caused by a Faulty Controller at the Start of Week 2 of Environmental Conditioning

Figure A.3 Boxplots of ΔV_1 in HCLV PTH Circuit by Phase and Process Figure A.4 Boxplots of ΔV_3 in HCLV PTH Circuit by Phase and Process

Figure A.5 Boxplots of ΔV_3 in HCLV PTH Circuits Grouped by Phase and Conformal Coating

Figure A.6 Boxplots of LR and RMA Phase II Current Measurements (μA) for HVLC PTH Circuit by Test Time and Process

A.6 Test Results for High Voltage Low Current

The four sets of current measurements for the HVLC PTH circuits are shown in boxplots in Figure A.6 (SMT results are not given for Phase II due to the unavailability of functional HVLC SMT components). These results can be compared to the Phase I results shown in Figure 4.14. Note that all measurements in Figure A.6 are very close to 10 μ A, which results in the boxplots appearing as a single horizontal line. All measurements are well within the bounds of 9 μ A and 11 μ A that are identified with horizontal dashed lines in Figure A.6.

The anomalies shown in Figure 4.14 (PTH) due to shorted vias, open resistors, and an incorrect resistor installation are not present in Phase II. The only exception is one data point that is not shown in Figure A.6. This value was 300 μ A and was associated with a LR board. The problem was traced to a 500 V flashover at an inner layer between two pins on the 29-pin test connector. The flashover was related to the dielectric strength of the board (likely exacerbated by high humidity) and not to the LR soldering process. The spacing between the two pins is approximately 0.060 in, which is far in excess of the MIL-STD-275 guidelines for 500V.

A.7 Test Results for High Speed Digital

Rise and fall time measurements were made on PTH and SMT HSD circuits at each testing time in Phase II. Rise time measurements for HSD PTH are shown in Figure A.7. These measurements are well below the upper limit of 7 ns and are approximately 1 ns lower than the Phase I measurements that are also shown in Figure A.7. The slightly lower readings may simply reflect an increase in test signal fidelity due to an improvement in measurement techniques in Phase II. While the Phase II rise times are lower than in Phase I, it should be noted that a few of the Phase I rise time measurements shown in Figure 4.16 for Alliant Techsystems were above 7 ns at week 1. The same is true for one AlliedSignal measurement. Since neither Alliant Techsystems nor AlliedSignal processed LR boards for Phase II, there is no way of knowing if their rise time measurements would also have improved in Phase II.

Figure A.8 gives the corresponding fall time measurements for HSD PTH. These measurements are approximately 1 ns lower than those in Phase I. Figure 4.17 gives fall time measurements for Phase I by site and shows a few values above 7 ns at week 1 for Alliant Techsystems and AlliedSignal. Again, there is no way of knowing if their fall time measurements would also have improved in Phase II.

Figures A.9 and A.10 are analogs of Figures A.7 and A.8 for HSD SMT. Phase II measurements shown in Figures A.9 and A.10 are all below 7 ns, compared to some of the Phase I LR and RMA measurements exceeding 7 ns. The redesign of the LRSTF board to eliminate parasitic capacitance (see Figure 4.20) is the likely reason for this improvement. Based on these results, it seems reasonable to conclude that if Hughes, Alliant Techsystems, and AlliedSignal were to process redesigned boards, they would also show improvement in rise and fall times.

At the suggestion of one of the members of the LRSTF, propagation delay time measurements were added in Phase II to see if they would show any differences in the two soldering processes. Figures A.11 and A.12 display propagation delay times for HSD PTH and SMT circuits. These times are similar for both LR and RMA boards. Propagation delay times are approximately 2 ns/gate. Since the PTH circuits have 2 ICs (8 gates), the propagation delay time could be as long as 16 ns. Likewise, the SMT circuitry with a single IC (4 gates) could have propagation delay times up to 8 ns. The propagation delay times are all close to 11 ns for PTH circuitry and close to 4 ns for SMT circuitry, both of which are well below (better) their respective expected upper limits.

A.8 Test Results for High Frequency Low Pass Filter

High frequency transfer function response measurements were recorded for the low pass filters (LPFs) on the LRSTF functional boards for both PTH and SMT at each testing time in Phase II. The transfer function response was measured at 50 MHz and the frequency was measured at -3 dB and -40 dB. The post-test -

pre-test deltas for the transfer response at 50 MHz are displayed in boxplots in Figures A.13 and A.14 for PTH and SMT, respectively. All deltas for both Phase I and II are very close to zero and are well within the ± 5 dB test plan criterion. The outlying point in Figure A.14 was due to the failure of component C20.

Figure A.7 Boxplots of Rise Times (ns) for HSD PTH Circuits by Test Time and Process

Figure A.8 Boxplots of Fall Times (ns) for HSD PTH Circuits by Test Time and Process

Figure A.9 Boxplots of Rise Times (ns) for HSD SMT Circuits by Test Time and Process

Figure A.10 Boxplots of Fall Times (ns) for HSD SMT Circuits by Test Time and Process

Figure A.11 Boxplots of Phase II Propagation Delay (ns) for HSD PTH Circuit by Test Time and Process

Figure A.12 Boxplots of Phase II Propagation Delay (ns) for HSD SMT Circuit by Test Time and Process

Figure A.13 Boxplots of Δ_3 in the PTH LPF 50 MHz dB Response by Phase and Process

Figure A.14 Boxplots of Δ_3 in the SMT LPF 50 MHz dB Response by Phase and Process

Figure A.15 Boxplots of Δ_3 in the PTH LPF Frequency Response (MHz) at -40 dB by Phase and Process

Figure A.16 Boxplots of Δ_3 in the SMT LPF Frequency Response (MHz) at -40 dB by Phase and Process

The frequency at -40 dB for PTH and SMT are displayed in boxplots in Figures A.15 and A.16. The test plan criterion for change in frequency from pre-test was ± 50 MHz. The changes were all within this criterion except for one RMA board and one LR board.

The anomaly on the RMA board was attributed to an open circuit and the anomaly on the LR board was due to the failure of component C20. The frequency data at -3 dB were similar to those at -40 dB.

A.9 Test Results for High Frequency Transmission Line Coupler

High frequency measurements were recorded for the transmission line coupler (TLC) on the LRSTF functional boards at each testing time in Phase II. Forward coupling measurements were made at 50 MHz, 500 MHz, and 1 GHz. Reverse coupling frequency and response measurements were taken at the null point (see the minimum point on the dashed line in Figure 2.17). The 50 MHz forward coupling measurements are displayed in boxplots in Figure A.17. These boxplots show that the Phase II measurements are all less than the test plan criterion of -33 dB

and are all slightly lower (better) than the corresponding Phase I measurements. Also, the variability in the Phase II RMA measurements is greater than in Phase I, but similar to those of LR in Phase II.

The reverse coupling null measurements are displayed in boxplots in Figure A.18. These measurements were also all less than -33 dB. These boxplots show that the LR measurements are all slightly lower (better) in Phase II and slightly lower than the RMA measurements, which are about the same as in Phase I.

A.10 Test Results for PGA, Gull Wing, 10-Mil Pads, and Stranded Wires

PGA. The layout for the PGA socket was previously shown in Figure 2.19. Leakage measurements were made between the two inner squares (PGA-A) shown in this figure and between the two outer squares (PGA-B). The two outer squares were covered with solder mask to provide a direct comparison with a similar pattern without solder mask. Measurements were made at each testing time in Phase II.

During Phase I testing, 720 leakage measurements were made on PGA-A (see Figure 4.29) and another 720 were made on PGA-B (see Figure 4.30). An additional 40 measurements were made on each of PGA-A and PGA-B during Phase II pre-tests. Thus, a total of 1520 consecutive leakage measurements were made prior to the failure of the chamber controller, which caused the extreme temperature and humidity profiles shown in Figure A.1. These 1520 measurements were all in the "noise level" and far below the upper limit of 1000 nA.

Leakage measurements made at the end of week 1 of ESS in Phase II (after the failure of the chamber controller) showed that some RMA and LR boards exhibited erratic and inconsistent leakage measurements that were well above the 1000 nA criterion. The Phase II leakage measurements for PGA-A and PGA-B are shown by test time in boxplots in Figures A.19 and A.20, respectively. At the end of week 3 of ESS, two RMA boards and four LR boards exhibited excessive leakage measurements.

Since the 1520 consecutive leakages mentioned above were made without condensation and without applied bias, it was felt that the heavy condensation on the PWBs, due to the failure of the test chamber controller (see Section A.4), in conjunction with the applied bias could have created leakage paths through the formation of dendritic filaments. Thus, these six boards were sent to Texas Instruments for further examination to determine the source of the leakage. Four of these six boards were selected for further evaluation: #4 (RMA) and #21, #30, and #35 (all LR).

Leakage was measured at TI on PGA-A, PGA-B, and between PGA-A and PGA-B with 5 VDC bias in forward and reverse polarity. The leakage was measured at least four separate times during the analysis. The erratic and inconsistent readings observed during testing at Sandia were confirmed. The leakage current changed over many orders of magnitude during these tests. High leakage (approximately 1 mA or greater) was observed on at least one test for boards #4, #21, and #30.

The layer 2 traces from P1 to the PGA were severed at the PGA to isolate the source of the leakage. A Dremel bit was used to make a plunge cut on boards #4, #21, and #30. Subsequent electrical testing isolated the leakage to the PGA.

Board #30 (LR) exhibited high leakage on PGA-A, PGA-B, and from PGA-A to PGA-B. This board was vacuum baked to determine if the leakage was related

Figure A.17 Boxplots of HF 50 MHz Forward Coupling Response by Test Time and Process (upper limit = -33dB)

Figure A.18 Boxplots of HF Transmission Line Reverse Null Coupling Response by Test Time and Process (upper limit = -33dB at pre-test and -31dB thereafter)

Figure A.19 Boxplots of Phase II PGA-A Current Leakage (nA) by Test Time and Process (no solder mask)

Figure A.20 Boxplots of Phase II PGA-B Current Leakage (nA) by Test Time and Process (solder mask)

to moisture remaining on the board. It was placed in a 50°C chamber at -28 in Hg for 12 hr. The subsequent electrical test did not identify a significant decrease in leakage.

Board #4 (RMA) exhibited high leakage only on PGA-A. This board was cold soaked at -40°C for 2 hr, removed and allowed to become wet with condensation in an attempt to duplicate the conditions caused by the chamber malfunction at week 1. Then it was baked at 35°C for 2.5 hr and tested. The leakage decreased slightly on PGA-A, so the presence of moisture without bias does not appear to be a contributing factor to leakage. This suggests that the leakage was *not* due to ionic contamination, rather the moisture (as described in Section A.4) in conjunction with bias was most likely necessary to promote the original leakage mechanism through the growth of conductive filaments.

Board #21 (LR) exhibited leakage greater than 1 mA at 5V. It was felt that any conductive filaments on this board would likely be observable under 10X magnification. The PGA socket on this board was encapsulated with a transparent epoxy and evacuated to eliminate voiding. The PGA was then removed with an end mill to expose the layer 1 pads on the board under the PGA. The deposits were observed in-situ through the epoxy.

Dendritic structures were observed in some areas, although they were difficult to detect under 10X magnification. The growth orientation of the traces was from the inner trace of each circuit pair (A and B). There also appeared to be general degradation of the traces, with the underlying copper exposed in many areas. This was evident on only two (the outer trace of circuits of A and B) of the four traces under the PGA. The DC bias that induced the migration was applied with the positive voltage on the outer traces of the A and B circuits. It was apparent that the conformal coating did not coat the area under the PGA.

The PGA socket on board #4 (RMA) was encapsulated and removed in the same manner used with Board #21. This board also showed the presence of dendritic filaments, but to a lesser degree than board #21. The copper traces appeared to be intact. Boards #4 and #21 were the only ones examined for the presence of dendritic filaments.

Uncoated boards (#4, #22, #30) exhibited the appearance of corrosive attack on the solder joints, as evidenced by white powdery deposits on the GW traces and between the backside solder fillets. A sample of the deposit on board #30 was removed for elemental analysis. Multiple scans of this sample

revealed similar results: oxygen, lead, tin, and copper in various ratios. These results are consistent with moisture on a solder joint.

Summary of PGA Analysis. The electrical leakage at the PGA test patterns was likely due to electrochemical migration of the constituent metals on the PWB. This is supported by four primary observations:

1. The magnitude of the leakage with only a 5V bias suggests a metallic bridge, rather than corrosion products of the metals.
2. Elemental analysis identified the presence of all three of the available metals (copper, tin, and lead).
3. Degradation on the traces (board #21) and the dendritic structures appear to have a preferred orientation that corresponds to the applied voltage during the environmental test.
4. The magnitude of the leakage was not affected by removing the moisture with a vacuum bake.

Electrochemical migration requires surface moisture (such as was created when the test chamber controller failed to operate properly), absorbed or condensed, and the application of an electrical (DC) bias. It has been demonstrated that tin, lead, and copper electrodes will form dendritic structures across an insulator when wet with distilled water and bias is applied (1). Other experimental work has shown that the presence of condensed water on an insulator increased the speed and severity of the electrochemical migration by several orders of magnitude versus an elevated temperature/humidity environment (2).

The erratic and inconsistent leakage measurements on the RMA and LR boards may have been due to the delicate dendritic structures becoming intermittent due to handling induced shock and vibration. The polarity dependent growth of the dendrites is a likely explanation for the variation in leakage as a function of test polarity.

Gull Wing. A nonfunctional gull wing device was planned to be soldered in Phase I. As explained in Section A.2, the GW device was not used due to a mismatch between the actual spacing of the GW device (25.6 mils) and the lands on the PWB (25 mils). The board layout was modified in Phase II to allow the GW device to be soldered to the board. The lands of the GW device were daisy chained (every other land was connected to form two parallel paths around the device). Hence, total leakage measurements were made on adjacent lands of the GW device. These measurements are displayed in boxplots in Figure A.21.

Figure A.21 shows all GW leakage measurements within test criterion at pre-test and at the end of week 1 of ESS. At the end of week 2 of ESS, three RMA boards and one LR board exceeded the test criterion. At the conclusion of ESS, the LR board returned to a normal reading while three RMA boards remained considerably above the test criterion. Of these three RMA boards, two were repeats from week 2 and one was on a new board. Since only the RMA boards had excessive current leakage at the conclusion of environmental conditioning, they were not analyzed further. However, these leakages are likely due to the formation of dendritic filaments as was discussed above with respect to the PGA socket.

10-Mil Pads. The 10-mil pads were laid out in two rows of five pads each and the pads within each row were connected on the bottom layer of the board. The 720 leakage measurements for Phase I were previously shown in boxplots in Figure 4.31. These measurements were all in the "noise level" and well below the upper limit of 1000 nA. Phase II leakage measurements are shown in Figure A.22. The upper limit for current leakage in the test plan was 1 μ A (1000 nA) for the 10-mil pads. Figure A.22 shows all leakage measurements within the test criterion at pre-test and at the end of week 1 of ESS. One LR board had a leakage current equal to the test criterion at the end of week 2. At the conclusion of ESS, this LR board had a reading near zero, while two RMA boards

exceeded the test criterion. In addition, one other RMA board produced an unstable reading. Since only the RMA boards had excessive current leakage at the conclusion of environmental conditioning, they were not analyzed further. However, these leakages are likely due to the formation of dendritic filaments as was discussed above with respect to the PGA socket.

Stranded Wires. Two 22-gauge stranded wires were hand soldered as previously shown in Figure 2.20. Stranded wire 1 was soldered directly into plated through holes and stranded wire 2 was soldered to two terminals. Voltage for stranded wire 1 was measured from probe points directly on the wire. Voltage for stranded wire 2 was measured from terminal to terminal. Use of the terminals increases the resistance and produces higher voltages.

The voltage measurements for stranded wires 1 and 2 are displayed in boxplots in Figure A.23 and A.24, respectively. These measurements are quite similar for both RMA and LR processing. Stranded wire 2 measurements are approximately 5 mV higher than those for stranded wire 1 due to the added resistance from the terminals. The test criterion calls for an increase in voltage over pre-test measurements of no more than 35 mV. As can be seen in Figure A.24, it is mathematically impossible to have a voltage change as large as 35 mV, so these test data were not analyzed further.

A.11 Summary of Phase II Test Results

Phase II testing used a redesigned board to verify that problems that affected both RMA and LR boards in Phase I were design, not process, related. These design related problems arose as the result of deliberate decisions by the LRSTF to challenge MIL-STD-275 design guidelines in order to evaluate the robustness of LR processing. Not only were MIL-STD-275 guidelines challenged, but in some cases good design practices were deliberately violated (see Section 2.4).

In normal manufacturing environments, good design practices would not be challenged and problems such as were encountered in Phase I would be discovered and corrected prior to actual production runs.

However, the short time schedule for Phase I did not allow for these normal procedures.

Phase II testing was successful in verifying that problems that affected both RMA and LR boards in Phase I were design related. Overall, Phase II performance was as good as or better than that observed in Phase I. The only problem area encountered in Phase II was due to dendritic filaments that were formed as a result of bias applied to the PWBs with heavy condensation, which occurred when the test chamber controller malfunctioned. The dendrites caused high current leakages at the PGA socket, gull wing, and 10-mil pads on RMA/cleaned boards and at the PGA socket on LR boards.

A.12 References

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- (2) Krumbein, S. J., "Metallic Electromigration Phenomena," IEEE Trans. on Comp., Hybrids, and Manufacturing Tech., Vol 11, No. 1, 1988.

Figure A.21 Boxplots of Phase II Gull Wing (25.6 mil pitch) Current Leakage (nA) by Test Time and Process

Figure A.22 Boxplots of Phase II 10-Mil-Spaced Pads Current Leakage (nA) by Test Time and Process

Figure A.23 Boxplots of Phase II Voltages (mV) for Stranded Wire 1 (soldered to the PWB)

Figure A.24 Boxplots of Phase II Voltages (mV) for Stranded Wire 2 (soldered to terminals)

A.13 Additions to Distribution List

Husamuddin Ahmadzai - Swedish Env. Prot. Agency
 Mir Ali - London Chemical Co.
 Barry Allen - USAF ESC/ZJ
 Leon E. Allen - Automotive Controls Corporation
 David Andrews - GEC-Marconi
 Bernard Aronson - Electronic Industries Assoc.
 Jerry Arreola - Pargain Technologies
 Sherman Banks - Trimble Navigation
 Charles Bauer - TechLead Corporation
 Bryan Baxter
 Roland Beaudette - State of Massachusetts
 George Behlke - Detection Systems
 Vic Beldans - Marquette Electronics
 Diana J. Bendz - IBM Corp.
 Col. James Beres - USAF ESC/TD
 Normand J. Bergeron - USAF ESC/EN-2
 Jeff Bighan - Lockheed Martin
 Ed Bingle - Cisco Systems, Inc.
 Wayne Bishop - Boeing Commercial Airplane Group
 Commander P. Blakley - Naval Surface Warfare Center
 Greg Blalock - Naval Air Warfare Center
 Phillipe Blostein - Air Liquide
 Brian Bode - Circuit Image Systems
 Arnold Bonadies - Sikorski Aircraft
 John J. Boericke - Performance Controls
 Tom Borkes - The Jefferson Project
 Ron Boyce - Tektronix, Inc.
 David Boyle - Northrop Corporation
 Peter Bratin - ECI Technology
 David Brendley - De Amertek
 Stan Browne - University of Texas El Paso
 Bill Brox - IVF
 Donald Burr - Unisys Corporation
 Maj. Samuel Carbaugh - USAF WL/FIVS
 Tara Carleton - Sverdrup Technology Inc.
 Charles Carpenter - Waste Policy Institute
 Al Cash - Northrup Grumman
 Pakasit Chanvinij - Thai Airways International Ltd.
 John R. Chase - American Technical Ceramics Corp.
 Tom Chung - Tandem/MCC
 Ray Cirimele - Elect. Mfg. Prod. Fac.
 Dominick Cizek - Talla-Com
 Mike Clark - Sketchley Dry Cleaners
 David P. Connor - USAF ESD/EN-E
 Jorge Corona - Env. Comm. of Mexico
 Peter Cote - Hamilton Standard
 Bill Craver - Eastern Electronic Devices
 Art Crisostomo - 35 Systems
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 Marc J. Dalderup - Dover Soltec
 Doug Dalessio - USAF ESC/AVJ
 Shigeru Dejima - Fabricare Research Center
 Lawrence H. Dubois - ARPA/DSO
 Bernie Dufort - NCR Corporation
 Scott Elrod - SEMATECH
 Stephen Evanoff - Lockheed Martin Corporation
 Greg Evans - Indium Corporation of America
 Arnold Ferreri - Grumman Corporation
 Alan Filip - United Technologies
 Yitzhak Firestein - Tadiran Telecommunications Ltd.
 John Fisher - AT&T Bell Laboratories
 Art FitzGerald - IFC
 Joseph M. Fletcher - Boeing
 Frank Foederl - AT&T Bell Labs
 Richard E. Forslind - Kaiser Electronics
 Pamela Foster - Friends of the Earth
 Rick Freeman - Boeing Commercial Airplane Group
 Rich Freiburger - GSS Array Technology, Inc.
 Yuichi Fujimoto - JEMA
 Ing. G. Gabelmann - ITT Teves GmbH
 Marco A. Garcia - Hughes Aircraft Co.
 Tim Ginzburg - Zytec Corporation
 Johnny L. Golden - Boeing Defense and Space Group
 Gene Green - Boeing Commercial Airplane Group
 Col. Harvey Greenberg - USAF SSC/XOC
 James R. Hale - Litton Guidance & Control Systems
 Michael Hall - Dept. of Trade and Industry
 Jack Hallgren - General Electric
 Thomas M. Hallworth - AT&T Network Systems
 Lt. Darwin Hemeyer - USAF ESC/ICI
 Ralph Hermansen - Hughes Aircraft Company
 Tim Hines
 Rose Hoff - Stratacom
 Ed Holton - Lectron Products, Inc.
 Maj. Scot Hoskins - USAF AFMC/XRMP
 Rod Howell - Libra Industries
 Don E. Hunt - USAF AGMC/CN
 Ray Iannuzzelli - Digital Equipment
 Bruce Inpy - Pitney Bowes
 Yoshiyuki Ishii - Hitachi Ltd.
 Joe Jackson - Naval Air Warfare Center
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 Kevin Joback - Molecular Knowledge Systems
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 Steve Lai - Singapore Inst. of Stand. & Indust. Res.
 Leo Lambert - Digital Equipment Corporation
 Bill Lee - Rockwell International
 Dale Lee - Evans & Sutherland
 Tom Lepsche - Honeywell, Inc.
 Bud Levine - Deft Chemical Coatings
 Donald Liebo - Universal Electronics
 George Lindner - Symbol Technologies
 Bjorn Lindstrom - Ericsson Radar Electronics
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 Tim Nolan - CompuServe
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 Othmar Ober - Temic
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 Michael Pavlov - ECI Technology
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 William M. (Pete) Peterson - ECI Technology
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