Design of Intertransition Digitizing Decomutator

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Abstract

Development of automated test equipment for an advanced telemetry system in weapon applications requires capturing and analyzing Terminal Data Analyzer (TDA) data. TDA data is generally a quick burst of Pulse Code Modulated (PCM) data which relates the status of the weapon just prior to impact. Many systems use bit sampling to capture the state of the data stream at periodic intervals. This method may fail to capture glitches in the data stream if two transitions occur between sampling intervals. A more complete method of data capture was desired. The solution was intertransition digitization. Intertransition digitization captures all transitions in the data stream while keeping track of the time elapsed between transitions.

Summary

Capturing TDA data is a routine part of testing telemetry units for a weapon system. TDA data is a quick burst of PCM data relating the status of a weapon just before impact. Most PCM decoders use bit synchronization to synchronize the decoder with the data being captured. Bit synchronizing decoders work well for many applications, but there are some cases that cause problems for them. When a long stream of bits occurs without change, or glitches occur at the wrong time, or the duty cycle is significantly off 50%, then a bit synchronizing decoder will have problems. This project was set up to create a decoder that is less susceptible to these types of problems. The method of intertransition digitization was conceived. This method digitizes the amount of time that occurs between transitions of the data.

The intertransition digitizing decoder was created using an Intel single board computer with a Multibus I backplane and compatible chassis. There are two custom boards for capturing the data. Two IEEE 488 interfaces are used to pass commands and data between the decoder and the test system controller. Four to 16 Mbytes of storage are available to store the captured data. A custom operating system was written to wed the commercial hardware to the custom hardware.

Discussion

Scope and Purpose

Development of automated test equipment for an advanced telemetry system in weapon applications requires capturing and analyzing TDA data. TDA data is generally a quick burst of PCM data that relates the status of the weapon just prior to impact. Most PCM decoms use bit sampling to capture a data stream. Bit sampling works well when the data being captured has a 50% duty cycle and is glitch free. A bit synchronizer uses the transitions of the PCM stream to delay a fixed amount after each transition before the sample is taken. Glitches in the data stream can throw off the bit synchronizer, causing extraneous bits to be captured. If the duty cycle strays too far from 50%, then it can be difficult to determine the correct amount of delay to use between the bit synchronizer and the bit sampler. Bit synchronization also has problems when a series of sequential bits have the same value, causing the PCM stream to have no transitions. This project was initiated to find a better way to capture PCM data from streams that present problems for bit sampling decoms.

Activity

This project involved putting together a PCM decom that would overcome the shortfalls of the bit sampling style of decom. A bit sampling decom triggers a delay circuit at each signal transition. The delay circuit allows the signal sample to be taken at some time after the signal transition occurred. This allows the measurement to be made when the signal is at a DC level between transitions. This is illustrated in Figure 1. Decoding the data after the capture requires the assumption that each of the bits in the stream was taken at a periodic rate. If a large enough glitch occurs during the capture, then an error is introduced into the data stream.

Figure 1. Bit Synchronizer of a Bit Sampling Decom

The intertransition digitizing decom captures all of the transitions that occur in the data stream and records the amount of time that occurred between each of them. This is illustrated in

Figure 2. Recording the time values between all of the transitions allows the decoding software to identify glitches because of the shorter than normal time values. Since the glitches can be identified, they can be ignored during the decoding process.

Figure 2. Transition Digitization

Hardware

The system was created using an Intel single board computer in combination with the Multibus I specification and a compatible chassis. Two custom-printed circuit boards were designed to perform the digitizing work. Two IEEE-488 interfaces were added to the single board computer.

Chassis

The chassis is an Intel iSBC 661 chassis. It contains an eight-slot cardcage and backplane assembly, a power supply, a dual cooling fan, a line filter, and a reversible control panel all completely enclosed within an aluminum alloy housing. The chassis may be installed as a desktop unit or may be rack mounted in a standard 19-inch cabinet. The chassis is shown in Figures A-1 and A-2 in the Appendix.

Multibus

The Intel Multibus backplane was selected because of its 32-bit data path.

Single Board Computer

The iSBC 386/12 single board computer is used as the controller for the decom system. The computer provides two serial ports, one parallel port, a programmable interval timer, a Multibus interface, and has 1Mbytes of EPROM. The board also supports the use of Intel's ICE 386 emulator for debugging purposes

Memory Disk

The memory disk is composed of one to three Intel iSBC 040EX memory boards. These boards each contain 4 Mbytes of DRAM storage accessible through the Multibus interface. The amount of memory installed for the memory disk determines the amount of burst data that can be stored before the data must be analyzed and purged.

Operating System

The operating system is custom built using the Intel C compiler. The actual code is composed of both C source and 80386 Assembly code. A 32-bit flat memory model was used.

IEEE 488

The decom contains two IEEE 488 interfaces. One interface is used to send commands to the decom from the test system's computer controller. The other interface is used to get data back from the decom. In previous generations of the decom, the GPIB would sometimes lock up during a data transfer. If the decom locked up, the only way to regain control was to manually press the reset button on the front of the device. With a second interface, the user is able to continue sending commands to the decom if it locks up during a data transfer. A remote software reset can be sent to the decom to regain access and attempt the data transfer again.

Custom Boards

The first custom board, shown in Figure A-3, handles the trigger functions. It keeps track of the start and stop addresses in memory that the digitized stream is recorded into. The second custom board, shown in Figure A-4, performs the actual digitizing. It contains the digitizing counters and the memory that the values are recorded into. Both boards are designed with Programmable Logic Devices (PLD) to reduce the amount of printed circuit board space required.

Theory of Operation

The decom actually begins digitizing from the moment that initialization is complete upon power-up. Figure 3 shows a simplified block diagram of the digitizer design. With the digitizer actually digitizing before a trigger occurs, the decom is able to capture and analyze pretrigger data. The time stamp is zeroed upon power-up, with certain default characteristics being preset. When the digitizer begins digitizing, the counter in Bank 1 begins counting from 0. When the next transition occurs, the value in the Bank 1 counter is stored into the Bank 1 memory and the counter in Bank 2 begins counting from 0. With each successive transition, the bank counter value is written into its corresponding bank memory and the next bank begins counting. When the fourth bank writes its count to memory, Bank 1 begins counting again. Each bank memory has its own address counter to ensure that the digitized values are stored sequentially within its bank. The address counters wrap around when the end of their address range is reached.

Figure 3. Diagram of Digitizer

When the decom is triggered, the capture controller latches the start address of each of the bank memory address counters. When the capture is completed, the ending address is latched and the single board computer generates a header for the captured burst which includes such things as the burst label and time stamp information. The computer then uses the latched start and stop addresses to copy the digitized data from the bank memories to the memory disk. Once the transfer to the memory disk is completed, the computer resets parameters in the digitizer, allowing it to resume digitizing.

Accomplishments

The reason for designing the decom was the need to be able to maintain lock on a data stream with long intervals of repeating bits. There was also a need to be able to identify a glitch when it occurs. Some new test systems are requiring the ability to store longer data streams than in the past. These reasons serve as the criteria to which the decom was evaluated.

Most decoms with bit synchronizers will loose lock on the PCM stream with certain types of encoding when long intervals of repeating bits occur because there are no transitions. Lock is lost because it is unlikely that the sampling frequency exactly matches the frequency of the data being captured. With the intertransition method, the decom is able to compensate for the frequency differences through software. Glitches are easy to identify in the software because of the very short time interval between transitions with respect to the duty cycle of the data. The decom was also able to capture longer data streams with the increased size of the bank memory. The decom can capture data for 131,000 transitions before the bank memory is filled.

Appendix
Decom Views

Figure A-1. Front View of the UB1200 Decom

Figure A-2. Rear View of the UB1200 Decom

Figure A-3. Custom Board for Triggering the Decom

Figure A-4. Custom Board for Digitizing and Storing Data to the Bank Memory