Ion Beam Induced Charge Collection (IBICC) From Integrated Circuit Test Structures Using a 10 MeV Carbon Microbeam

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As feature sizes of Integrated Circuits (ICs) continue to shrink, the sensitivity of these devices, particularly SRAMs and DRAMs, to natural radiation is increasing. In this paper, the Ion Beam Induced Charge Collection (IBICC) technique is utilized to simulate neutron-induced Si recoil effects in ICs. The IBICC measurements, conducted at the Sandia National Laboratories, employed a 10 MeV carbon microbeam with 1 μ m diameter spot to scan test structures on specifically designed ICs. With the aid of IC layout information, an analysis of the charge collection efficiency from different test areas is presented.

INTRODUCTION

Ionizing particles that affect ICs include alpha particles emitted by trace amounts of radioactive atoms in the memory chip packaging materials (1) and cosmic ray produced neutron induced Si recoil or reaction products (2). The ionizing radiation passes through an IC, deposits energy along the track, and generates excess electron-hole pairs. The device junctions can collect the induced charge before electron-hole recombination occurs. High electric field gradients present near the junctions can enhance the charge separation and collection due to the charge funneling effect (3). If the induced charge collection by the IC exceeds a critical threshold charge, the state of the IC can be altered. For example, the memory state of a bit in SRAMs or DRAMs (Static or Dynamic Random Access Memories) can flip, and thereby produce a soft error, or Single Event Upset (SEU).

The critical volume V_c is defined as the enclosure volume of an ionizing particle track, which contains just enough induced charge Q_c to cause a circuit upset. As the critical volume V_c dimensions decrease with smaller feature sizes of unhardened ICs, the critical charge Q_c also tends to decrease due to voltage scaling, lower cell capacitance, etc. Bragg curves of generated charge (fC/ μ m) versus particle penetration length are shown in Figure 1 for the ions Si, Al, Mg, Na, F, C, and He, which were obtained by the conversion of Linear Energy Transfer (LET) versus depth using TRIM-96 (4). The area under each curve is the total charge generated by the respective ions. Each ion (except helium) can induce hundreds of fC of charge within a few microns to upset almost any modern circuit. Studies have shown that cosmic ray produced neutron induced soft errors

will dominate for the 64M DRAM generation and beyond compared with the alpha-induced errors. The reason is the higher LET for neutron-induced Si recoils or reaction products compared to alpha particles within the smaller sensitive volume (5).

FIGURE 1. Bragg curves for various ions passing through silicon using TRIM-96.

The response of ICs to natural radiation is therefore of great concern for the reliability of future devices. Immunity to soft errors is listed as a requirement in the semiconductor technology roadmap (6). It is essential to create and test accurate models of induced charge collection and transport. The induced dense plasma around the track of an energetic heavy ion from an accelerator can be regarded as a reasonable experimental analogy for cosmic neutron induced recoil or reaction products passing through ICs. A heavy ion microbeam produced by an accelerator is an ideal tool to study charge collection processes in the ICs and to locate the weak nodes and structures for improvement through design hardening.

In this paper, Ion Beam Induced Charge Collection (IBICC) is utilized to simulate neutron-induced Si recoil

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effects in ICs (7). Specially designed test structures were studied using a Carbon ion microbeam produced at the Ion Beam Materials Research Lab at Sandia National Laboratories. Similar test structures had been studied using a moderate resolution pin-hole external beam system at the University of North Texas (8).

EXPERIMENTAL DETAILS

Nuclear Microprobe and Data Acquisition

The IBICC measurements, conducted at the Ion Beam Materials Research Lab at Sandia National Laboratories, employed a carbon microprobe with a 1 μm diameter beam spot size to scan test structures on specifically designed ICs. The beam scanning area was calibrated using the known feature sizes of scanning test structures. The ion-induced charge was measured using standard charged particle detection electronics, except that the detector was the IC itself. The collected charge was converted to charge pulse heights after passing through a charge-sensitive preamplifier (Ortec 142A) and an amplifier (Ortec 590). The pulse heights are digitized and recorded along with the scanning beam (X,Y) coordinates in list mode by a computer for off-line analysis. In order to minimize ion induced damage effects on samples, the test structures were optically targeted using a front viewing microscope and then scanned by the beam (9).

Test Structures

The specifically designed ICs contain various kinds of test structures. The ring-gate-inner diodes and large diode were used for the IBICC measurements. These diodes are formed from the diffusions in a p-substrate. Test structures are separately connected through different metal pads for outside packaging wires, thereby allowing the operating voltage of test structures to be controlled independently.

The ring-gate-inner diodes are one test node of a 6T-CMOS test structure, which is specifically designed to measure the charge collection from junctions typical of SRAMs and DRAMs. Figure 2 is the 6T-CMOS equivalent circuit diagram (A) and charge collection node (B) with cross sectional view (C). The ring and inner diodes are formed from the contact diffusions of an n-channel MOSFET in a p-substrate. The gate (G3) of this transistor is a square ring, completely enclosing the inner diffusion diode. The ring diode is the ring-shaped diffusions surrounding the gate. The diode voltages can be continuously monitored by source follower transistors. The gate width was chosen to be the approximate node-to-node spacing of memories rather than typical of the pass gate width of DRAMs.

The shape of the large diode is defined in Figure 3. The metal lines are mapped on the top of the large diode. The large diode contains three metal pads, the middle one is used for wiring, and the other two are only used as references. The area enclosed by the square box

corresponds to the beam scanning area ($240\mu\text{m} \times 240\mu\text{m}$). The labeled areas A, B, and C in Figure 3 were selected to study the charge collection efficiency with different reverse biases applied on the large diode.

FIGURE 2. An equivalent circuit diagram of 6T-CMOS test structure (A) and the ring-gate-inner FET node (B) with the cross sectional (AA') view (C). The area of the ring diode is $25\mu\text{m} \times 25\mu\text{m}$, the inner diode is $10\mu\text{m} \times 10\mu\text{m}$, and the gate width is $2\mu\text{m}$.

FIGURE 3. The design layout for the large diode. The areas labeled A, B, and C were selected to study charge collection efficiency with different reverse biases. A, B, and C correspond to large diode with SiO_2 , metal pad, and metal line as top layer, respectively. The solid areas of the metal pads were $100\mu\text{m} \times 100\mu\text{m}$ window cuts used to bond wires.

RESULTS AND DISCUSSIONS

Figure 4 and Figure 5 are IBICC measurements on the ring-gate-inner FET with gate G3 off (0V bias) and gate G3 on (4V bias), respectively. The V_{in} and V_{dd} of the source followers in Figure 2-A were tied together and fed into the preamplifier, which was biased at 3 V. The source

followers were biased at -1.4 V. The gates (G1 and G2) were set on with 4V bias. The p-substrate was grounded. The microbeam was scanned over a $60\mu\text{m} \times 60\mu\text{m}$ area. The counting rate of charge collection was about 2×10^3 counts per second (cps). Because of the different charge collection efficiencies for different regions, the 3D images (Figures 4-A and 5-A), show the differential charge collection abilities around the FET. The total charge collected by a pin diode was used to calibrate the measurements. Figures 4-B and 5-B are the images based on the median values of collected charge. Figures 4-C and 5-C are charge collection cross sectional views from the slices shown in Figures 4-B and 5-B, which are cut along the X-axis at the central Y-axis.

FIGURE 4. IBICC measurements on the ring-gate-inner FET test structure with gate G3 off. A is the 3D image around the FET, B is the median value of the collected charge, and C is the cross sectional view of the slice which is cut along the X-axis in B at the central Y-axis.

In the central region of Figure 4-A, the charge forms a square crater shape, which corresponds to the area enclosed by G3. As a comparison with central region of Figure 5-A, the charge forms a flat mesa, which can be related to the entire area of the FET. The discontinuities of the collected

FIGURE 5. IBICC measurements on the ring-gate-inner FET test structure with G3 on. Other details are the same as Figure 4.

charge in Figures 4-C and 5-C indicate the transition from the outside to the inside of the ring diode. When ions strike outside the ring diode, charge is exclusively collected by the outer ring diode whether the gate G3 is on or off, and the collected charge decreases as the ions strike spots further away from the diodes. In the central region of Figure 4-C, charge is collected from the inner diode. There are two channels (through V_{in} and through V_{dd} of the source followers) to the preamplifier for charge collection. When the G3 is turned off, the charge is coupled in AC fashion to V_{dd} through the gate oxide capacitance of the inner source follower. The collected charge is an indication of the voltage change when ions strike the inner diode. Also charge is localized to the inner diode when ions directly strike the inner diode. When ions strike the gate area with G3 off, the collected charge is smaller than that with G3 on, and decreases with distance when the ions strike closer to the inner diode but further from the gate area (Figure 4-C). When G3 is turned off, only the charge coupled through the V_{dd} of the inner source follower is registered as the ions striking spots move closer to the inner diode. When G3 is turned on, the charge from the gate area is totally collected through both channels. Therefore, the charge is shared

between the inner and ring diodes when ions strike the gate G3 area as shown in Figure 2-C.

It is interesting to note that a junction is shown at the lower part in Figures 4-B and 5-B, which locates another independent source follower. This source follower includes a pn junction directly coupled to V_{dd} . The charge collection from this source follower confirms that charge collection from V_{dd} exists. But it is direct charge collection rather than the AC coupled charge collection to the inner diode through the source follower gate.

The measured charge is about 80fC when ions directly strike the charge collection node from the ring-gate-inner FET (inner diode size $10\mu\text{m} \times 10\mu\text{m}$). Previous work using 11MeV F as incident ions showed that the collected charge for ions directly striking the inner diode ($5\mu\text{m} \times 5\mu\text{m}$) is about 110fC (8). With reference to the Bragg curves for the different ion species with the same effective track length in silicon, the values are consistent. This leads to another interesting question about how much collected charge is contributed by the AC charge coupling through the V_{dd} of the inner source follower. The flat top of the charge collection with gate G3 on (Figure 5) suggests that the AC coupling charge is a secondary contributor compared to the direct charge collection by the diode. This may be due to different response times between charge collection from the diode and the source follower.

In Figure 6, the median values of the collected charge from selected areas (A, B, and C) as shown in Figure 3 are plotted again the reverse bias applied to the large diode. Basically, the collected charge under the metal line and the metal pad follow the same ascending trend as the large diode with increasing reverse bias. The similarity among the trends can be demonstrated by shifting the curves with constant offsets. This indicates that the main difference in collected charge is the differential energy loss as the particles pass through the overlayers such as SiO_2 , metal pad and metal line. Because there are window cuts on the metal pads which are used to bond the packaging wires, the charge collected from the metal pad is more than that from the metal line.

FIGURE 6. The median values of collected charge from the selected areas A, B, and C shown in Figure 3.

In Figures 4-C and 5-C, charge collection has non-symmetric shoulders for the two sides of the ring diode. This is due to a metal line that runs above one side of the ring diode.

It is observed that the charge collection from the large diode is about three times larger than that from the ring-gate-inner FET test structure. It has been suggested that the larger junction has higher efficiency for charge collection by the funneling process (10). The reason is that the large diode has a bigger solid angle for collecting the induced charge along an ion penetrating track than that for the ring-gate-inner FET test structure.

CONCLUSION

In the present work, a 10 MeV Carbon high-resolution microbeam was used to demonstrate the differential charge collection efficiency in ICs with the aid of the IC design information. When ions strike outside the FET, the charge was only measured on the outer ring, and decreased with strike distance from this diode. When ions directly strike the inner and ring diodes, the collected charge was localized to these diodes. The charge for ions striking the gate region was shared between the inner and ring diodes. The IBICC measurements directly confirmed the interpretations made in the earlier work (8).

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