Material Development of Polymer/Metal Paste for

Flip-Chip Attach Interconnection Technology

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Abstract

In this report on Polymer/Metal Composite (PMC) adhesive we describe two aspects of the material that are crucial to its applicability as a viable material for Flip Chip Attach (FCA) technology. We describe the shelf-life of the material at room temperature and its effect on the adhesion. Then we discuss the electrical and mechanical behavior of PMC bond under strain. It is demonstrated that the bond can be subjected to well over 40% strain with insignificant change in its electrical properties.

Introduction: Background and Motivation

The major challenges to develop a Flip Chip Attach (FCA) structure using a polymer/metal composite (PMC) adhesive falls into two categories:

- The PMC material and its precursor paste
- The process to obtain the FCA structure

The material challenges for obtaining a PMC material with appropriate conductivity, rheology and bonding characteristics have been discussed before (2-5). From the reliability measurements and the 4-point probe measurements (2,4) the bulk conductivity of PMC is better than solder and the contact resistance is comparable to solder. The rheological characterization of the material reported that the viscous behavior of the paste is shear thinning with a much larger decrease in viscosity with shear rate than other commercially available conductive adhesives (6). The elastic effect of the paste, inducing the "hole-effect" is reasonably low (6). Since, the FCA structure will...
be encapsulated with an epoxy material, the bond strength of PMC to the chip and pad metallurgy needs to be reasonable good. The mechanical strength of the structure will mainly be determined by the encapsulant, which is well above the the strength desired. The bonding studies, performed at Endicott (3) revealed that good adhesion can be obtained as the load, temperature and bonding time increases. Thus, the paste characterization and testing studies reveal that the PMC in its present form meets most of the requirements. As a next step, PMC and its paste needs to be tested as a viable material that can perform FCA using a manufacturing process that is cost-effective.

In this report we address two major aspects of the PMC PMC and its precursor paste properties that are critical to the manufacturability of PMC based FCA structure. These two issues are:

- Effect of post mixing prior to usage - Shelf life
- Stress behavior of the PMC bond - Bond compliance

**Paste Shelf Life**

One of the major advantages of a thermoplastic based paste is that it does not require low temperature storage. However owing to ~10 fold higher density of the Ag-filler relative to the polymer, there is some sedimentation of the particles in a quiescent mixture. By optimizing the Ag particle treatment, proper choice of the polymer binder and compounding process we have significantly reduced this sedimentation rate by improving the particle/polymer interaction. Nonetheless, the paste needs to be mixed manually for 30-60 seconds to homogenize the particles before dispensing operation. It is suspected that, such a low-shear mixing process will tend to entrap air that may lead to a porous bond. A porous bond can affect the properties in two distinct ways:

- They can reduce the ultimate bond strength of PMC by acting as nucleation site for cracks.
- During the under-filling process, the encapsulant can be incorporated in the PMC producing detrimental effects, such as swelling the bond.

We studied the effect of low-shear stirring on the behavior of the bond strength. A batch of freshly compounded paste is partitioned into three sub-batches. The bonds were made from the first batch on Pd/Ni coated 'L' described elsewhere (2). The second
batch was stirred for less than 10 mins. Subsequently, similar bonds as with batch-1 were assembled. The third batch was stirred for 40 mins. During the mixing, 25\% by volume of air was slowly injected during the process. Similar 'L' bonds were made from this batch immediately after the mixing operation. Fig. 1 compares typical stress-strain curve for PMC bond made from the three batches.

The bond strength, defined by the stress at break-point, for 'as received' and '10 min. stirred' paste are similar. The strain at break is also large (well above 5\% for solder bonds). However, a significant degradation of bond strength is observed for batch 3. This degradation in batch 3 proves that entrapped air will reduce the bond strength significantly and is therefore a cause of reliability-concern. Nevertheless, a stirring process up to 10 mins. does not affect the paste's bonding characteristics significantly. Since, stirring time required for a paste stored for a year is less than 5 mins., we can safely conclude that the paste has a shelf-life of at least 6 months at room temperature.

**Mechanical and Electrical Compliance of PMC**

One of the most important reliability concern is the mechanical and electrical integrity of the PMC bond under thermal cycling. The origin of the stress on the bond is due to the thermal mismatch that induces a shear stress, $\varepsilon$ given by,

$$\varepsilon \sim \frac{\Delta \alpha \Delta T}{h}. \quad (1)$$

Where, $\Delta \alpha$ is the difference between the in-plane, linear thermal expansion coefficient of the chip and the substrate, $\Delta T$ is the temperature difference, and $h$ is the height of the bond. We assume the chip is 1x1 cm. It is important to note that $\varepsilon$ will increase if the substrate is organic instead of ceramic. Furthermore, to lower the $\varepsilon$, the bond height should be increased to largest possible value. The $h$ is fixed by the size, shape and pitch of the features to be screened, the method for dispensing, and the bonding process. For a typical FCA geometry (1x1 cm chip, 75 $\mu$m bump height), $\varepsilon$ ranges from <2\% for typical glass ceramic substrate to as high as 18\% for an organic carrier, such as FR4. The temperature difference is assumed to be 100 $^\circ$C. Thus, the question is, can the PMC with stand 20\% strain?
Before we discuss the compliance behavior, we consider the effect of temperature on the PMC. Fig. 2 indicates that on the first heating the PMC behaves in a non-linear manner. However on subsequent cooling and heating cycles the resistivity follows a linear behavior typical of an ohmic material. Thus electrically PMC is ohmic under thermal cycling.

Next we consider the compliant behavior of PMC. Fig. 3 shows a typical stress-strain curve of a PMC bond with controlled thickness of ~100 µm. The bond was obtained at 220 °C. It is obvious form the behavior that the PMC is compliant well above 20% strain.

PMC is a composite material of silver particles dispersed in polymer matrix. It is reasonable to expect that under tensile load, the particles will tend to move farther apart that will increase the particle-to-particle and particle-contact pad contact resistance. To measure this behavior, we devised a special measurement to probe (the true four-point probe) contact resistance during tensile deformation. Fig. 4 shows a typical contact resistance versus strain behavior. Up to 50% strain, well above the required strain limit of 20%, the contact resistance is nominally constant (as seen from the % contact resistance change axis on the right hand side y-axis).

In most application, the chip is usually subjected to a thermal cycle: (a) during the bonding process, (b) as the appliance is turned on and off. Thus, the hysteresis behavior is also important. Fig. 5 shows the contact resistance characteristics as the paste is subjected to a loading-unloading cycle. We note that a cycle up to 60% strain, the change is insignificant. This indicates that PMC is resilient both electrically and mechanically, under large strains. Furthermore, the reversibility for strain >40% suggests that FCA to organic substrates should be feasible.

References

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**Figure Captions**

Fig. 1: Effect of low shear mixing on stress-strain behavior of PMC bond.

Fig. 2: Thermal characteristics of PMC bond

Fig. 3: Stress-strain behavior of PMC bond at room temperature and at a constant pull speed of 0.25 cm/min

Fig. 4: Change in contact resistance as a function of tensile strain for a PMC bond. The measurement performed at room temperature and incremental elongation of 0.01 mm.

Fig. 5: Hysteresis behavior of PMC bond contact resistance under condition identical to Fig. 4.
Effect of Air Entrapment on Adhesion

Stress (MPa)

IBM/Yorktown

% Strain

120

40 min/25% air

10 min/no air

as received

SARAF/Yorktown

Fig-1
Stress (MPa)

IBW/Yorktown

Mechanical Loading Behaviour of YKT-Paste BOND

Contact Resistance: 0.38 Ω·cm²
Bond Strength: 18.1 MPa
Mechanical Loading Behaviour of YKT–Paste Bond

C4 Bond Resistance: 4.8 mΩ
(C4 Diameter: 125 μm)

% Contact Resistance Change

0 0.60 0.64 0.68
Contact Resistance (μm–cm²)

0 40 80 120
IBM/Yorktown Saraf/Roblau

% Strain
IBM, ENDICOTT SECOND QUARTER, YEAR 2, REPORT
EXECUTIVE SUMMARY

IBM Endicott, Assembly Process Design has completed the second quarter of the second year of development activity on ARPA TRP No. DE-FC-04094AL98817 for High Performance, Low Cost Interconnections for Flip Chip Attach. This report covers the period 12/1/95 to 3/31/96. The scope of Endicott activity includes

1. Test Vehicle Design and Fabrication
2. Paste Deposition Process Development
3. Bonding Process Development
4. Mechanical Modeling
5. Reliability Testing

TEST VEHICLE DESIGN AND FABRICATION

Summary
Objective: Test vehicles are necessary to develop reliability databases and models as well as develop and verify process windows.

Accomplishments: The test cards that were incorrectly designed with the same stitch pattern as the test chips have been redesigned to be compatible with the test chips. New test cards have been received for both of the test chip pitches (0.005" feature/0.010" pitch and 0.010" feature/0.020" pitch). Current process development for paste deposition and chip bonding is using shorted chips that have blanket metal deposition of either gold, palladium or palladium nickel.

A single flip chip PCMCIA card that is manufactured in Toronto has been identified as a possible functional test vehicle candidate. The two major changes that will have to be made are

1. The chip site on the card will have to be plated with nickel and gold.
2. A special order of a wafer will be required to build up the correct chip pad metallurgy

PASTE DEPOSITION PROCESS DEVELOPMENT

Summary
Objective: PMSP (Polymer Metal Solvent Paste) material must be deposited either on a wafer, (typically five inches in diameter), an individual chip, or on a chip carrier. Preferred as a manufacturing process is deposition onto a wafer. Deposition onto a single chip is useful in the early development work so that other important work can proceed in parallel--bonding, reliability, encapsulation, vision for placement.

Accomplishments:

A 16 trial, 4 variable DOE was run on copper panels using the photobumping process. The hole diameters varied from 0.005" to 0.010" on 0.020" pitch. The variables included

1. Injection head downward force: 21, 28 lbs
2. Injection feed pressure: 6, 10 psi
3. Head Speed: 0.15, 0.25 inches/sec
4. Photoresist thickness: 0.003, 0.004 inches

Responses measured before stripping were
1. Surface flooding: presence of PMSP on the surface after blade wiping
2. Hole blooming: deposition of PMSP into a slight depression in the photoresist that surrounds the circumference of the aperture.
3. Hole filling: completeness

Responses after stripping photoresist were
1. Residual photoresist
2. Deposit survival: the removal of PMSP deposits by the mechanical action of the stripping process.
3. Deposit coplanarity
4. Deposit diameter
5. Deposit height

Although the head force was varied too frequently and experimental sensitivity was lost, these observations were made:
1. Surface flooding can be controlled by a balance between head force and injection pressure. Downward head force is needed to wipe the surface clean, however, injection pressure that is used to fill the apertures has an opposing force that lifts the head up.
2. Hole blooming was more severe on 0.004" photoresist. Sometimes this extra film deposit is removed as the supporting photoresist is stripped. The thin and fragile film breaks away. On other occasions the mechanical action of the stripper appears to lift up the film up and over onto the top surface of the deposit. The result is an annular ridge at the circumference. The annular ridge prevents complete area bonding over the deposit surface. One method used to reduce the effect of this ridge is to coin or flatten the PMC bumps. Experiments and analyses are in progress to gain understanding and eliminate blooming.
3. Hole filling improves with slower blade speed.
4. Deposit survival is 100% for deposits > 0.007" in diameter.

The initial approach was to deposit polymer metal solvent paste (PMSP) onto individual chips. However, working with a 6 x 6 array of individual chips has been difficult. Challenges include non coplanarity of the chip surfaces, tolerances between chips and the nest openings in the 6 x 6 array fixture and temporarily holding the chips in the fixture during photoresist strip. Consequently, PMSP deposition onto five inch wafers is preferred because the problems above are eliminated. Initial results with screening the 6 x 6 array of chip footprints onto a five inch wafer have been successful. Photoglass has been ordered for a fully personalized wafer for both the test chip designs. For now, deposition process development will utilize blanket five inch wafers. Experiments are planned to optimize the stripping process and to provide a flat or convex PMC surface rather than concave.
BONDING PROCESS DEVELOPMENT

Summary
Objective: The objective of the bonding process development effort is to identify the significant process variables that influence bond strength and fracture. Design-of-Experiments (DOE) is the method used to determine the effects of every variable. Process optimization will be accomplished by using the Response Surface Analysis (RSA) experimental procedure.

Accomplishments: Several test chips have been bonded and encapsulated to test cards. Card warpage has been controlled by heating the card to 125°C during bonding and heating the chip to about 240°C. Moire interferometry measurements for card warpage show that the warpage decreases 0.0005" as the card is heated from ambient to 180°C. Encapsulation is accomplished after cooling from the bond temperature at 225°C to 80°C. A transient thermal model has been developed and verified for card and chip heating during the bond cycle. A very small card volume heats up to the bond temperature of 225°C, while the rest of the card sets at 125°C. The heated volume is the size of the chip in area and about one half the card thickness for a 280P card. Ability to heat this minimal volume to accomplish bonding supports the concept of very rapid heating through the chip. The thermal model is being used to predict thermal profiles for different card cross-sections as well as various heating boundary conditions.

MECHANICAL MODELING

Summary
Objective: The objective of modeling is to validate and verify the design concept of interconnecting flip chips to organic carriers with (PMC) bumps. The disciplines of modeling and experimentation are used interactively and iteratively to predict design responses to stress. The results will be used to make and refine material, design and process changes in order to establish a reliability database that supports field use. Additionally, predictive and comparative models developed will be available to assess new and diverse application specific designs.

Accomplishments: UIC has provided a rapid heating bonder for the tensile/shear peg samples. Bonding temperatures are reached in 15 seconds. This ramp time will be decreased to < 10 seconds by improving the temperature feedback loop. Initial tensile results for butt samples has identified two areas of further refinement. The first is to ensure that the face of the 0.125" diameter pegs is square. Out-of-squareness has been measured across the diameter to be 0.0005" to 0.0008". The result is non uniformity in stress distribution within a sample bond line that is typically 0.005" thick and sample-to-sample variability. Improved squareness and thicker bond lines are being pursued. The second improvement to make is the fixture for the tensile pull. Minimizing errors from out-of-axis loading can be achieved by using a nine inch chain both above and below the sample. Short, heavy clamping fixtures are prone to out-of-axis loads that result in low pull strengths for the smaller tensile samples. Data for the out-of-square samples has shown variable results. Note Sample 1 that had a highly variable bond line thickness. Samples 2 and 3 are more favorable and show consistency with a more uniform bond line thickness. thickness.
<table>
<thead>
<tr>
<th>Sample</th>
<th>Modulus (psi)</th>
<th>Strength (psi)</th>
<th>% Elongation</th>
<th>Bondline (mils)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2625</td>
<td>333</td>
<td>14%</td>
<td>4-7.25</td>
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<tr>
<td>2</td>
<td>1892</td>
<td>812</td>
<td>47%</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>2173</td>
<td>767</td>
<td>38%</td>
<td>5.3</td>
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### RELIABILITY TESTING

#### Summary

**Objective:** The objective of reliability testing is to demonstrate that the PMC joints between a chip and card laminate can maintain stable contact resistance as a function of exposure to environmental stress. These stresses include thermal cycle (ATC), thermal age and temperature and humidity (T/H).

**Accomplishments:** Two sets of cards with one chip per card have been placed on stress test. Set one includes four cards that were made with photobumped chips (concave surface), and one card that was made by hand dispensing deposits (convex surface). Three cards, including the card with hand dispensed deposits, were placed on thermal cycle testing between 0 and 100°C. Two cards were placed on temperature and humidity test, 85°C/80% RH. Set two had photobumped chips bonded to cards that had hand deposits. These card deposits were intended to fill the concave surface of the chip photobumps. Seven cards were placed on test: three in thermal cycle, two in temperature/humidity, and two in temperature age, 125°C. Sixteen nets of two joints per net were electrically measured. Some prior experiments had resulted in defining an expected contact resistance $CR_{exp}$ value for good joints for most nets. A '?' is noted in the table where the $CR_{exp}$ had not yet been determined. For the two sets of cards, it was known that several joints had resistances higher than $CR_{exp}$, however, these were still stressed for information. The results are summarized in the two tables below. Note that the joints that have resistance increases that exceed the failure criteria, all show initial contact resistance $CR_0 > CR_{exp}$, suggesting an initial defect or low bond area. Joints that $CR_0 < CR_{exp}$ are stable with stress. These data demonstrate that a stable PMC interconnection between a chip and laminate can be achieved. There are several opportunities to further improve the contact resistance performance. The bond line has been measured around 0.002". Experience with solder flip chip attach to organic carriers supports a preferred solder height between 0.0025" and 0.003". By making 0.003" or 0.004" high bumps with 0.003" or 0.004" photoresist and controlling bond pressure, PMC bond heights equivalent to solder should be achievable. A second improvement can be realized by eliminating the concave surface.
<table>
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<tr>
<th>Test</th>
<th>Duration</th>
<th>ID #</th>
<th>Fails</th>
<th>CR₀</th>
<th>CRₑxₚ</th>
<th>CRₑ/CRₑxₚ</th>
</tr>
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<tbody>
<tr>
<td>0-100 C, ATC cycles</td>
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<td>1</td>
<td>1</td>
<td>1.94</td>
<td>?</td>
<td>?</td>
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<tr>
<td></td>
<td>220</td>
<td>3</td>
<td>3</td>
<td>1.73/1.71/1.37</td>
<td>0.90/0.85/0.73</td>
<td>1.9/2.0/1.9</td>
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<td>?</td>
<td>?</td>
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<td>?</td>
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<td>1</td>
<td>1.15</td>
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<td>?</td>
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<td>85°C/85% RH, hours</td>
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<td>1</td>
<td>1.60</td>
<td>0.72</td>
<td>2.2</td>
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<td>?</td>
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<td>?</td>
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<td>1.38/1.41/1.34</td>
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<td>1.5/1.5/2.4</td>
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<td></td>
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<td>0.85/0.68</td>
<td>1.9/4.3</td>
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<td></td>
<td>546</td>
<td>2</td>
<td>4</td>
<td>1.98/2.03/1.32</td>
<td>0.81/??/??</td>
<td>2.4/??/??</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.32/1.42</td>
<td>??/??/??</td>
<td>??/??/??</td>
</tr>
</tbody>
</table>

- S/S= 16 readings/card
- Card 5, hand dispense, 1 fail after 1000 cycles
- Card 4, photobumps, 0 fails after 546 hours T/H
<table>
<thead>
<tr>
<th>Test</th>
<th>Duration</th>
<th>ID #</th>
<th>Fails</th>
<th>$CR_0$</th>
<th>$CR_{exp}$</th>
<th>$CR_d/CR_{exp}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-100 C, ATC, cycles</td>
<td>100</td>
<td>1</td>
<td>4</td>
<td>1.04/2.03</td>
<td>0.49/?</td>
<td>2.1/?</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.81/0.85</td>
<td>0.50/?</td>
<td>1.6/?</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>3</td>
<td>2</td>
<td>1.83/1.84/1.16</td>
<td>0.4/??</td>
<td>4.6/?</td>
</tr>
<tr>
<td></td>
<td>116</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>295</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>400</td>
<td>3</td>
<td>1</td>
<td>1.90</td>
<td>0.49</td>
<td>3.9</td>
</tr>
<tr>
<td>85C/85% RH, hours</td>
<td>116</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>236</td>
<td>0</td>
<td></td>
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<tr>
<td></td>
<td>397</td>
<td>0</td>
<td></td>
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<td>125 C, hours</td>
<td>116</td>
<td>7</td>
<td>3</td>
<td>2.18/3.45/3.1</td>
<td>0.58/0.49/?</td>
<td>3.8/7.0/?</td>
</tr>
<tr>
<td></td>
<td>236</td>
<td>6</td>
<td>1</td>
<td>4.64</td>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>

- ATC: card 2 has 0 fails, 400 cycles
- T/H: card 4 and 5 have 0 fails, 397 hours
Overview and Summary

The work by Universal during the 1Q96 timeframe was concentrated in three general areas:

- Refinement of the initial laboratory testbed(s) to allow additional material property testing to be done by IBM.
- Expansion of the scope of the Cost Estimation System for Flip Chip Attach Alternatives activity being carried out with the help of personnel from Binghamton University.
- Initiation of the design for the second generation testbed to allow automatic alignment and bonding of ECA bumped Flip Chips on a variety of substrates.

Work in these areas is designed to progressively expand the knowledge base and allow determination of the performance, cost and functional requirements needed to provide a salable production equipment solution to the Electronics Assembly Industry for the use of the IBM developed Electrically Conductive Adhesive material.

The work of Universal is being paced to conform to the schedules generated by IBM and to control the rate of labor expenditure such that the knowledge gained feeds the next work activity planned. This approach keeps the project moving as rapidly as possible, while attempting to minimize "re-engineering" activity and "throw away" effort.

Laboratory Test Support and Testbed Refinement

Bonding tests with the initial laboratory testbed design showed that ECA material bulk property characterization could better be carried out through the use of custom designed cylindrical test coupons. The design of the thermode heating system provided to allow rapid temperature ramping (Figure 1.) was modified to allow the heating of IBM provided cylindrical test vehicles. These test vehicles are required to be precisely aligned such that the ends of the cylindrical test vehicles are registered longitudinally and radially prior to the bonding operation.
Cylindrical split bushings (Figure 2.) were designed and fabricated to provide the alignment and registration task, integrated to the laboratory testbed along with a means to support the ends of the test vehicles independently from the thermode ring heater used to provide the programmable temperature ramp required for the bonding experiments.

The modified testbed, with Universal Instruments support was used extensively by IBM personnel in the continuation of the ECA material property testing activities. An additional laboratory bench setup (Figure 3.) was provided to allow an initial assessment of the visual and reflectance properties of the ECA material bumps when viewed against a reflective Silicon background as would be found in production application of the technology. This early observation set leads us to believe, after observing the resulting bump image as a function of a variety of illumination techniques, that we will be able to achieve image qualities sufficient to adequately determine the location of the bump pattern on ECA bumped die. This information can then be used as input for the positioning of a placement / bonding tool.

Expansion of the Cost Modeling Activity

With the introduction of any nascent technology, an important step in the justification process should be devoted to analyzing its economic impacts against the cost factors of the current, viable state of technology. The purpose of this section is to delineate the effort being performed in the development of a computer-assisted cost estimation (CACE) system for ECA-based flip chip technology.

To this end, the CACE is being created for comparing IBM’s ECA-based attach method versus a variety of solder-based methods (namely, solder on chip (SOC), solder plating (SP), solder jetting (SJ)). In a previous meeting (November 1995, IBM’s Yorktown Heights facility), the Binghamton University team working on this effort presented a rough, first-pass cost comparison of ECA vs. SP. That first-pass analysis was based on some assumptions, some of those being the following: wafer processing costs are the same, PCB assembly steps only differed at the board population (e.g., bonding (ECA) vs. placing (SP)) step, and PCB assembly material costs were the same. Based upon these assumptions, it does appear that, when comparing ECA vs. SP alone, ECA is a viable competitor. This is mainly due to the fact that SP board processing is a time and labor intensive operation which severely impacts costs. On the other hand, ECA board processing is, in comparison, minimal with regards to cost impacts. The question of course arises of How proper are these assumptions? While the material costs at the PCB assembly stage are probably a “wash”, the other assumptions are rather limiting.

Since that analysis, the CACE has been undergoing continuous improvement. Specifically, efforts are being carried out to take into account cost factors that
were previously not included. Furthermore, as mentioned above, ECA is being compared to other solder-based steps in addition to the SP method. The major thrust of the cost modeling is to encompass various components of the overall process. Previously, the PCB assembly stage practically received the only attention (with some being given to SP board processing cost estimates). Now, we realize that in order to fully understand the entire system, three cost components need to be compared. These are the wafer processing stage, the board preparation (processing) stage, and the PCB assembly stage.

As depicted above, these stages are interdependent (for all flip chip attach methods) and are all cost-adders. For example, the PCB assembly stage may be comparatively inexpensive (in terms of time or throughput considerations and equipment sets) for one flip chip attach method, but the wafer and/or board processing stages may be comparatively expensive in regards to another flip chip attach method.

The CACE is created for use on PC-based machines and is written as a Microsoft Excel™ file running under Microsoft Windows™ operating system. Thus, the CACE is ensured for ease of use and portability. The CACE is product driven; i.e., the user need input information related to a specific product and then the cost estimates for the various methods are generated. The types of inputs requested of the user, among others, are the following:

- Number of flip chip components per product;
- Number of non flip chip components per product;
- Expected annual product demand (volume);
- Cycle time estimates (bonding times, placing times, etc.);
- Production time information (shifts per day, days per week, etc.);
- Estimates of material usage (solder, tin, etc.) in the various processes.

The CACE will then take these inputs and performs a variety of calculations to estimate the cost factors for the three different stages, the major factors being the following:

- Equipment sets necessary to meet volume;
Corresponding equipment costs required to meet volume;
Floor space usage (to estimate utility costs);
Material costs required to meet volume.

The individual equipment costs and the material costs (for the various processing stages) are incorporated as default values in the system. As it now stands, the CACE system is near completion with the remaining steps needed to be filled are some equipment costs (in board preparation and wafer processing; PCB assembly equipment costs are complete) and some material costs. Otherwise, once these equipment and material costs are located, the current version will be complete.

Second Generation Testbed Design

As the material property testing continues, the resulting information has been used to determine and refine the necessary functional attributes of the second generation testbed. As originally conceived in the program, the second generation testbed will be used to actually carry out the ECA bonding process under fully computer controllable process sequences, allowing direct extrapolation of the test results to anticipated production machine performance. In addition, the automated testbed will allow continued refinement of the bonding process parameters so as to optimize the production operation sequence to achieve the objectives of a cost competitive, robust assembly process.

The design of the second generation testbed is currently under way, and those elements already identified as being necessary are being procured as shown below:

<table>
<thead>
<tr>
<th>Element</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical Bench Frame Structure</td>
<td>On hand</td>
</tr>
<tr>
<td>Electrical Cabinet</td>
<td>Design not started</td>
</tr>
<tr>
<td>Head Support and Overbeam Structure</td>
<td>In fabrication</td>
</tr>
<tr>
<td>One Micron X-Y Positioning System</td>
<td>On hand</td>
</tr>
<tr>
<td>with 12 inch X 12 inch Travel</td>
<td></td>
</tr>
<tr>
<td>Positioning System and Head Controller</td>
<td>On hand</td>
</tr>
<tr>
<td>Upward Looking Camera Assembly</td>
<td>On hand</td>
</tr>
<tr>
<td>Upward Illumination System</td>
<td>On hand</td>
</tr>
<tr>
<td>Downward Looking Camera (DLC)</td>
<td>On hand</td>
</tr>
<tr>
<td>Y - Axis Positioning Slide for DLC</td>
<td>On hand</td>
</tr>
<tr>
<td>Board Support Thermode</td>
<td>In design</td>
</tr>
<tr>
<td>Board Support Actuator</td>
<td>In design</td>
</tr>
<tr>
<td>Board Holder</td>
<td>In design</td>
</tr>
<tr>
<td>Bonding Thermode</td>
<td>Mock up completed,</td>
</tr>
<tr>
<td></td>
<td>final design underway</td>
</tr>
<tr>
<td>System Software</td>
<td>In design</td>
</tr>
<tr>
<td>Placement Head</td>
<td>In design</td>
</tr>
</tbody>
</table>
- Vision Processor Engine On hand
- Pneumatics 80% on hand

Activity is expected to continue the design and procurement function on the second generation testbed, assembling it, performing the debug and beginning to run automated bonding tests in the next quarter.
FIGURE 1: Thermode Heating System
FIGURE 2: Cylindrical Split Bushing
FIGURE 3: Optical Bench Illumination Set-up
FIGURE 4: Bonding Thermode Mock Up