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Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements

Annual Subcontract Report 1 January 1995 – 31 December 1995

John Wohlgemuth
*Solarex, A Business Unit of
Amoco/Enron Solar
Frederick, Maryland*

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

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NREL technical monitor: R.L. Mitchell

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PREFACE

This Annual Technical Progress Report covers the work performed by Solarex for the period January 1, 1995 to December 31, 1995 under DOE/NREL Subcontract # ZAI-4-11294-01 entitled "Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements". This is the second Annual Technical Report for this subcontract. The subcontract is scheduled to run from December 8, 1993 to December 7, 1996.

The following personnel at Solarex have contributed to the technical efforts covered in this report.

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In addition, Solarex has been supported by the staff at the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI). ARRI staff working on the subcontract include:

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SUMMARY

The objective of this three-year program is to advance Solarex's cast polycrystalline silicon manufacturing technology, reduce module production cost, increase module performance and expand Solarex's commercial production capacities. Two specific objectives of this program are to reduce the manufacturing cost for polycrystalline silicon PV modules to less than \$1.20/watt and to increase the manufacturing capacity by a factor of three. To achieve these objectives, Solarex is working in the following technical areas:

CASTING

The goal of the casting task is to develop the ability to cast ingots that yield four bricks with a cross-section of 15 cm by 15 cm with at least equivalent material quality as now achieved for 11.4 cm by 11.4 cm bricks. This represents a 73% increase in the useable silicon obtained from each casting.

WIRE SAWS

The goal of the wire saw task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μ m centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

CELL PROCESS

The goal of the cell task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. The developed process must be compatible with automated manufacturing at large volumes.

MODULE ASSEMBLY

The goal of the module assembly task is to modify Solarex's present module assembly system to increase throughput by 100% and decrease the labor requirement by 50%. The Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI) is to work with Solarex to model the present automated module assembly system and to recommend modifications to increase throughput and reduce labor.

FRAMELESS MODULE DEVELOPMENT

The goal of the frameless module task is to develop and qualify a frameless module design incorporating a lower cost back sheet material (less than \$0.05/square foot) and user friendly, low cost electrical termination (less than \$1.00/module). Since PVMaT is designed for large systems, modules can be designed to mount directly onto the support structure without integral frames.

AUTOMATED CELL HANDLING

The goal of the automated cell handling task is to develop automated handling equipment for 200 μm thick 15 cm by 15 cm polycrystalline silicon wafers and cells with a high yield (less than 0.1% breakage per process handling step) at a throughput rate of at least 12 cells or wafers per minute.

ACCOMPLISHMENTS

Accomplishments during the reporting period include:

- Cast larger ingots with 4 - 15 cm by 15 cm bricks with equivalent material quality.
- Cast larger ingots with 9 - 11.4 cm by 11.4 cm bricks with equivalent material quality.
- Operated the wire saw in a production mode, producing more than 1,000,000 wafers at a higher yield than achieved on the ID saws.
- Reduced the cost of wire saw consumables (grit and oil), spare parts (pulleys) and waste disposal.
- Developed and demonstrated a prototype machine that can load a cassette from a stack of wet wafers.
- Completed two pilot runs of the cost effective Al paste back surface field process, verifying a 5% increase in cell efficiency and demonstrating the ability to process and handle the BSF paste cells.
- Environmental qualification of modules made using the cost effective Al paste BSF process.
- Fabrication of the first 15.2 cm by 15.2 cm polycrystalline silicon solar cells.
- Fabrication of the first modules using 15.2 cm by 15.2 cm solar cells.
- Demonstrated that cell efficiency increases with decreasing wafer thickness for the Al paste BSF cells.
- Developed a process with all printed contacts that requires only one high temperature contact firing step after emitter diffusion.
- Completed modifications to the module assembly area to increase capacity by a factor of two.
- Completed qualification testing of modules built using Spire's automated tabbing and stringing machine developed under their PVMaT Program.
- Selected, tested and qualified a low cost (less than \$1.00 per module) electrical termination system.
- Qualified the structure and adhesive tape system for mounting frameless modules and used the adhesive tape system to build a 100 kW system at SMUD.
- ARRI completed a study of the fracture properties of cast polycrystalline silicon wafers and provided the information necessary to calculate the maximum stresses allowable during wafer handling.

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1.0 INTRODUCTION

The goal of Solarex's Crystalline PVMaT program is to improve the present Polycrystalline Silicon manufacturing facility to reduce cost, improve efficiency and increase production capacity. Key components of the program are:

- Casting of larger ingots.
- Use of wire saws to cut thinner, larger size wafers with less kerf loss.
- Transfer of higher efficiency cell processes to manufacturing.
- Increased automation in module assembly.
- High reliability mounting techniques for frameless modules.
- Automated handling of large, thin wafers.

The results of these efforts will be to reduce the module cost per watt to less than \$1.20/watt, to increase the production capacity of Solarex's Frederick plant by a factor of 3 and to provide larger, higher efficiency modules that reduce the customer's balance of systems cost. All of this is to be achieved without sacrificing the high reliability already achieved with the crystalline modules in use today.

The rationale behind the Solarex program is to use as much as possible of the present equipment and processes, making improvements that lead to larger sizes, better utilization of materials, higher efficiencies and reduced labor requirements. In this way the maximum increase in capacity and reduction in cost can be achieved with justifiable capital investments in equipment modifications. Specific areas to be addressed in the program are discussed briefly below.

Today Solarex casting stations are used to produce ingots from which 4 bricks, each 11.4 cm by 11.4 cm in cross section are cut. The stations themselves are physically capable of holding an ingot that would be large enough to cut 4 bricks 15 cm by 15 cm in cross-section or 9 bricks 11.4 cm by 11.4 cm. Task 6 involved making the modifications in equipment and process necessary to cast larger ingots. This effort will lead to an increase in the production capacity of Solarex's casting stations and reduce the labor content.

Wire saws can be used to cut thinner wafers with less kerf, than is possible on the Internal Diameter (ID) saws. The program goal is to reduce the center to center cut distance from 600 microns on the ID saw to 400 microns on the wire saw. This will result in a 50% increase in solar cell and module output from the same silicon feedstock purchased and cast. That is, with the same amount of feedstock material and the same casting capacity Solarex will be able to increase its output of PV modules by 50% (on top of the increase achieved by casting larger ingots). In addition, wire saws can also be utilized to cut larger wafers, something ID saws can not do.

Finally, wire saws have a much higher production capacity than ID saws. One wire is producing as many wafers as 16 ID saws. To increase capacity with wire saws requires a much smaller capital investment than would be required to achieve the same increase with ID saws. The major issue with wire saws was the ability to reduce the variable cost to cut a wafer. Efforts to reduce the cost of grit, oil, wire, spare parts and labor make up the major part of Task 7.

In this program, Solarex is working on the transfer of high efficiency cell technologies from the laboratory to production. Issues involved in the successful transfer include process cost, ability to

scale to large volume, adaptability to automation and the degree to which each step integrates into the overall cell process sequence. Therefore, it is necessary as a part of this program to evaluate each component of the sequence that has proven effective at increasing cell efficiency to determine the most cost effective cell process sequence. Specific areas under investigation during the second year include:

- Optical Coupling
 - mechanical texturing
- Passivation/Gettering
 - hydrogen passivation
 - phosphorous gettering
- Back Surface Field (BSF) Formation
 - Al paste BSF

The goal of the Task 8 cell effort is to increase average cell efficiency (as obtained from a production line, not just from the laboratory) to 15% as measured at STC (Standard Test Conditions - 1000 W/m², AM1.5, 25° C). This must be achieved with a process sequence that lowers the module \$/Watt manufacturing cost.

Solarex had a first generation automation system in use at the Frederick facility for tabbing, matrixing and lay-up of the PV modules. During Task 4 the system was evaluated to determine how it could be modified to increase production throughput, yield and process control and to minimize production labor and cost. To assist with this effort, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington is serving as a subcontractor. ARRI has assisted Solarex in analysis, modeling and development of handling concepts to improve the operation of the module assembly area. In Task 9 the assembly area was modified as modeled.

Solarex modules use low iron tempered glass as a superstrate and Ethylene Vinyl Acetate (EVA) as the encapsulation system. No change is proposed in this encapsulation system to maintain the module reliability. However, a reduction in the cost of the backsheet was achieved during Task 5 without negatively impacting the module reliability.

Today most PV modules are sold with a frame to provide means for mounting the module and a junction box for electrical connection. This frame is the largest single contributor to module cost. In large systems, the support provided by the system structure is adequate making the module frame redundant. Eliminating this frame can reduce the module selling price by more than \$0.50/Watt. During Task 10, testing of a candidate frameless module mounting schemes was completed and this mounting technique was utilized in a large scale PV system at SMUD.

Similarly, the junction box adds appreciable cost to the module, while requiring additional labor for system assembly. In Task 10, a simpler electrical termination scheme costing less than \$1.00 per module was tested and qualified for use.

Task 5 also included the design of a 122 watt module using 36- 15 cm by 15 cm solar cells. Tasks 10 and 15 include qualification of the design through accelerated environmental tests

(CEC-503, IEC-1215, UL 1703, and IEEE-1262) and design of the automated equipment necessary to finish the module.

An important issue for many crystalline silicon PV manufacturers is the ability to handle thinner and larger wafers through the production line. Task 11 and 17 are addressing this issue. Once again, Solarex is supported in this effort by ARRI, whose background and experience is ideally matched to the task of developing handling methods for parts such as the large thin wafers to be used in this program. ARRI has performed detailed analysis and modeling of the requirements for thin wafer handling. Prototype stations have been built to evaluate various approaches to handling such wafers. Once the concepts have been verified at ARRI, Solarex will design and have built a production unit to verify its capability.

The results of this program will be the modification of today's polycrystalline production facility to:

- Increase production capacity by a factor of three
- Reduce the "profitable" selling price from over \$4.00 per peak watt to less than \$2.00 per peak watt.

Solarex plans to continue an aggressive market development program that would support the increased capacity obtained as a result of this program.

2.0 BASELINE PROCESS AND PRODUCTS

Solarex's Crystalline Silicon Technology is based on use of cast polycrystalline silicon wafers. The process flow used at the beginning of this PVMaT program is shown in Table 1. The primary product was a module with 36 solar cells each 11.4 cm x 11.4 cm, that produces 60 or 64 Watts under Standard Test Conditions (STC).

Table 1
Baseline Cast Polycrystalline Si Process Sequence

Casting

ID Wafering

Cell Process
(Thick Film Print)

Module Assembly

Lamination

Finishing

The various segments of Solarex's module manufacturing process as practiced at the beginning of this PVMaT program are described below.

Casting

Solarex has developed and patented a directional solidification casting process specifically designed for photovoltaics¹. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semicrystalline silicon ingot. In house manufacture of low cost, high purity ceramics is a key to the low cost fabrication of Solarex semicrystalline wafers².

The casting process is performed in Solarex designed casting stations. The casting operation is computer controlled. There are no moving parts (except for the loading and unloading) so the growth process proceeds with virtually no operator intervention.

Wafering

Wafering was done with Internal Diameter (ID) saws. These are the same saws that are used in the semiconductor industry to wafer single crystal CZ ingots. Solarex has many years of experience with these ID saws, resulting in low labor and process costs. This is a mature technology with little opportunity for significant increases in productivity or reduction in kerf loss.

Cell Process

The cell process sequence is based on the use of Thick Film Paste (TFP) metallization, where a commercially available screen printed silver paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps including diffusion, firing of the front print paste and Chemical Vapor Deposition (CVD) of a TiO_2 antireflective (AR) coating are all performed in belt furnaces.

Polycrystalline cells processed through this line have an average cell efficiency of 12.5 to 13% at STC. There are many modifications to this process sequence that can increase cell efficiencies. However, many of these modifications would actually increase the total dollar per watt module cost rather than decrease it. Detailed cost analyses indicate what changes in cell processing can lead to both higher cell efficiencies and lower dollar per watt module cost.^{3,4} Implementation of these changes require laboratory verification of the candidate process sequences as well as improvement in the accuracy of the input cost data.

Module Assembly

The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. Each tab is soldered in 4 places for reliability and redundancy. Solarex uses automated machines to perform the tabbing. Tabbed cells are then laid up into a 36 cell matrix by a robot. The tabs are then soldered to the backs of the solar cells using automated equipment. Each tab has 2 back solder joints.

Module Lamination

The module construction consisted of a low iron, tempered glass superstrate, EVA encapsulant and a 3 part Polyethylene-Mylar-Tedlar backsheet. A single sheet layer of Tedlar replaced the 3 part backsheet during the first year of the program. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

Finishing

Most modules are sold with a frame to protect the edges and provide a means of mounting. Solarex uses an extruded aluminum frame that is attached both with a butyl rubber adhesive between frame and glass as well as with 2 screws in each corner of the frame. The framing process is performed by an automatic, robotic framing system.

Most modules are also sold with a junction box to protect the output wiring and provide the terminals for electrically connecting the module to the balance of the system. The area where the lead wires are attached to the module is potted to protect the laminate from moisture incursion. The junction box is then attached to the module with adhesive to seal it to the back of the laminate.

3.0 PVMaT PROGRAM EFFORTS

The following sections detail the progress made during 1995.

3.1 TASK 6 - POLYCRYSTALLINE SILICON CASTING IMPROVEMENTS

The goal of the casting task is to develop the ability to cast ingots that yield four - 15 cm by 15 cm bricks with at least equivalent material quality as now achieved when casting four - 11.4 cm by 11.4 cm bricks. During the first year of the program, Solarex designed and fabricated new larger ceramic pieces, designed and implemented modifications to a casting station and designed and implemented modifications to the sizing saws in order to be able to cast and size larger ingots.

During this reporting period efforts turned to casting full size ingots to yield 4 x 15 cm by 15 cm bricks. The first several large ingots had well-behaved runs, but had cracks extending upward from the bottom. An 11.4 cm by 11.4 cm brick was cut from one of these ingots, and then wafered and processed into cells. The cell efficiency from this brick was significantly lower than normal, with the average cell efficiency for this brick being approximately 90% of a standard production brick. A number of modifications to the insulation package and to the casting program were attempted, but none was able to eliminate the bottom cracking.

Analysis of the crystal growth and modeling of the casting process indicated that a larger separation between the bottom heater enclosure and the lower can was required. This change was made and the insulation configuration and process program optimized on standard sized ingots. We verified that this configuration could produce equivalent material by casting and processing 9 standard size ingots. There was no statistical difference in yield or efficiency between these 9 ingots and the overall production line average during that time period.

Using this configuration full size ingots for 4 x 15 cm by 15 cm bricks were cast. The new configuration and program eliminated the cracking. Sample 15 cm by 15 cm bricks and all of the wafers cut from one of these bricks on the wire saw have been delivered to NREL. Sample 11.4 cm by 11.4 cm bricks were cut out of the larger ingots and processed to make standard solar cells for comparison of material quality. Cell efficiencies were equivalent to similar resistivity material cut from standard size ingots.

Most of Solarex's products are still based on the use of 11.4 cm by 11.4 cm solar cells, so an effort was undertaken to develop casting of ingots large enough to produce 9 x 11.4 cm by 11.4 cm bricks. Such an ingot requires approximately 20% more silicon than the PVMaT ingot. The initial efforts to cast these "mongo" ingots required changes in the insulation and receiver, but utilized the same pour crucible as the PVMaT ingot. We were able to load the added charge of silicon feedstock into the PVMaT crucible and successfully pour and freeze out the larger mongo ingots.

During the process development cell results and a microwave lifetime measurement system were utilized to evaluate the material quality. During process development, results from an edge brick showed a low lifetime at the bottom of the ingot and on the outside edge. Cells results were consistent with this picture with an average cell efficiency of 11.87%, considerably below the results for standard size ingots. The center brick had no edge drop-off in lifetime and had an

average cell efficiency of 12.52%, much closer to the efficiency of standard size ingots. After further process optimization the overall lifetime measurements increased with much less reduction at the edges of the ingots. Optimization of the casting process for larger ingots continues.

3.2 TASK 7 - WIRE SAW IMPROVEMENTS

The goal of this task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μ m centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

3.2.1 Wire Saw Operations

The first step in this effort was to select and procure a wire saw. Solarex selected and purchased an HCT wire saw⁴. The HCT wire saw has been operational since July, 1994. During the first year of the program the saw was used to successfully demonstrate the ability to cut 11.4 cm by 11.4 cm, 11.4 cm by 15.2 cm and 15 cm by 15 cm wafers on 500 μ m and 400 μ m centers.

The major efforts during the second year were to:

- gain experience operating the saw in a production mode.
- reduce the cost of consumables, spare parts and waste disposal.
- develop improved methods for demounting and cleaning the wafers after they are cut on the wire saw.

Production operators were trained on the saw and then used to operate the saw as a production operation on the off-shifts, while we perform experiments to improve the process and reduce costs during the day shift. For 1995 on one wire saw we processed in excess of 1,000,000 wafers at higher yield than achieved on the ID saws. Much of the yield loss comes from aborts, where all of the bricks being cut are completely lost. One major problem during this period has been the lack of a source for a quick turn-around on regrooving of wire guides. Occasionally an abort will ruin one or more of the wire guides. We have then been forced to run for longer periods than advisable with a worn wire guide, while waiting for the damaged guides to be regrooved.

Cost saving efforts during the reporting period include:

1. Qualified a new oil that costs 32% less than the original oil. This change alone reduces the wafer cost by several cents.
2. Identified and qualified a new vendor of pulleys. The new pulley cost about one-third of what the saw vendor charged for the original pulleys.
3. Identified and qualified grit from several vendors. Negotiated a long term contract to save \$0.25 per pound of grit.
4. Found someone who can recycle our waste slurry and in doing so reduced our cost to dispose of the waste by 90%.

3.2.2 Demounting and Cleaning

After wafers have been cut on the wire saw they must be removed from the hold down plate, placed in cassettes and cleaned. Today this process is done manually. An automated process is necessary to reduce cost and increase yield especially as the volume of wire saw wafers increases and the thickness of the wafers decreases. As a first step to better understand what is involved in removing wet wafers from a stack, ARRI performed a series of tests to evaluate the difficulty of separating wafers. The results of these tests were reported in the Third Semiannual Report for this contract.⁵

A set of experiments was then performed to gain a quantitative understanding of the forces involved in wafer separation under both dry and wet conditions. Six sets of test conditions were evaluated as described below.

Test Condition 1: Dynamic friction coefficient, dry wafer

With the bottom wafer fixed, a 200-gram weight was placed on the top wafer. A string and pulley arrangement with a cup at the free end imparts a horizontal force on the top wafer. The cup was slowly filled with water until the top wafer began to slide at a constant rate; cup and water are then weighed. The set-up for measuring the dynamic friction coefficient is shown in Figure 1.

Figure 1
Test Set-up for Measuring the Dynamic Friction Coefficient

Test Condition 2: Dynamic friction coefficient, semi-wet wafer

This test was performed in the same manner as test #1 except for the addition of a small amount of tap water to the center of the bottom wafer.

Test Condition 3: Dynamic friction coefficient, wet wafer

This test was performed in the exact same manner as test #2, but with the addition of a much larger amount of tap water to the bottom wafer. In this case so much water was added that some

squeezed out from between the wafers when the weight was added. This provides the maximum water layer thickness that the wafers can maintain under the given load.

Test Condition 4: Normal separation force, dry wafer

The bottom wafer was fixed and the second wafer was laid on top. A string and pulley arrangement with a cup at the free end imparted a vertical (normal) separating force on the top wafer. The cup was slowly filled with water until the wafers become completely separated. The set-up for measuring the normal separation force is shown in Figure 2.

Figure 2
Test Set-up for Measuring the Normal Separation Force

Test Condition 5: Normal separation force, semi-wet wafer

This test was performed in the exact same manner as test #4, with the addition of a small amount of tap water to the center of the bottom wafer. Because large forces at the interface between the wafers develop when water is present, a larger capacity container was required to provide the upward pull on the top wafer.

Test Condition 6: Normal separation force, wet wafer

This test was performed in the exact same manner as test #5, but with the addition of a much larger amount of water to the bottom wafer.

The experimental data and computed values for the dynamic friction coefficient tests are given in Table 2. Coefficients are calculated by the ratio of sliding pull weight to top assembly weight. All weights (masses) are in grams. The experimental data for the normal separation force tests is given in Table 3. All weights (masses) are in grams.

Under dry conditions, the sliding friction between wafers is easily overcome without breakage. Similarly, for dry wafers normal separation forces amount to little more than the weight of the wafer itself, indicating that no significant binding forces develop at the interface.

Table 2
Dynamic Friction Coefficients

#	Top asm weight	<u>Test 1</u> Dry sliding weight	<u>Test 2</u> Semi-wet sliding weight	<u>Test 3</u> Wet sliding weight	Dry sliding frict. coefficient	Semi-wet sliding frict. coefficient	Wet sliding frict. coefficient
1	202	111	2149	219	0.55	10.6	1.1
2	203	104	2053	208	0.51	10.1	1.0
3	204	102	2041	171	0.50	10.0	0.8
4	204	118	2589	105	0.58	12.7	0.6
5	206	114	2257	159	0.55	11.0	0.8
6	207	126	1976	208	0.61	9.5	1.0
avg	-	-	-	-	0.55	10.7	0.9

Table 3
Normal Separation Force

#	<u>Test 4</u> Dry separation weight	<u>Test 5</u> Semi-wet separation weight	<u>Test 6</u> Wet separation weight
1	7	2274	>5700
2	3	2018	>5700
3	12	2381	5101
4	16	1907	>5700
5	7	1864	>5700
6	6	1369	5573
avg	9	1969	>5700

The presence of water between the wafers, however, increases dramatically the sliding as well as normal forces required for separation. In the sliding tests, the separation force is greatest under semi-wet conditions. When the water layer is thick, the force required to separate the wafers is much lower. Normal separation pull forces, however, are strongest under a fully wet condition. The pull forces required to separate semi-wet and wet wafers are well within the breakage-causing range, as happened with several of the samples tested.

These results indicate that it would be best to dry the wafers before destacking. However, the present cleaning solvent dries slowly. When we began evaluating the use of a solvent that would dry more quickly, we realized that evaporating slowly is an important feature of the solvent, since it raises the flash point and minimizes the release of organic vapors into the air. Therefore, use of a more rapidly drying cleaning solvent is not recommended.

ARRI then proceeded to develop a number of concepts for equipment to destack wafers into cassettes that could be utilized on wet or semi-wet wafers. Two of the ideas were selected, prototype equipment was built and tested.

Pneumatic Wafer Ejection

In this design the stack of wafers lies vertically. A sheet of air blows across the top of the wafers, creating a vacuum above the top wafer. The vacuum causes the wafer to lift off the stack. The stream then pushes the wafer down a curved chute into a cassette. The cassette is then indexed to accept the next wafer. This concept has the following advantages;

- There are no mechanical parts touching the wafers, preventing contamination or mechanical damage to the wafers.
- The motion is smooth and quick easily meeting the throughput requirements.

Preliminary tests were successful in separating the wafers. The vacuum force generated by the air stream was sufficient to lift the wafers. Control of the process was required to insure that only one wafer was lifted during each cycle. In order for the second wafer to remain in the stack, the top wafer can not drag the second wafer off of the stack and the vacuum force must not be strong enough to pick up two wafers at the same time. Therefore, the air pressure must be maintained in a range where one wafer is picked up and ejected, but the second wafer is not moved. The system parameters can be controlled by the input air pressure as well as by the spacing of the air channels. Because the friction force between wafers is so important in this process, it does not work well with wet wafers. Therefore it is not a candidate for the wafer demounting-cleaning process. However, because it is a simple process with high throughput, we have continued to evaluate the pneumatic ejection process as a potential candidate for handling wafers and cells in the cell line.

Wafer Pull-Down

In this design the stack of wafers lies horizontally. A roller presses against the first wafer in the stack, pulling it downward through a slot into a cassette. The cassette is then index to accept the next wafer. This concept has the following advantages:

- It requires a single indexing slide rather than say a robotic pick and place.
- It requires relatively simple equipment.
- It is a rapid process with a low cycle time.
- It is highly energy efficient since it uses gravity to place the wafer in the cassette.

A prototype wafer pull down system has been built and tested at ARRI. During the demounting process, the front of the wafer is rubbed some by the rubber rings on the roller, while the back of the wafer registers two light streaks from sliding against the bottom support pins as the wafer is pushed down. Though there are ways to minimize these effects using different materials and roller speeds, they will always be present to some extent and therefore preclude the use of this demounting method in certain applications. However, this is no problem for cassetting after demounting, since the wafers will be etched afterward.

With the 250 micron wafers tested there has not been a single incident of wafer breakage due to the forces imparted by the rollers or the bottom support pins; in fact, wafers have survived hundreds of demount passes without breakage.

A series of tests were run to assess the reliability of this demounting method over extended operation. A stack of some 35 wafers was repeatedly loaded and demounted over a total of more than 2,000 cycles. There were only 15 cases in which the system did not remove a single wafer correctly. The most likely incident is the simultaneous delivery of two wafers (affectionately known as "twins"), which occurred 10 times. This is something that can happen even during manual demounting, and is associated with instances where the binding forces between two wafers become unusually strong; the machine cannot detect this condition on its own (other than by measuring the wafer thickness). Every one of these instances was noted by the operator. Far less often (4 times) is the case where a wafer cannot be demounted despite repeated stack advance attempts. This may correspond to several (three or four) wafers strongly binding together to the point where the roller friction cannot overcome the wafer-to-wafer friction. This condition can be easily remedied by the operator, who would simply remove the offending stack and either attempt to demount it manually or return it to the cleaning bath for later processing.

After verifying that the wafer pull down method worked with dry wafers, ARRI modified the equipment so that water could be pumped over the wafers while it was operating. The system works fine with wet wafers. The system successfully destacked wafers into the cassette for up to one hour after the water flow was turned off. The wafer pull down approach appears to be an encouraging technique for placing the wire saw wafers in cassettes after demounting.

3.3 TASK 8 - HIGH EFFICIENCY CELL DEVELOPMENT

The goal of this task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. While a number of approaches to achieving high efficiency have been reported, many of these utilize processes and material that are not likely to be cost effective when applied to cast polycrystalline silicon in a manufacturing environment. The key to achieving the goal of this task is to select modifications to the present process that increase efficiency while lowering the cost per watt. That is, the increased cost of the process is less than the value of the increased power produced by the improvement.⁶ During the period cover by this report, the major cell task efforts were in the areas of back surface fields (BSF), phosphorous gettering, mechanical texturing and an integrated cell process. Each of these areas is discussed below:

3.3.1 Back Surface Field Formation

In the first Annual Report⁷ of this program, we reported that an aluminum paste back surface field (BSF) could be used to cost effectively increase cell efficiency by approximately 5%. During the second year of the program efforts included manufacturing trials, environmental qualification of cells made with the Al paste in a module package, evaluation of the impact of cell thickness and development of an all screen printed process.

Two BSF manufacturing trials were completed. In excess of 25,000 BSF cells were fabricated with all processes except the back paste print and fire performed in production using standard processes, equipment and production personnel. Cell efficiencies were compared to cells without back surface field made during the same time period. During the two pilot runs the average cell efficiency increased by 5.4% and 5.3% respectively. The BSF process shifted the entire distribution to higher efficiencies as seen in Figure 3. The X bin represents the highest

efficiency with G bin the lowest. The largest portion of BSF cells are in the highest efficiency bin, while less than 1% of the standard process cells made this bin. The efficiency enhancement translated from cells to modules, demonstrating an average 5% increase in output power.

Figure 3

Distribution Comparison, BSF Pilot vs. Representative Standard
Production [November /95]

Modules made during the first pilot run were subjected to environmental qualification testing per IEC-1215 and IEEE-1262 with the addition of a second 200 thermal cycles as required for Solarex's 20 year warranty. The BSF modules successfully completed the testing with all power losses well below the maximum allowable by IEC-1215 with no measurable differences between the BSF and standard cell modules subjected to qualification at the same time.

The overall PVMaT plan calls for the use of thinner wafers to increase the yield of watts produced per purchased kilogram of silicon. Part of this effort then is to evaluate the effect of using thinner wafers on cell performance. An experiment conducted to study the effect of cell thickness on cell efficiency. The experiment was initially performed using Solarex's standard process with no BSF. The results of this experiment are shown in Figure 4. These cells are less efficient as they get thinner. With this technology we would expect to lose approximately one half a percentage point in efficiency when reducing the thickness from 290 μm to 190 μm .

A similar experiment was then conducted using BSF cells. The results are shown in Figure 5. In this case the thinner BSF cells are more efficient. With the BSF process we can expect the efficiency to increase by approximately one third of a percentage point when reducing the thickness from 290 μm to 190 μm . The 5% efficiency gain observed for BSF cells with today's cell thickness increases to approximately 10% for the thinner cells under development for this program.

Figure 4

Figure 5

The thinner BSF cells have increased efficiency because:

1. The fired aluminum on the back increases the back reflectance, enhancing the long wavelength response.
2. The BSF cells have lower back surface recombination velocity also enhancing the long wavelength response.
3. The presence of a p^+ junction on the back repels minority carriers, enhancing long wavelength response and increases the cell open circuit voltage.

4. There is less series resistance loss due to flow of majority carriers through the bulk of the silicon to the back junction, increasing the fill factor.

The initial back surface field work utilized Solarex's standard back spray process on top of the fired aluminum paste. This may not be the most cost effective sequence, since both back spray and the BSF process provide enough back conductivity to produce high efficiency cells. Therefore, it may be more cost effective to replace backspray with a screen printed Ag-Al paste grid. Table 4 shows the comparison of using either back spray or back print over the Al paste BSF back. The two processes yielded cells that have the same performance.

Table 4
Backspray versus Back Print over BSF

	Efficiency (%)	Jsc (mA/cm ²)	Voc (mV)	FF (%)
Backspray	13.2	30.68	579.3	74.2
Back Print	13.26	30.65	581.8	74.3

Rather than utilize a full back print grid on top of the fired aluminum, we investigated the possibility of just printing Al-Ag pads in the places where soldering is required. A set of cells were made using Al paste BSF and screen printed back pads with no back spray. As shown in Table 5 cell efficiencies averaged 13.6%, typical of BSF cells. Thirty six of these cells were then used to make a module. The cells were processed through production using the automatic tabber to solder the fronts and the X-Y positioner to solder the backs. There was good alignment of the solder heads to the back pads and good adhesion of the solder bonds. The module was laminated using a clear Tedlar back sheet so that the construction would be visible. The resultant module measured 65 watts, consistent with the quality of cells used (see Table 6). The fill factor was somewhat low (71.4%). Subsequent evaluation indicates that when only Al-Ag pads are printed, there is a significant difference between cell efficiency as measured on a test block and cell efficiency measured through soldered tabs. To maintain fill factor, the screen printed Al-Ag pattern must include at least a bus bar connecting the pads.

Table 5
Screen Printed Pad Cells

Efficiency (%)	Jsc (mA/cm ²)	Voc (mV)	FF (%)
13.61	31.65	593.1	72.5

Table 6
Module with Screen Printed Pads

Pmax (W)	Isc (A)	Voc (mV)	FF (%)
65.0	4.25	21.4	71.4

As part of the paste-back print trial, a group of thin (175 μ m) wafers were processed to gain experience with handling and printing of thin cells. Most of the thin cells made it through the cell process. They were even successfully tabbed on the automated tabbing equipment. The electrical results are shown in Table 7. The electrical results were not as good as the standard

thickness BSF cells (13.26% versus 13.6%), but since they were not matched silicon it is really not appropriate to compare the results.

Table 7
Trial of Screen Printed Thin Cells

Efficiency (%)	Jsc (mA/cm²)	Voc (mV)	FF (%)
13.26	30.74	598.7	72.0

The initial experiments with Al paste BSF involved a process with separate firings for the Al back paste and the Ag front paste. It would clearly be less costly if the pastes could all be fired at the same time. This would save process time, reduce equipment requirements and finally eliminate the potential for the Al back to bead during the second firing. A DoE trial was used to evaluate a variety of process conditions. Cell results are given in Table 8. The best group occurred at the center point of the design, producing an average cell efficiency of 13.7%, which is as good as usually achieved with the separate paste firings. Further optimization around the center point is likely to improve the results. This is very encouraging for design of a cost effective process.

Table 8
Single Firing Cell Process

Group #	Efficiency (%)	Jsc (mA/cm²)	Voc (mV)	FF (%)
1	13.34	31.6	582.9	72.4
2	9.27	31.64	537.7	54.5
3	13.69	31.93	583.5	73.5
4	12.1	30.45	581.2	68.3
5	13.3	32.51	576.0	71.0

3.3.2 Phosphorous Gettering

There have been a number of reports on the use of phosphorous gettering to improve the efficiency of solar cells, particularly on polycrystalline material^{8,9}. The most compelling results to date were those published by James Gee¹⁰ who reported a large increase in minority carrier lifetime after gettering for Solarex cast polycrystalline material.

If phosphorous gettering is to be a useful part of our high efficiency process sequence it must be compatible with the other components of that process sequence. Therefore, we investigated phosphorous gettering in conjunction with back surface fields and other components of the cell process sequence¹¹. Design of experiment (DoE) techniques were utilized to evaluate the impact of various factors on cell performance.

In the first experiment the variables were the wafer surface condition, the position of the wafer in the ingot and the use of a back surface field. All of the wafers were gettered using the optimum conditions defined by the previous work. The measured response variables were the open circuit voltages and short circuit currents of the cells. No antireflective coating was used in this experiment. The effects of the main factors are presented in Table 9. All of the results

are reported as a percentage change from the controls. The control cells had no BSF, were not gettered, but did have a damage etch. High and Low denote the relative position of the wafer in the ingot. It is clear from Table 9 that the BSF has a dominating effect on the performance of the cells. The effects of the other factors were studied using more detailed statistical analysis. The Analysis of Variance (ANOVA) Table for this experiment is presented as Table 10.

Preparation of the wafer surface, one of the factors considered in Experiment 1, was replaced by the method of emitter formation in Experiment 2. The two conditions were emitter etch off and emitter etch back. The cell results of the emitter etch back were very low, because the surface concentration of phosphorus after the emitter etch back was too low to form good ohmic contact to the screen printed metallization. The control cells for the second experiment were damage etched with a standard emitter and had a BSF. The impact of BSF and the position of the wafer in the brick is shown in Table 11. There was a 2.7% gain in the short circuit current density and efficiency for the cells originating from the top region of the ingot as a result of phosphorus gettering, in addition to the gain obtained from the BSF. The results obtained from the statistical analysis are shown in graphical form in Figure 6a and 6b.

Table 9
Phosphorous Gettering Experiment #1

BSF	ETCH	HEIGHT	GETTER	Change in Isc %	Change in Voc (%)
Yes	Yes	Low	Yes	6.4	1.3
No	Yes	Low	Yes	2.7	0.2
No	No	Low	Yes	-1.4	-2.1
Yes	No	Low	Yes	3.5	-1.4
No	Yes	High	Yes	1.2	-0.3
Yes	Yes	High	Yes	5.9	0.7
No	No	High	Yes	0.2	-1.0
Yes	No	High	Yes	5.4	0.2

Table 10

ANOVA Table for Isc for Gettering Experiment #1

Effect	Sum of Squares	Degrees of Freedom	Mean Square	F-Ratio	P-Value
A: BSF	0.03315	1	0.03315	216.51	0.0426
B: Si Surface	0.00714	1	0.00714	46.63	0.0913
C: Si Height	0.00007	1	0.00007	0.43	0.6355
AB	0.00004	1	0.00004	0.24	0.7163
AC	0.00012	1	0.00012	0.78	0.5461
BC	0.00308	1	0.00308	20.12	0.1377
Total Error	0.00015	1	0.00015		
Total (Corr.)	0.04375	7			

R-Squared = 0.9965

R-Squared (adjusted for degrees of freedom) = 0.9755

Table 11

Phosphorous Gettering Experiment #2

BSF	EMITTER	HEIGHT	GETTERING	Change Isc %	Change in Voc (%)
No	Etch off	Low	Yes	-5.2	-2.0
No	Etch off	High	Yes	-4.1	-1.6
Yes	Etch off	Low	Yes	-0.2	0.3
Yes	Etch off	High	Yes	2.7	-0.2

Figure 6a

Isc for Phosphorous Gettering Experiment #2

Figure 6b
Voc for Phosphorous Gettering Experiment #2

3.3.3 Mechanical Texturing

An improved method for evaluating the performance of an optical coupling surface in terms of its performance on solar cells has been developed in this program¹². The model predicted and we verified experimentally that chemical and mechanical texturing increase the short circuit current and maximum power of encapsulated solar cells by approximately 3% over planar cells made on the same material with the same cell process⁶. Work during this period involved use of mechanical texturing in the integrated process sequence as described in Section 3.3.5 and development of a tool to texture etch a cell in a single pass.

The large area texturing tool was mounted onto a Meyer Burger grinding machine. The tool mounted easily, was adequately concentric and was able to operate at high speeds. However, the machining of the tool was not particularly uniform. In each section there was one tooth that was much longer than the others. This tooth began cutting before the others and because of its large size, it cut too deeply before the other grooves were cut to the correct depth. The manufacturer of the tool has agreed to remachine it to eliminate the high teeth. At the same time we are looking for alternate vendors to provide us tools within the specified tolerance.

3.3.4 Integrated Cell Sequence

Both mechanical texturing and phosphorous gettering result in increased cell efficiencies. To utilize these technologies, they must be incorporated into a cost effective integrated cell process sequence. We have begun the effort to integrate the various components of the cell process into a high efficiency process, hopefully in a cost effective manner. An experiment was run combining mechanical texturing, phosphorous gettering and Al paste back surface field. The results were some of the highest efficiency full sized (11.4 cm by 11.4 cm) screen printed cells we have ever made. The cell results are given in Table 12. All cells shown in this table had an Al paste BSF. Both the mechanical texturing and the phosphorous gettering provided an efficiency increase.

Table 12
Integrated Cell Process Sequence (Bare Cells)

Samples	Efficiency (%)	Jsc (mA/cm²)	Voc (mV)	FF (%)
Planar Poly	13.67	31.38	597.1	73.0
Mechanical	14.06	32.30	595.9	73.0
Texture Poly				
Mech Tex Poly	14.35	32.61	597.7	73.6
+ Gettering				
Planar CZ	15.07	33.05	613.2	74.4

Since our cells are designed to be most efficient when encapsulated, cells from each of the three polycrystalline groups were tabbed and encapsulated using EVA and standard low iron glass. The results are given in Table 13. The encapsulated cell with both mechanical texturing and phosphorous gettering measured almost 14.9% efficient at STC. Measurement of the spectral response of this cell indicated that the current measured by our simulator is probably 1% less than the actual AM1.5 current meaning this cell was very close to the program goal of 15%.

Table 13
Integrated Cell Process Sequence (Encapsulated Cells)

Sample	Efficiency (%)	Jsc (mA/cm²)	Voc (mV)	FF (%)
Planar Poly	14.0	32.28	599	72.5
Mechanical	14.56	32.90	597	74.1
Texture Poly				
Mech Tex Poly +	14.88	33.04	600	75.1
Gettering				

A second larger run of high efficiency cells was utilized to fabricate two 36 cell modules for delivery to NREL. Test results for the modules are given in Table 14. The module measurements are consistent with the cell results, indicating no particular problems associated with using these cells in modules.

Table 14
Modules from Integrated Cell Process

Module	Max Power (W)	Isc (A)	Voc (V)	FF (%)
001	66.2	4.13	21.5	74.4
002	65.5	4.08	21.5	74.7

3.3.5 15.2 cm by 15.2 cm Solar Cells

The first issue in the design of the larger cell was to select the exact size. While our original plan called for the cells to be 15 cm by 15 cm, all of the equipment, the cassettes and the glass could accommodate a somewhat larger size. Solarex already has a commercial cell that is 11.4 cm by 15.2 cm in size. Selecting the larger cell to have one dimension in common with this

commercial cell has a number of advantages in terms of tooling and module BOS. Therefore, we selected 15.2 cm by 15.2 cm as the dimensions for the new cell.

Using process parameters developed for a 12.7% efficient 11.4 cm by 11.4 cm solar cell our model predicts the results shown in Figure 7. The model predicts that the efficiency will drop from 12.7% for the 11.4 cm by 11.4 cm solar cell to 12.4% for the 15.2 cm by 15.2 cm solar cell. Some of this efficiency loss can be recovered by utilizing wider and thicker interconnect ribbon and by increasing the number of solder joints on each cell. The option of adding additional buss bars (and interconnects) was evaluated, but the calculations indicated that the present two bus system would produce higher efficiency cells. The analysis lead to the design of a cell with 53 fingers and 2 buss bars with 6 solder bonds on the front of each interconnect and 3 solder bonds on the back of each interconnect.

To accommodate the large cells a number of modifications had to be made to equipment and tooling. Among these were:

1. Preparation of back spray masks.
2. Procurement of larger cassettes for handling through the liquid processes.
3. Screens for the front print pattern, back print pattern and aluminum paste BSF.
4. Wider and thicker tabbing ribbon.
5. Adjustment of the automated tabbing and matrixing equipment to handle the larger size.
6. Test equipment with large enough test block, uniform light exposure and power supply with sufficient current.

Modifications required to make larger cells have been completed. Those required for testing and module assembly are still ongoing.

The first 15.2 cm by 15.2 cm cells were fabricated during this period. The first group of cells were made using the standard process, without BSF, but using the higher resistivity silicon specifically designed for use with a BSF. A full size PVMaT module was made using 36 of these cells. The results are given in the first line of Table 14. A power of 108 watts equates to an average encapsulated cell efficiency of 13%, a very respectable value for the technology employed.

The second group of large cells was made with an aluminum paste BSF and screen printed Al-Ag back pads. These cells measured at least 5% higher than the cells from the first run, consistent with the use of a BSF. Cells from this group were then used to fabricate a 36 cell module. The results are given in the second line of Table 15. The current increased appreciably over the first module, but the fill factor was lower. Further investigation lead to the discovery that the use of just screen printed pads on the back of the cell is inadequate. There is approximately a 4% reduction in fill factor when comparing the same cell measured with back tabs versus measuring it on a test block. We have already evaluated several alternative back screen patterns and found several that reduce this fill factor difference to zero.

Table 15
PVMaT Modules with 15.2 cm by 15.2 cm Cells

Sample	Pmax (W)	Isc (A)	Voc (V)	FF (%)
#1 standard	108	7.16	21.0	72.0
#2 BSF	109.3	7.59	21.2	68.0

3.4 TASK 9 - AUTOMATED MODULE ASSEMBLY

The goal of this task is to modify Solarex's present automated matrix and module lay-up system to increase throughput by 100% and decrease the labor requirement by 50%. To assist Solarex in analyzing how this equipment can be improved to increase capacity and reduce labor, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington is serving as a subcontractor.

3.4.1 Modeling and Expansion

The first step in this task was the development of a process flow chart detailing all of the module assembly steps. ARRI used this information to model and analyze the manufacturing process. As a short term goal they identified the changes necessary to increase production capacity by 40% to meet Solarex's short term business plan. These changes were successfully implemented during the first year of the contract⁶.

The second phase of the program was designed to meet the PVMaT contract goal of increasing capacity by a factor of 100% from the original 1993 baseline capacity. ARRI developed two Factory of the Future concepts to meet this requirement. They used AT&T's discrete event simulation package called Witness to evaluate each scenario. The Witness software is capable of

modeling resource interactions in detail and providing an accurate representation of the factory using statistical analysis. The Witness software provided an analysis of the capacity and resource requirements of the two Factory of the Future concepts.

For Concept 1 Witness predicts an increase in production capacity of 58% over the present "As-Is" system or 120% increase over the PVMaT baseline. Labor utilization analysis indicates that Concept 1 requires no more labor than the baseline case, thereby reducing the labor content per module (or per watt) to 45% of the baseline.

For Concept 2 Witness predicts an increase in production capacity of 75% over the present "As-Is" system or 146% increase over the PVMaT baseline. Labor utilization analysis indicates that Concept 2 requires one less operator than the baseline case, thereby reducing the labor content per module (or per watt) to 37% of the baseline.

While the two proposed concepts could meet the PVMaT goals they could not meet Solarex's publicly announced polycrystalline expansion program designed to triple capacity by 1999. To meet this expanded capacity requirement, Solarex and ARRI developed a new factory concept that would allow for incremental increases to meet the shorter term capacity requirements and would ultimately result in the required tripling of module assembly capacity. The plan was based on replacing the back solder robots with XY positioners to increase the number of solder bonds made at one time from 2 to 4, thereby increasing the through-put by nearly a factor of two. This modification was implemented during the second year of the program. The XY positioners are now on line and operating at the capacity predicted.

Solarex provided ARRI with a module build plan for each year through 1999. The Witness model developed initially in Year 1 was updated with the latest changes in the factory and used as a base model. Changes in the model were made for subsequent years thereafter (through 1999) providing a representation of the future factory. As the volume of product is ramped up, various pieces of equipment will reach maximum throughput capacity. ARRI provided Solarex with a table of additional equipment requirements by year. This analysis then became the basis for establishing a capital investment budget for equipment purchases. The following areas were identified as requiring increased capacity within the next year.

1. Tabbing System - Solarex has already begun the process of identifying and procuring an additional tabbing system.
2. Module Lay-up System - Modifications to the system are required to reduce the cycle time to handle the increased output of the XY positioners. One of robots that had been doing the back soldering will be transferred to matrix lay-up. ARRI is assisting Solarex in the development of an improved method for dispensing the EVA sheet.
3. Laminator Capacity - Solarex procured, installed and is using a new Spire laminator to increase the lamination capacity.
4. Framing System - The cycle time of the framing system is too long to meet the framing requirements. ARRI is assisting in redesign of the system to reduce cycle time by 50%.

ARRI is continuing to support Solarex to improve and streamline the module assembly operation. Areas of emphasis are:

- Lay-up robot: It would simplify the process if tabbed cells could be placed directly onto the EVA-glass and soldered in place. This can only be accomplished if the alignment of cells as they are placed on the matrix is improved and if some method of detecting and removing broken cells is developed. If these issues can be solved, we would then determine if it is feasible to solder on top of the EVA.
- EVA handling: The properties of the EVA we use today will not allow us to roll it out and cut it directly onto the glass. Our EVA vendor, Springborn, is now reviewing their process and handling to determine if they can make the necessary changes so the EVA can be handled in this way.
- Trim/Lead Attach: ARRI is designing a work station to allow inspection, lead attach and testing without requiring operators to lift the modules. A concept work station design has been presented to Solarex staff and approved for development into a prototype.
- Module Transfer Cart: ARRI is designing a common module transfer cart to be used to transfer modules from the laminator through the framing operation, that reduces operator lifting of the modules. A conceptual design has been presented to Solarex staff and approved for development into a prototype.
- Framing: ARRI has recommended a number of changes to the framing robot system that would decrease the cycle time. A prototype of a direct frame feeding/butyl dispensing system has been designed and is being built.

3.4.2 Spire Assembly System

Spire Corporation of Bedford, Massachusetts has a PVMaT contract to develop automated high throughput equipment for interconnecting large area solar cells¹³. To evaluate the Spire equipment and process, standard Solarex 11.4 cm by 11.4 cm polycrystalline solar cells were shipped to Spire. Spire tabbed the cells and made strings of 9 cells each for incorporation into Solarex MSX-60 modules. Solarex completed fabrication of three modules. The results of module performance is given in Table 16. All three of the modules made from Spire strings had normal electrical output.

Table 16
Modules Made from Spire Strings

Module	Isc (A)	Voc (V)	FF (%)	Pmax (W)
Spire 1	3.86	21.3	73.9	60.9
Spire 2	3.88	21.3	73.6	60.7
Spire 3	3.86	21.3	73.9	60.7
Reference	3.80	21.4	74.0	60.1

These modules were then subjected to accelerated stress tests from IEC 1215 and IEEE 1262 PV Module Qualification Test Sequences. Since we only had 3 modules, we used one in each of the three environmental test legs. All three modules successfully passed the requirements of IEC 1215 and IEEE 1262.

3.5 TASK 10 - FRAMELESS MODULE DEVELOPMENT

In this task Solarex will develop and qualify a frameless module design incorporating a lower cost back sheet material (less than \$0.05/square foot) and user friendly, low cost electrical termination (less than \$1.00/module).

3.5.1 Backsheet

A key component in frameless module design is the backsheet, since the electrical termination and the support system itself must adhere to the backsheet. This offered an additional opportunity to reduce cost from the 3 part backsheet being used at Solarex at the start of this PVMaT Program.

Three candidate materials were selected for evaluation:

- Pigmented Chlorinated polyethylene (CPE)
- Affinity polyolefin
- Thin Tedlar - polyvinyl fluoride

Small modules made from these materials successfully completed environmental qualification testing to IEC 1215 and IEEE 1262. The three materials also successfully passed in-house simulated UL fire tests.

Each material was then exposed directly to a equivalent of 2 years UV in Phoenix, AZ. We estimate that the normal UV exposure of the back sheet is no more than 10% of direct exposure, so this test should represent 20 years of UV on the back of the module. All of the materials except for the CPE shown no degradation after the UV exposure. The CPE samples turned a dark black color with evidence of leaching of green pigment from the samples exposed to UV. Based on these results we have dropped CPE as a candidate back sheet.

Large area samples of white pigmented polyolefin were provided by Richmond Technology. This material was utilized as a backsheet in the standard EVA lamination process. After lamination all of the samples had numerous pin holes through the back sheet. Most of these pin holes occurred directly over solder bonds, although others appeared over back tabs, but not where they were soldered. It appears that the polyolefin gets too soft at the lamination temperature and is easily punctured by any irregularities that occur behind the cells. Unless we can find an inexpensive way to strength the polyolefin, it will not work as our back sheet.

We are now left with only single sheet thin Tedlar as a candidate material. Tedlar does meet all of the technical requirements of a back sheet and Solarex has been using a single layer Tedlar backsheet now for several years. However, Tedlar will not meet the \$0.05/square foot cost goal of this PVMaT program. However, it does represents at least a 70% reduction in back sheet cost over the three part material that Solarex was using at the beginning of this PVMaT program.

3.5.2 Electrical Termination

Most commercial modules have junction boxes for electrical termination. While these provide for a great deal of flexibility in use, they are expensive to purchase, probably will not meet the

PVMaT cost goals and require significant labor of skilled electrical personnel for field installation. Our initial approach was to use a quick connect-disconnect system that would eliminate most of the field assembly labor. However, we were unable to find such a system that would meet our environmental requirements and cost less than \$1.00 per set of male and female connectors. Therefore, we changed our approach and decided to use a quick connect system that doesn't offer quick disconnect. This may actually have some advantages in the field because it will make it more difficult for unauthorized personnel to disconnect modules and such systems are less likely to accidentally become all or partially disconnected.

We have selected a butt crimp connector and SPC Technology type PHS black polyolefin shrink tubing. These connectors have successfully passed all of the requirements of IEC 1215 and IEEE 1262. Samples are undergoing extended outdoor testing.

3.5.3 Mounting System

The frameless module mounting system is based on the use of 3M's Very High Bond (VHB) Tape to attach the back of the module directly to galvanized B-Line cross members. The prototype system has now been under test at our Frederick facility for more than 1 year. The array, especially the tape has held up well to the weather, including high winds during several severe storms. Solarex has now used this mounting system to build several large PV arrays.

3.6 TASK 11 - Automated Thin Cell Handling

In this task Solarex will develop automated handling equipment for 200 μm thick 15 cm x 15 cm polycrystalline silicon wafers and cells that has high yield (less than 0.1% breakage per process handling step) and can handle at least 12 cells per minute. ARRI is under subcontract to assist Solarex in the development of handling methods and equipment for large thin wafers and cells.

3.6.1 Silicon Wafer Fracture Testing

ARRI begun the effort by determining the stress limits for handling large area wafers and solar cells. The initial analysis was based upon destructive testing of wafers. The amount of weight that must be applied to fracture a wafer was then used to calculate the maximum stress a polycrystalline silicon wafer will withstand. Details of the test design and results were presented in the Third Semiannual report for this program⁵.

A four-point bend test was developed, where the specimen is supported along its length at two points and a distributed load is applied transversely causing the specimen to bend in flexure and ultimately fracture at a certain load. The test structure is shown in Figure 8. The bottom plate B contains 2 pins running the length of the plate, spaced 5.125 cm apart. A test wafer is placed on top of the pins. Plate A with 2 pins running the length of the plate, spaced 2.55 cm apart, is placed on top of the wafer. Weights are added in steps on the center of the top plate A till the specimen fractures. The deflection at each step of load is recorded as well as the final load to fracture.

The bend strength shows some scatter, yielding an average bend strength of 124.6 MPa. The scatter in strength results determined from the four-point bending experiment is shown in Figure 9. The average value of Young's modulus for the bending tests was 24.5 Mpsi (169 Gpa) in

excellent agreement with the value of 23.56 Mpsi as reported by King¹⁴ for polycrystalline silicon and the value of 27.5 Psi (190 Gpa) as reported by McGuire¹⁵. The primary mechanism of failure was transgranular cleavage failure.

Figure 8
Four Point Bend Test

Figure 9
Bending Strength of Polycrystalline Silicon Wafer from Four Point Bending Test

3.6.2 Interpretation of Wafer Strength

The scatter in strengths may be modeled using Weibull statistics¹⁶. Using the weakest link model, the strength distribution is given by:

$$F = 1 - \exp - \int_v \left(\frac{\sigma - \sigma_u}{\sigma_o} \right)^m dV$$

where F is the probability of failure of a specimen, V is the specimen volume, σ is the maximum tensile stress at any given point, σ_u is the threshold stress (below which no failure will occur), σ_o is the characteristic strength, and m is the Weibull modulus. In four-point bending a rectangular specimen has an effective volume given by:

$$V_E = \frac{V(m+2)}{4(m+1)^2}$$

Weibull graphs are a convenient means to report strength data. The graph has special axes chosen to linearize the data. Each strength is assigned a probability estimate given by:

$$F = \frac{(i - 0.5)}{N}$$

where i is the specimen number, and N is the total number of specimens. This estimator has been shown to have the least bias and lowest scatter¹⁶. Values of

$$\ln \ln \left[\frac{1}{(1-F)} \right]$$

are then plotted versus $\ln \sigma$ and a least square line is fitted to the data minimizing the scatter. The Weibull modulus is interpreted as the slope of the line on the graph. The characteristic strength of the test specimen is the stress for which the vertical axis has

$$\ln \ln \left[\frac{1}{(1-F)} \right] = 0.$$

The Weibull graph is shown in Figure 10. It has been used to determine that the Weibull modulus is 9.56.

Figure 10
Weibull Graph
Modulus and Strength Estimate

A plot of the strength distribution F versus σ_f , where σ_f is the experimentally determined stress for failure of the wafer is shown in Figure 11.

Figure 11
Weibull Graph
Strength versus Probability of Failure

3.6.3 Simulation of Wafer Handling

ARRI has developed a Finite Element Model to analyze a realistic handling scenario. The scenario consisted of a handling process in which a 11.4 cm by 11.4 cm wafer with a thickness of 288 μm was lifted from a stack using four suction cups. In the model, a loading pattern was defined with 4 suction cups symmetrically placed around the center of the wafer, while the edges of the wafer are restrained from displacement in the direction of the load. A simulated load of 0.25 lb. was applied to each of the 4 points. The calculation yielded a maximum stress of 28 MPa and a deflection of 0.0864 cm. From the relationship between strength and probability in Figure 11, the average strength in bending, 125 MPa, determined from the four point bending test, corresponds to a probability of failure of 7%. It would require a force in excess of 1 lb. on each suction cup to reach this level of stress. The calculated stress of 28 MPa for the 0.25 lb. per suction cup scenario will have a very low probability of failure (breakage) and so would be an acceptable design for wafer handling equipment.

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