MULTI-LEVEL INTERCONNECTS FOR HETEROJUNCTION BIPOLAR TRANSISTOR

INTEGRATED CIRCUIT TECHNOLOGIES

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Heterojunction bipolar transistors (HBTs) are mesa structures which present difficult planarization problems in integrated circuit fabrication. We report a multilevel metal interconnect technology using Benzocyclobutene (BCB) to implement high-speed, low-power photoreceivers based on InGaAs/InP HBTs. Processes for patterning and dry etching BCB to achieve smooth via holes with sloped sidewalls are presented. Excellent planarization of 1.9 μm mesa topographies on InGaAs/InP device structures is demonstrated using scanning electron microscopy (SEM). Additionally, SEM cross sections of both the multi-level metal interconnect via holes and the base-emitter via holes required in the HBT IC process are presented. All via holes exhibit sloped sidewalls with slopes of 0.4 $\mu\text{m}/\mu\text{m}$ to 2 $\mu\text{m}/\mu\text{m}$ which are needed to realize a robust interconnect process. Specific contact resistances of the interconnects are found to be less than $6 \times 10^{-8} \Omega\text{cm}^2$. Integrated circuits utilizing InGaAs/InP HBTs are fabricated to demonstrate the applicability and compatibility of the multi-level interconnect technology with integrated circuit processing.

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I. Introduction

Heterojunction bipolar transistor (HBT) technologies are attractive for electronic and optoelectronic applications requiring high-speed and low-power consumption, as well as high current drive or sink capabilities. Due to the nonplanar structure of the HBT, a low-loss, low-stress, stable dielectric material exhibiting good metal and semiconductor adhesion properties and chemical stability at elevated temperatures is required for planarization. This dielectric material must insure electrical isolation between multi-level metals over discrete devices. Additionally, via holes through the dielectric material at different levels in the HBT structure must be etched with sloped sidewalls to yield low resistance metal interconnects that are essential for high-speed, low-power integrated circuit implementation.

Numerous types of dielectric films such as SiO_2 , SiN , and polyimides are used for implementation of interconnect technologies. SiO_2 and SiN can suffer from interfacial strain that exists when they are deposited on the compound semiconductors. Polyimides can exhibit poor adhesion properties which make packaging and bonding difficult. Benzocyclobutene (BCB), originally used extensively for multi-chip module (MCM) applications, is a thermoset resin which exhibits a relatively low dielectric constant of 2.7, low water absorption properties, good adhesion properties, and excellent planarization properties[1,2]. Within the past few years, BCB has been investigated for planarization and multi-level interconnects based on various devices[3-6]. In this paper, we report a multi-level metal interconnect technology using BCB to implement high-speed, low-power photoreceivers based on InGaAs/InP HBTs.

Detailed BCB processing information is discussed in the next section. The Results and Discussion section discusses planarization, via hole etch results, and specific contact resistances of the interconnects. The compatibility and functionality of the interconnect processes is demonstrated with an InGaAs/InP HBT-based optoelectronic integrated circuit (OEIC) process.

II. Experimental

The InGaAs/InP high-speed, low-power photoreceiver circuit was implemented with InGaAs/InP HBTs, InGaAs pin photodiodes, and either TaN or NiCr thin film resistors. The circuit design, material stack and process development for the HBT, photodiode, and resistor technologies have been discussed in detail previously and will only be summarized in this paper[7,8]. Figure 1 shows a cross section diagram of a planarized HBT. The fabrication process begins with a non-alloyed emitter contact deposition. This ohmic metal was used as the etch mask for the emitter mesa etch. The emitter mesa was formed using a wet-dry etch combination to etch down to the InGaAs base layer. This combination etch process provides the necessary mesa recess under the emitter ohmic metal to insure that the self-aligned, non-alloyed base ohmic contact deposited in the next step will be electrically isolated from the emitter mesa. After the base ohmic metal is deposited, 0.2 μm of SiN is deposited on top of the InGaAs base layer for junction protection and to improve the via hole etch process. The base mesa is then patterned and the SiN on the InGaAs base layer is etched. This thin layer of SiN covering the base mesa is the semi-transparent layer visible in the inset of Figure 2. A wet-dry etch process is used to etch through the InGaAs base, the InGaAs collector, and stop at the InP subcollector. The non-alloyed collector ohmic metal is defined and an sloped sidewall collector mesa is defined with a selective InP wet etch enabling the first metal to be brought up on to the collector mesa to contact the collector ohmic metal. The remaining optoelectronic integrated circuit fabrication prior to planarization includes TaN or NiCr thin film resistor deposition and deposition of first metal. The HBT has a vertical change of 1.9 μm from the substrate field to the top of the emitter ohmic metal and represents a difficult interconnect problem.

Planarization is accomplished via spin coating of BCB. Thicknesses ranging from 0.9 μm up to 12 μm are achievable with single spin applications using BCB. For this work, BCB 3022-35 with a solid content of 35% is used. Thickness versus spin speed measurements show that post cure BCB thicknesses between 0.95 μm at 6 krpm to 1.4 μm at 3 krpm are obtainable.

Two types of adhesion promoters, designed for use with BCB, were investigated . 3-

Methacryloxypropyl-trimethoxysilane (MOPs) is a methanol-based adhesion promoter while 3-

Aminopropyl-triethoxysilane (APS-3) is a water-based adhesion promoter. The same application procedure was used for each adhesion promoter and BCB coating. A solvent clean followed by a dehydration bake at 120 °C for 3 minutes was performed initially. The adhesion promoter was applied dynamically on a spinner at 3 krpm for 30 seconds. During the adhesion promoter spin cycle, the spin speed was ramped to the spin speed required to obtain the targeted post cured BCB thickness. The BCB was applied via a syringe with a 0.2µm filter in place and spun at 5.2 krpm for 30 seconds to yield a post cure BCB thickness of 1.0 µm. Cured BCB samples prepared with both MOPs and APS-3 were subjected to tape tests. Delamination did not occur for samples prepared with either adhesion promoter. APS-3 was used for all subsequent BCB adhesion promoter treatments.

The BCB was cured in a nitrogen purged, quartz tube furnace with ramped temperature control. The atmosphere was continuously purged with nitrogen during the cure cycle to avoid degradation of the BCB electrical properties. The curing cycle began with a 30 minute ramp to 50 °C, followed by a ramp to 300 °C in 80 minutes where it soaked for 30 minutes. The sample cooled to room temperature in approximately three hours.

A sizeable BCB edge bead was produced with this process which must be removed in order to achieve well-resolved sub-micron size features with subsequent photolithography. The edge bead was removed by dry etching. A thick positive tone resist, postbaked at 120 °C for 3 minutes, was used as an etch mask during edge bead removal. As BCB is a silicon-based polymer, the etch chemistry must include fluorine to obtain an appreciable etch rate. Our etch process uses 3.6 sccm of O₂, 2 sccm of SF₆, a controlled pressure of 250 mT, and RF power density of 0.45 W/cm² to yield a BCB etch rate of approximately 0.5 µm/min and a photoresist etch rate of approximately 0.4 µm/min.

As diagrammed in Figure 1, the first metal via holes and the base-emitter via holes differ in depth by over 1 μm . In order to maintain the sub-micron resolution required for base-emitter via holes, it is necessary to etch the first metal via holes and the base-emitter via holes in two separate processes. The first metal via hole was etched first. It is a $8 \times 8 \mu\text{m}^2$ via hole which enables interconnection of the second level metal to the first metal. The second etch defines the base-emitter via holes which range from $1.6 \times 7.4 \mu\text{m}^2$ down to $1.2 \times 2.6 \mu\text{m}^2$ in size. The base-emitter via holes enable electrical contact to the base and emitter ohmic contacts which are on mesas $\sim 1.4 \mu\text{m}$ higher than the semi-insulating field.

The first metal via hole etch mask was defined using a $1.8 \mu\text{m}$ thick photoresist layer. The photoresist was postbaked at 120°C for 3 minutes. This postbake process flows the photoresist to produce a sloped sidewall profile in the patterned openings. During the etch process, the sloped sidewall will be transferred into the BCB. This sloped sidewall profile is desirable for the first metal via hole to insure good step coverage of the second metal interconnect and improve yield.

The base-emitter via hole etch mask was defined using a $1.1 \mu\text{m}$ thick positive tone photoresist process. Both flowed and unflowed photoresist profiles were investigated as etch masks for the base-emitter via holes. Unflowed photoresist profiles were determined to yield more desirable base-emitter via hole results than flowed photoresist profiles. This is discussed in more detail in the Results and Discussion section.

The BCB via holes were etched using 2 sccm of O_2 , 10 sccm of SF_6 , a pressure of 100 mT, and RF power density of 0.45 W/cm^2 . This etch chemistry removes BCB at a rate of $\sim 0.1 \mu\text{m/min}$ and photoresist at $\sim 0.09 \mu\text{m/min}$. We observed particulate formation in the via holes when completing the via hole etch in the presence of O_2 . The O_2 is required in the BCB process to etch the photoresist mask during the BCB etch to form sloped sidewalls in the via holes. As mentioned previously, a thin SiN layer is used to protect the base-emitter junctions. The requirement to etch this thin SiN in the via holes provided the means to avoid the particulate formation. The SF_6 and

O₂ based BCB etch is terminated as close to the BCB/SiN interface as possible. An SF₆ only is used to slowly etch through the SiN and minimize particulate formation. This SiN etch has the following parameters: 2.5 sccm SF₆, 50 mT controlled pressure, and 0.3 W/cm² RF power density and etches both BCB and SiN at approximately 60 nm/min.

III. Results and Discussion

The highly non-planar topography of a typical HBT is shown in Figure 1. This clearly shows the difficulties of implementing interconnects to the ohmic contacts at three different mesa heights which can vertically span over one micron. Further complications arise from the great difference in the via hole dimensions which vary from as small as sub-micron for the base and emitter via holes to tens of microns for the first metal interconnect on the substrate. The inset in Figure 2 shows an HBT with an emitter of $2.6 \times 10.4 \mu\text{m}^2$ that is used in the optoelectronic integrated circuit process reported here. The inset clearly shows the non-planar features of the HBT structure. The foreground SEM micrograph in Figure 2 shows the interdigitated interconnect to the center emitter ohmic contact and the two outer base ohmic contacts of a $2.6 \times 5.2 \mu\text{m}^2$ HBT also implemented in the OEIC process. This SEM micrograph vividly shows that BCB planarizes the HBT structure very effectively. Additionally, profilometer measurements of $1.9 \mu\text{m}$ topologies prior to planarization exhibit vertical changes of $0.6 \mu\text{m}$ after planarization indicating that greater than 68% degree of planarization is achieved.

In order to obtain cross section views of the base-emitter via holes, both via holes were patterned and etched into $1.0 \mu\text{m}$ of BCB on bare GaAs with the via holes oriented along a major flat. This was required as the small area HBTs in the integrated circuit process are oriented 45° to the major flat making cleaving difficult and impractical. It is noted that the absence of the $0.2 \mu\text{m}$ does not affect the shape of the via hole but does lead to the residue in the via holes as evident in Figures 3a and 3b. The first metal via hole, shown in Figure 3a, was formed by etching through the entire $1.0 \mu\text{m}$ BCB layer. The via holes are characterized by smooth sidewalls with slopes of less than $0.5 \mu\text{m}/\mu\text{m}$.

A $1.2 \times 7.4 \mu\text{m}^2$ base-emitter via hole, shown in Figure 3b, was etched approximately $0.55 \mu\text{m}$ deep using the flowed $1.1 \mu\text{m}$ thick photoresist etch mask. As seen from Figure 3b, the base-emitter via hole is characterized by sidewalls with slopes less than $1 \mu\text{m}/\mu\text{m}$. However, while the

bottom of the via hole is 1.2 μm wide, the top of the via hole is 3.8 μm wide. This large degree of lateral expansion during the etch is due to the flowed photoresist profile and is not tolerable in the base-emitter via hole definition due to the close proximity of the base and emitter via holes and the resulting alignment requirements. Additionally, the sub-micron openings in the flowed photoresist have on occasion flowed closed during the postbake. For these reasons and the additional fact that step coverage is not as severe a problem for the base-emitter interconnects as for the first metal interconnects, all base-emitter via etches use the unflowed 1.1 μm photoresist as an etch mask. SEM cross sections of base-emitter via holes produced with the unflowed photoresist mask are characterized by smooth openings with sidewall slopes of 2 $\mu\text{m}/\mu\text{m}$. Figure 4 shows a typical interdigitated metal interconnect to the base and emitter ohmic metals using the unflowed photoresist etch mask and a 0.6 μm thick interconnect metal. Excellent step coverage and low resistance contacts were obtained. Physical isolation between the base and emitter mesa is apparent and good yield is obtained.

Via hole interconnect chain measurements were used to determine the specific contact resistance of the metal-to-metal interconnections through the via holes described above. A current density of $1 \times 10^4 \text{ A/cm}^2$ was used for all the electrical measurements. Over five thousand first metal via holes were tested to obtain an average first metal via hole resistance of 0.012 Ω which includes the resistance of the interconnect metal. Removing the series resistance of the interconnect metal (0.037 Ω/square) yields a specific contact resistance of less than $5 \times 10^{-9} \Omega\text{cm}^2$. With a similar analysis, over 700 base-emitter via hole resistances were averaged to obtain an average base-emitter via hole resistance of 0.41 $\Omega/\text{via hole}$. A specific contact resistance of $6 \times 10^{-8} \Omega\text{cm}^2$ was obtained by taking into account the sheet resistance of both the interconnect metal (0.037 Ω/square) and the ohmic metal (0.149 Ω/square).

The via hole processes described above were incorporated into an OEIC fabrication process based on InGaAs/InP HBTs to produce the photoreceiver shown in Figure 5. This photoreceiver is implemented using three HBTs with one emitter and two base via holes per HBT, arrays of first

metal via holes for the interconnect to the first metal, three bias resistors, and two junction diodes.

HBTs with DC current gains in excess of 100 A/A and f_T greater than 40 Ghz have been fabricated

and reported previously[3,7]. Large arrays of the photoreceiver shown in Figure 5 were

implemented and have been functionally demonstrated to operate at bit rates in excess of 800

Mb/sec with greater speeds possible[3,7].

IV. Conclusions

We have developed robust processes for planarizing HBT-based integrated circuits using benzocyclobutene (BCB). Details of the via hole patterning and processing have been presented and discussed. These processes yield via holes with excellent profiles for achieving good step coverage which is essential for low resistance interconnects. First-to-second level sloped sidewall via holes 1 μ m deep have been demonstrated with specific contact resistances less than $5 \times 10^{-9} \Omega\text{cm}^2$. Additionally, via holes as small as $1.2 \times 2.6 \mu\text{m}^2$ have been successfully implemented with typical specific contact resistances of $6 \times 10^{-8} \Omega\text{cm}^2$ being observed. Integration of these BCB multilevel interconnect processes has been achieved and demonstrated by the fabrication of large arrays of photoreceivers with over 800 Mb/sec performance. These high performance circuits demonstrate that BCB is well-suited for multi-level interconnect technologies required for highly non-planar HBT-based integrated circuit technologies in both digital and analog applications.

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Figure Captions

Figure 1 Diagram of the highly non-planar mesa cross section of an HBT planarized with BCB and the first metal and base-emitter interconnects required for IC fabrication. The base and emitter interconnects are $1.4\mu\text{m}$ above the first metal interconnect which creates the need for definition of the base-emitter via holes in a separate process from the first metal interconnect.

Figure 2 The inset micrograph is a $2.6 \times 10.4 \mu\text{m}^2$ HBT prior to planarization. The foreground micrograph illustrates a side profile of a $2.6 \times 5.2 \mu\text{m}^2$ HBT with the interdigitated second metal interconnect to the emitter and base ohmic metals after planarization, via hole definition, and deposition of the interconnect metal.

Figure 3 a.) Cross section SEM micrograph of the $8 \times 8 \mu\text{m}^2$ 1st metal via hole. The via holes are characterized by smooth sidewalls with slopes of less than $0.5 \mu\text{m}/\mu\text{m}$. The particulates visible in the micrograph are reduced significantly with the addition of a thin SiN layer under the BCB and use of a SF_6 only dry etch to etch through the thin SiN layer.

Figure 3 b.) Cross section of a $1.2 \mu\text{m}$ wide base-emitter via hole using a flowed photoresist etch mask. Note the large degree of lateral expansion that occurs due to the flowed photoresist profile. Unflowed photoresist profiles are used in the OEIC interconnect process to avoid this problem.

Figure 4 Interdigitated emitter and base interconnect metal through the base-emitter via holes obtained with an unflowed photoresist etch mask and $0.6\mu\text{m}$ of interconnect metal.

Figure 5 A high-speed, low-power optoelectronic integrated circuit implemented with HBTs, diodes, resistors, and BCB multi-level interconnects. Large arrays of these photoreceivers have been operated at 800 Mbits/s demonstrating that BCB can be used to implement high quality interconnect technologies.

Figure 2

Figure 3 a.

Figure 3b.

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Figure 4

Figure 5