Low-Power, Parallel Photonic Interconnections for Multi-Chip Module Applications

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Abstract — New applications of photonic interconnects will involve the insertion of parallel-channel links into Multi-Chip Modules (MCMs). Such applications will drive photonic link components into more compact forms that consume far less power than traditional telecommunication data links. MCM-based applications will also require simplified drive circuitry, lower cost, and higher reliability than has been demonstrated currently in photonic and optoelectronic technologies. The work described is a parallel link array, designed for vertical (Z-Axis) interconnection of the layers in a MCM-based signal processor stack, operating at a data rate of 100 Mb/s. This interconnect is based upon high-efficiency VCSELs, HBT photoreceivers, integrated micro-optics, and MCM-compatible packaging techniques.

INTRODUCTION

Chip count, clock speed, and number of I/O per chip are growing rapidly in digital electronic systems, thus pushing the limits of electrical I/O channels on MCMs. The Semiconductor Industry Association (SIA) road map, for example, projects up to 2000 interconnects per chip or module (at 100-200 Mb/s) by the year 2001 [1]. While this is a requirement that represents the high end of the performance spectrum, applications such as distributed computing, signal and image processing, and display technology are certain to push the limits of interconnect technology.

Present two-dimensional MCM technology has done much to enable shorter electrical interconnect paths for reduced volume and higher performance. Similarly, stacking of MCMs will allow the advantages of compact packaging to be extended into a third dimension to further enable interconnect-intensive applications [2]. Many stacked MCM architectures, however, will benefit if they are easily separated. This would allow each high-value layer in the stack to be separately constructed, tested, and reworked as needed. Such an approach is presently limited by the lack of a high-density, low-crosstalk, separable interconnect that can run at 100 MHz (plus) clock speeds with acceptable ground-bounce.

Due to recent advances in devices and packaging, photonic technologies can now be applied to enable high-density z-axis interconnects as in Fig. 1. Here, photonic interconnect chips that communicate between levels are placed on the MCM among the electronic signal processing and memory chips that are electrically interconnected on each level. These photonic paths pass vertically through optical via holes in the MCM substrate or possibly the optical sources could operate at wavelengths where the substrate is transparent, thus forming a Z-Axis Photonic Interconnect (ZAPI).

Figure 1. The z-axis photonic interconnect concept for stacked, separable MCMs.

The ZAPI approach has several potential advantages over an area array of electrical interconnects for high-density, high-speed data transfer through the MCM stack. It can reduce problems caused by electrical parasitics and cross-talk at the separable pads and electrical through-substrate vias that would be required for stacking. Because the ZAPI system does not require *physical* contact of each of the interconnect channels as separable electrical pads would, it will need less mechanical pressure than large numbers of small-pitch electrical contacts, and may thus be capable of higher interconnect density. In addition, the optical signals may be tapped in order to test each of the MCM layers. Another advantage is that the ZAPI system will reduce the effect of ground bounce between the layers, thus acting as a multi-channel high-speed optical isolator system. Finally, the interconnect concepts, device technologies, and packaging approaches described here for simple "point-to-point" photonic interconnects could be applied to reconfigurable interconnect architectures that realize 3-D optically interconnected computers [3], [4].

The signal processing system that serves as the target application for the ZAPI implementation is based on 3.3 V CMOS electronics. It will operate at data rates of 80 to 100 Mb/s and will contain up to 2000 interconnect channels per layer in the stack. The goal for power consumption in the photonic interconnect is 20 W per layer (10 mW per channel). Individual modules in the z-axis stack are to be based on a "chips first" MCM technology such as General Electric's High Density Interconnect (HDI), where electrical interconnect layers are overlaid on top of the chips [5]. The photonic chip set that is being developed, however, could also be used to implement stacking in a "chips last" or MCM-D technology, where the chips are bonded onto the interconnect layers.

An important operational parameter for the Z-axis interconnect system is that it reproduce data exactly. Because the processors in the stack are highly interconnected, timing margin and latency are important factors to consider. In addition, the large number of

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parallel channels in the interconnect may preclude the use of advanced error coding or clock recovery circuits. Thus, photonic channels in the z-axis will need to carry data near the 100 Mb/s rate with rise and fall times of about 1.0 to 1.5 ns, pushing the equivalent link bandwidth to near 1 GHz. The signal fidelity and timing requirements in our application also preclude the use of multiplexing to reduce the number of physical data-carrying channels. Using present circuit technologies, multiplexing would unacceptably increase the latency associated with the interconnect, and would require much more power than the current budget allows. Thus, the z-axis interconnects must be established as parallel data channels operating at the system clock speed, and must appear much like another CMOS gate in the processing system. These timing requirements, combined with the need for low-power, low crosstalk operation, call for a system based on photonic device technologies such as Vertical Cavity Surface Emitting Lasers (VCSELs).

APPROACH

The design of this interconnect stack was directly driven by the above requirements, in conjunction with the additional constraints implied by packaging compatibility. A number of possible approaches and wavelengths were considered for the baseline emitter design, including visible LEDs and/or VCSELs, 1300 nm LEDs, and 980 nm VCSELs. Packaging constraints were identified for each of the approaches, based on substrate transparency issues and output characteristics of the optical source. Expected power budgets were also developed, according to emitter device and receiver circuit power consumption characteristics and light collection efficiency in the optical path.

Some of the most basic criteria that were found to influence the choice of approach were the packaging constraints. The most restrictive requirement was that the photonic devices must be compatible with a "chips first" packaging approach such as GE's High Density Interconnect (HDI) [5]. In this realization, the chips are all mounted in wells with the electrical interconnect overlaid on top. It would thus be very difficult to mix the mounting mode such that some chips are mounted up (in the normal HDI fashion) while others would be mounted down (thus needing electrical interconnects in the well of the MCM substrate). When chip mounting constraints are combined with the fact that the photonic channels must communicate both up and down to the next layer in the stack, the interconnect design becomes constrained to wavelengths and device technologies that allow light to be passed through the photonic device substrate. This will then allow for bi-directional communication as in the cross-section of Fig 2, shown for an advanced stack structure. Here, the outputs of the transmitter

Figure 2. Cross-section of an advanced "chips-first" architecture for z-axis photonic MCM interconnects. Reflective and transmissive optics are integrated into the photonic device substrates to effect upward or downward communications.

and receiver devices are reflected and/or focused (through their transparent substrates) to achieve bi-directional communications. A simplified two-layer test interconnect with mixed mounting modes (chip-up on one layer and chip-down on the next layer as in Figure 3) is currently under construction to demonstrate optical integration and functional link characteristics.

The next factor influencing interconnect design was the electrical power budget allowed for the interconnect. This called for a balancing of power consumed between the transmitter device and the photoreceiver circuit. In general, the more optical power that could be focused on the photoreceiver, the lower the amplifier gain in the circuit, resulting in a lower overall receiver power consumption at a given bit rate. The two factors in the source device that strongly influenced the power budget were overall conversion efficiency from electric power to light, and the divergence of the output light beam to be focused on the photoreceiver. In both of these areas, VCSELs are far superior to LEDs.

As demonstrated in our test interconnect based on LEDs, narrow-band resonant-cavity surface-emitting devices exhibited only a 2 percent power conversion efficiency and near-Lambertian beam profile [6]. Thus, even lenses with a numerical aperture of 0.4 (a full-angle acceptance cone of 47 degrees or f-number of 1.25) would only collect 16 percent of the output light. This would lead to low overall efficiency in the power budget and high cross-talk, compared to a VCSEL-based system with 10% overall power conversion efficiency and an output full angle divergence of 12 degrees.

Figure 3. Cross-section of a prototype to demonstrate z-axis stacking using VCSELs and HBT photoreceivers with integrated lenses.

A VCSEL TRANSMITTER ARRAY

As indicated, a VCSEL-based transmitter enables optical links with high efficiency and low cross-talk. In addition, VCSEL devices have shown high (10-14 GHz) modulation bandwidth [7] and can be designed for minimal sensitivity to ambient temperature excursions [8]. The VCSEL arrays being constructed for the

interconnect of Fig. 3 are 980 nm back-emitting InGaAs devices on GaAs substrates. The devices are gain-guided, with the active region defined by a surrounding ion implant. They are distributed in a 4 x 4 array pattern on 500 μm centers as in Fig. 4. The DC light-current-voltage characteristics of a typical device appear in Fig. 5. Here, the power conversion efficiency is better than 5 percent at an output power of 1.0 mW. Note that the drive voltages are typically less than 3 volts, while drive currents are less than 10 mA, thus enabling compatibility with direct 3.3V CMOS drivers. Similar, more optimized devices have exhibited 10% to 13% efficiency and more recent devices using oxidized layers for lateral confinement have shown efficiencies as high as 50% [9], though our present ZAPI power budget assumes simpler and more highly developed 10% efficient devices [10].

Figure 4. Top View of a 4 x 4 VCSEL array on 500 μm centers, designed for z-axis communication in MCM applications. Emission is through the bottom of the wafer.

Figure 5. DC light-current characteristic for a bottom-emitting 980 nm VCSEL. Wall plug efficiency for this device at a 1 mW output is 5%.

The VCSEL array was probe-tested at modulation rates equivalent to those encountered in a 100 MHz interconnect. Here, an equivalent 100 Mb/s signal was applied with pulse amplitudes similar to those expected from a CMOS driver. The voltage across the device was monitored with a high-impedance active probe. As shown in the dashed curve of Fig. 6a, the high level of the applied pulse train is near 3 V and the low level is 0.0 V (no DC bias on the device). These results for devices with a 20 μm emitting diameter indicate that the laser could operate at the required speeds.

If laser turn-on delay is too severe, the first few bits in a data stream might be lost after a long period of inactivity. In order to test for possible delay effects from thermal lensing in the VCSEL [11] devices were measured with a low duty cycle. Pulse monitoring delays were adjusted to zero under biased, constant lasing conditions. Relative delay was then measured for a 2 ms pulse period (with no DC bias) as in Fig. 6b, effectively eliminating any thermal lensing due to previous pulses. Here, the overall laser delay was approximately 1.0 ns as shown. Depending on applied pulse height, the delay varied between 1.0 and 1.7 ns. In this case, the applied pulse height of 3.8 V was considerably larger than that expected for CMOS drivers, and would correspond to much larger input currents than those displayed in Fig. 5. This was done to test the minimum obtainable pulse delay without a DC bias. As with the relatively high (30 mA) peak current corresponding to the voltage pulses of Fig. 6a, this large input pulse height also allowed the device to produce a discernable signal on our small area, unamplified monitor photodiode.

a. 50 % duty cycle operation at a 100 Mb/s equivalent rate

b. Single-pulse characteristic, showing 1.5 ns turn-on delay.

Figure 6. Tests of the gain-guided VCSEL light pulse modulation characteristic for low and high duty cycle.

The above tests indicate that the 20 μm diameter, gain-guided VCSEL devices should be able to operate at the speeds necessary for realization of this interconnect system. Smaller (10 μm) device diameters showed a strong thermal lensing effect that produced pattern-dependent turn-on delays, thus making them unsuitable for direct digital modulation.

In addition to the tests of Fig 6, other (top-emitting) VCSEL samples were wire-bonded and operated directly with 3.3 V CMOS buffers at 100 MHz. Simultaneous operation of up to 4 devices was demonstrated using the direct CMOS drive. Index-guided devices are also being constructed and will be demonstrated in a test link along with the gain guided- devices described above.

HBT PHOTORECEIVERS

As indicated in the interconnect cross-sections of Figs 2 and 3, the VCSEL transmitter devices feed signals to integrated photoreceivers. The photoreceivers to be used in this design are

based in HBT circuits, constructed on InP substrates. This allows for efficient light collection in an integrated p-i-n/HBT vertical structure, where the base-collector junction of the HBT can also be fabricated as a separate p-i-n photodetector.

Again referring to Figs 2 and 3, it is clear that the receiver substrates must be transparent for lens integration and back-side detection in the p-i-n detector. The semi-insulating InP:Fe substrates used will be transparent to the 980 nm light, as long as the iron concentration is not so excessive as to cause the InP absorption edge (at 960 nm) to have a long tail effect [12], [13]. Our measurements indicate that, at our chosen substrate thickness of 350 μm , the room-temperature light absorption in the substrate at 980 nm could range from 2% to 20%. At higher temperatures such as 75 C, this could range from 20% to 40%, making substrate pre-selection or thinning and remounting (as on GaAs) possible important factors for efficient link manufacture.

The photoreceiver circuit schematic appears in Fig. 7. It is a simple low-gain digital receiver designed specifically for low power consumption, 3.3V CMOS-compatible outputs, and optical inputs with near 1 mW peak pulse powers. The non-linear circuit response, which enhances data fidelity, requires the use of very high speed semiconductor transistors. The circuit was modeled using SPICE and was shown to switch with photocurrents as low as 100 μA . Transient analysis predicted <1.5 ns rise and fall times driving a typical CMOS 4 pF input load capacitance.

The photoreceiver circuits were laid out in a 4 x 4 pattern on 500 μm centers to match the laser array pattern of Fig. 4. They were fabricated in collaboration with Research Triangle Institute [14]. DC operation matched that predicted, showing a switching threshold with an optical power input of 250 μW (100 μA of photocurrent), and a high-level output of 2.7 V. The circuits were tested at speed, using a 980 nm laser input. Operation was demonstrated as in Fig. 9, where the receiver tracked 2 ns wide laser pulses at a 100 MHz repetition rate. The photocurrent pulses peaked at 500 μA (about 1.25 mW peak light input power). Testing speed was limited by the frequency response of the available 980 nm laser source, as indicated by the long tail in the response. This tail was also observed on fast photodiodes used to characterize our laser source. The required levels for 3.3 V CMOS operation were met (as indicated on the plot of Fig. 8), even though the circuit output was loaded by a 5000 Ohm probe impedance.

Figure 7. Circuit schematic for the HBT photoreceiver.

Figure 8. 200 Mb/s operation of the HBT photoreceiver. Long tails were the result of limited fall times on the test laser.

OPTICAL DESIGN AND LENS TECHNOLOGIES

In order to accommodate VCSEL divergence and re-focus of light to a 50 μm detector diameter, lenses are to be placed on the back sides of the VCSEL and HBT device substrates as in Fig. 3. An optical design for the demonstration link appears in Fig. 9, where the GaAs and InP device substrates have a thickness of 350 μm and are separated by up to 1200 μm to accommodate possible thicknesses of the silicon MCM substrate that forms the platform for level 2 of the stack. The first lens, formed on the back of the VCSEL substrate, is partially collimating, and thus limits the optical beam diameter at the receiver substrate. This design accommodates lens-to-device misalignments of up to 3 μm and level-to-level misalignments of 5 μm by the use of an oversized receiver lens. For shorter layer separation distances and tighter alignment tolerance, the receiver lens diameter may be reduced.

Figure 9 An optical design to connect the VCSEL to the photodetector in a Z-Axis Stack such as Fig. 3.

In the demonstration link array of Fig 3, the lenses will be realized using both refractive and diffractive lens technologies. A combination of both lens types will allow for maximum design latitude and efficiency in the advanced link cross-section of Fig. 2. In such an architecture, refractive lenses and/or gratings would be used on the VCSEL substrates to turn and collimate the beam; thus allowing upward transmission. Either the refractive or binary lenses may also be metal-coated as focusing mirrors and used with

a low-shadowing photodetector to form a Cassegrain receiver for top-side detection as in Fig. 2.

The diffractive or binary optic lenses are etched into the back of the VCSEL substrate with a 8 phase-level pattern as in Fig. 10a. They have been integrated with back-emitting VCSEL arrays, and have demonstrated effective collimation with a diffraction efficiency of 80% [15]. The refractive lenses are constructed by thermal flowing of a polyimide material as in Fig. 10b. They have also been integrated onto the back-emitting VCSELs, again collimating the beam to a divergence angle of 1 degree [16]. These structures have also been transfer-etched into GaAs for shorter focal length lenses.

a 8 phase-level binary lens.

b Refractive lens formed in polymer material on an etched pedestal.

Figure 10 Integrated lenses for VCSEL beam collimation.

PACKAGING

In many "chips first" modules, wells are cut or etched into the MCM substrate material [5]. Materials such as alumina or aluminum nitride are typically used for the MCM substrate [17]. In a stacked arrangement, silicon is a likely choice for the MCM substrate material, since it has reasonably good thermal properties compared to other candidate substrate materials. The thermal conductivity of silicon is 150 W/(m K) versus 170 W/(m K) for aluminum nitride and 17 W/(m K) for alumina [18]. Also, silicon is inexpensive and easily patterned using lithography, deposition, and etching.

The effectiveness of v-groove etching in Si for alignment of vertical photonic communication channels was previously demonstrated for a simple LED-based stack as in Fig. 11. Here, a 4 x 4 CMOS photodetector array is attached to a silicon submount. It was stacked with a correspondingly mounted LED using two layers of spacers having v-grooves etched on both sides. The stack maintained the necessary alignment over the layers of silicon [6].

Figure 11 Partial prototype of a test stack based on a silicon submount. Note the v-groove etched features which align spacers to the features on the silicon surface.

Though it is a wavelength at which silicon is opaque, the device constraints discussed previously drove this design to 980 nm. It follows that the Si MCM substrates must have optical via holes as shown in Figs. 2 and 3. In the silicon MCM substrates, these vias can be constructed by the use of laser-drilled holes. The laser drilling process, in particular, can create very precise holes with a high aspect ratio. Fig. 12 shows the cross-section of 2 mil (50 µm) holes that have been laser-drilled into a standard 25 mil silicon substrate [17]. This is well in excess of the aspect ratio required for the 150 µm aperture in the optical design of Fig. 9.

Figure 12 Laser-drilled via holes in Si allow for a high aspect ratio that can realize optical paths between layers in a z-axis stack.

The laser-drilled silicon MCM substrates that form the demonstration stack of Fig. 3 are to be assembled for testing as in Fig. 13. Here, the CMOS drivers, buffers, decoupling capacitors, and photonic devices will be placed into the two-layer stack, which will fit into a large-cavity (55 mm by 35 mm) PGA package for

operation in a standard digital tester. Intermediate tests on simpler silicon submounts will experimentally verify alignment tolerance and electrical drive requirements.

CONCLUSION

This photonic interconnection link will meet the requirements outlined above by the use of large numbers of parallel photonic channels. Transmitters are constructed from two-dimensional arrays of high-efficiency VCSELs that can be driven by CMOS with a minimum of external interface circuitry and electrical power. For this application, the VCSELs are designed to operate at a wavelength of 980 nm, which presently offers maximum performance. The GaAs VCSEL die are then also transparent to the light, allowing micro-optics to be integrated into the device substrates for beam collimation and/or redirection. The VCSEL devices have been demonstrated to operate at 100 Mb/s.

Figure 13 Prototype demonstration MCM stack with VCSELs, photoreceivers, drivers, and capacitors in a PGA package for testing.

The photonic data channels defined by the transmitter die are completed by the use of corresponding monolithically-integrated InGaAs Heterojunction Bipolar Transistor (HBT) photoreceivers, built on InP substrates. This choice of materials allows for efficient absorption of the 980 nm photons in a p-i-n photodetector structure that is vertically integrated into the HBT layers. Like the VCSEL, this photoreceiver design again makes use of substrate transparency, though iron doping in the semi-insulating InP may cause some optical losses. Collection micro-optics are integrated into the backs of the device substrates to focus the light beam and thus allow for small photodetector areas. The photoreceiver circuits are optimized for low power consumption, and have been demonstrated to operate in excess of 200 Mb/s. Digital data fidelity is achieved by matching the large optical power provided by the VCSEL-based transmitter with the non-linear receiver allowed by the very high speed HBTs.

Compatibility with MCM-based packaging is another important aspect of the use of photonic interconnections. This Z-axis interconnection approach makes use of emerging packaging techniques such as solder-bump bonding for alignment and laser drilling of via holes to allow for inter-layer communication within the stack. Since the optics are integrated into the photonic die, assembly and alignment is greatly simplified, thus helping to make the photonics more compatible with emerging MCM techniques. All of these factors will help to make photonics more attractive for use in a variety of interconnect applications, ranging from free-space data architectures to optical fiber-based data communication links.

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