NEW DEVELOPMENTS IN ELECTRICAL LINEWIDTH AND OVERLAY METROLOGY FOR ULSI FABRICATION PROCESSES


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1. Characteristics of Electrical Test Structures

Compared to other metrology approaches, electrical test structures for the measurement of dimensional characteristics such as linewidth and overlay directly relate to the electrical performance of the circuits being fabricated. In the case of linewidth, electrical metrology evaluates the part of a feature’s cross section that participates in electrical conduction. In contrast, optical or electron-beam-based metrologies provide values pertaining to that part which scatters photons or charged particles. The corresponding results may be within respective uncertainty ranges for nominal feature widths of approximately one micrometer or more. However, when nominal feature widths descend to deep submicrometer ranges, the different metrologies can generate substantially different results. Systematic metrology-dependent differences are said to constitute “methods divergence.” However, electrical methods, when applicable, tend to exhibit measurement uncertainties less than those of all other techniques.

The inherent disadvantage of electrical techniques is that they can be applied only to the extraction of the dimensions of features patterned in electrically-conducting materials. They cannot be directly applied to patterned resist films or dielectric material layers. In the case of narrow on-wafer features patterned in resist, for example, linewidths are preferably extracted by electron-beam methods. These methods are sufficiently repeatable for monitoring fabrication-process variations. However, the traceability of the units in which linewidth is expressed is thwarted by the unavailability of suitable calibration artifacts.

In the case of overlay metrology, the same limitations as regards electrical conduction apply. However, similar advantages accrue in principle to electrical overlay methods when they can be utilized. It is the electrical quality of the overlay of a conducting via relative to underlying or overlying conducting material which is of driving importance for circuit functionality. This may differ from the overlay values extracted from the same patterns by commonly-used optical overlay tools.

Further refinements in the state of the art in both electrical linewidth and electrical overlay metrologies are desirable as feature sizes and spacings continue to shrink in emerging generations.
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2. Growing Challenges in Linewidth and Overlay Metrology

Measurements of the linewidths of features below about 0.25 micrometer are particularly subject to unacceptable levels of methods divergence. This generates two classes of problem. The first is the unreliability, attributable to methods divergence, of measurements conducted by any one method. Electrical methods, while offering the lowest overall uncertainties and while being directly related to the physical quantities of interest, tend to be among the methods showing the greatest overall divergence from other methods. The second class of problem is certifying the linewidths of features on reference materials for linewidth-instrument calibration. Ideally, a reference material feature should be certifiable by multiple linewidth-measurement methods and be applicable to the calibration of instruments of multiple kinds. Currently, such a requirement is not met in practice.

One source of methods divergence in linewidth metrology is the unavailability of a universally-accepted definition of the linewidth of a feature having an arbitrary geometrical cross section and material non-uniformity. Different linewidth metrologies generally report the dimensions of different properties of a given feature. Secondly, as a consequence of the adverse impact of methods divergence on the availability of calibration artifacts, traceability of the units in which linewidth is expressed by a particular instrument is compromised. These two deficiencies impede the development of linewidth metrology for deep submicrometer features.

Electrical test structure innovations have recently been introduced to address problems in overlay metrology that are growing in importance as downward scaling of device dimensions continues. The impact of tool-induced and wafer-induced shifts make relating overlay values extracted by optical tools to the electrical integrity of the circuitry being fabricated of increasing importance. As in the case of linewidth metrology, certified reference materials are unavailable.

The increasing popularity of chemical-mechanical polishing is presenting a serious challenge to overlay extraction from some layers because inspection targets are rendered invisible by the planarization process. A new class of electrical test structures is being evaluated that has the potential of replacing optical instruments for such applications. However, the principle subject of this paper is the fabrication and utility of reference materials, and related target-design enhancements, to support overlay-metrology development rather than hardware innovation.


The principles of fabricating features in bulk silicon having sub-nanometer surface planarity and smoothness, and lattice-determined sidewall slopes, have been recently adopted from Micro-
Electro-Mechanical Systems (MEMS) technology. Earlier this year, the concept of combining MEMS and Silicon-On-Insulator (SOI) technologies was introduced at NIST to provide reference-material architectures which address the limitations imposed by methods divergence on linewidth reference-material certification and utilization as described above.\(^1\) This innovation allows electrical metrology and inspection of the same feature by transmission optical and electron-beam techniques. In other words, with the single-crystal architecture, both certification and application are fully compatible with multiple metrology techniques. In addition, the same architecture offers potential opportunities for shift management in overlay metrology.

A limitation of growing seriousness in electrical measurement of deep submicrometer linewidths is the standard practice of providing Kelvin voltage-tap widths commensurate with the subject linewidth. For the purpose of minimizing systematic errors arising from the finite extent of as-replicated tap widths in the standard electrical linewidth structure, bridge lengths are extended and tap widths are commensurately reduced to submicrometer widths. The new SOI implementation, however, results in a structure which is robust to manufacture and less vulnerable to the impact of bridge/voltage-tap junction inside-corner rounding. It has multiple very short bridge lengths and no limitations on permissible drawn tap widths. Figure 1 shows the schematic of a structure which is designed for replication in (110) SOI by potassium-hydroxide based etching and provides single-crystal features with vertical sidewalls. Scanning electron micrographs of portions of the first structures of this type ever made are now available. Linewidth measurements extracted electrically from these structures indicate that the essential buried-oxide insulating requirement is satisfied and that the structures exhibit completely nominal electrical behavior.

Because of the unique attributes of the single-crystal MEMS-SOI approach, there is a unique opportunity for fabricating structures which may be electrically certified and used for extracting tool-induced shift from optical overlay instruments used for applications in which wafer-induced shifts prevail.

4. Hybrid targets for On-substrate Overlay Metrology

Figure 2 shows a new hybrid structure which is patterned in an amorphous or polycrystalline conducting film to allow the comparison of overlay measurements extracted from the same features by optical and electrical techniques respectively. For the purposes of simplicity, a one-dimensional version derived from a standard bars-in-bars target is shown. Figure 3 shows how measurements by the two respective techniques compare typically to within several nanometers for programmed overlays ranging from -60 nm to +60 nm. The slight deterioration of the agreement at the smaller linewidth design rules is attributed to exceeding the operating specifications of the tools used to execute the double-reduction technique employed to generate the very small programmed overlays. This work was undertaken to take a first look at the
The potential precision of electrical techniques for extracting overlay values unaffected by shifts in the sub-50-nanometer region. It is possible that the structure will have applications in pixel calibration and overlay extraction from targets that are partially obscured optically.

As emphasized previously, electrical test structures for the measurement of overlay directly relate to the electrical integrity of the circuits being fabricated. However, so far, electrical structures for the evaluation of overlay between vias and patterned conductor levels, for example, have not demonstrated resolution of the optical methods. However, the latter are generally vulnerable to shift. This paper reports an entirely new approach to the utilization of electrical techniques for extracting the extent to which optical overlay measurements are affected by tool-induced and process-induced shifts. The performance has been simulated and provisionally shown to be capable of performance at better than 2.5-nm when fabricated with typical state-of-the-art lithographic tooling.

5. Summary

Electrical test structures for the measurement of dimensional characteristics such as linewidth and overlay directly relate to the electrical performance of the circuits being fabricated and exhibit measurement uncertainties less than those of other techniques. However, they tend to exhibit the greatest overall divergence from other methods. The concept of combining MEMS and Silicon-On-Insulator (SOI) technologies was introduced at NIST to provide reference-material architectures which address the limitations imposed by methods divergence on linewidth reference-material certification and utilization. This innovation simultaneously allows electrical metrology and inspection of the same feature by transmission optical and electron-beam techniques and others. In other words, with the single-crystal architecture, both certification and application are fully compatible with multiple metrology techniques. In addition, the same architecture offers potential opportunities for shift management in overlay metrology. An essential requirement of the MEMS/SOI implementation is that the implanted or bonded silicon dioxide layer have electrical insulation sufficient to withstand the stresses of electrical testing. A preliminary selection of measurements has demonstrated that this requirement is met. A new hybrid optical-electrical overlay test structure which is replicated in single-crystal or amorphous/polycrystalline materials provides electrical and optical overlay measurements which agree to within several nanometers over a range of programmed overlays from -60 nm to +60 nm. Finally, a new process-compatible overlay structure for electrical evaluation of overlay between vias and patterned conductor levels has been simulated and provisionally shown to be capable of performance at better than the 2.5-nm level.
References


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Figure 1. Schematic of a linewidth structure designed for replication in (110) SOI by potassium-hydroxide based etching and providing single-crystal features with vertical sidewalls.

Figure 2. A new hybrid structure which is patterned in a single conducting film to extract overlay measurements from the same features by optical and electrical techniques respectively. (The lower part of the figure is an enlarged representation of the active region of the structure shown above.)

Figure 3. Measurements extracted electrically from hybrid overlay structures with programmed overlays ranging from -60 nm to +60 nm. (The dimensions in micrometers above each chart are the respective structure's feature linewidths.)