Title: High-Resolution Transmission Electron Microscopy Calibration of Critical Dimension (CD) Reference Materials

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Abstract - NIST and Sandia have developed a procedure for producing and calibrating critical dimension (CD), or linewidth, reference materials. These reference materials will be used to calibrate metrology instruments used in semiconductor manufacturing. The artifacts, with widths down to 100 nm, are produced in monocrystalline silicon with all feature edges aligned to specific crystal planes. A two-part calibration of these linewidths is used: the primary calibration, with accuracy to within a few lattice plane thicknesses, is accomplished by counting the lattice planes across the sample as-imaged through use of high-resolution transmission electron microscopy (HRTEM). The secondary calibration is the high-precision electrical CD technique.

NIST and Sandia are developing critical dimension (CD), or linewidth, reference materials for use by the semiconductor industry. To meet the current requirements of this rapidly changing industry, the widths of the reference features must be at or below the widths of the finest features in production and/or development. Further, these features must produce consistent results no matter which metrology tool (e.g., scanning electron microscope, scanned probe microscope, electrical metrology) is used to make the measurement. This leads to a requirement for the samples to have planar surfaces, known sidewall angles, and uniform material composition. None of the production techniques in use in semiconductor manufacturing can produce features with all these characteristics. In addition, requirements specified in the National Technology Roadmap for Semiconductors indicate that the width of the feature must be accurately calibrated to approximately 1-2 nm, a value well beyond the current capabilities of the instruments used for semiconductor metrology.

Since current processes used for semiconductor device fabrication cannot produce features with these requirements, an approach utilizing features processed from monocrystalline silicon has been developed. Monocrystalline silicon allows for lattice-plane selective etch processing that produces features which are roughly aligned to the mask but are aligned exactly to the silicon crystal lattice plane. These etch techniques, commonly associated with the processing of

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MicroElectroMechanical Systems (MEMS) devices, are capable of providing features with atomically planar surfaces and crystallographically-defined sidewall angles. A selection of reference features of different widths was assembled into a 10 mm square test chip. This test chip was patterned into BESOI (bonded and etched-back silicon-on-insulator) substrates. BESOI features a buried SiO₂ layer below the top surface, to provide electrical isolation as well as an etch stop. Since BESOI’s buried oxide is produced thermally, before bonding, there is a sharp interface between the surface silicon and the buried oxide. The reference features described in this paper have {110} top and bottom surfaces and edges aligned to the {111} planes along <112> directions. Thus, the sidewalls intersect the surface orthogonally and each other at 70.529 degrees.

The calibration procedure consists of two measurement techniques: high-resolution transmission electron microscopy (HRTEM) and electrical probe. These techniques will complement each other since electrical metrology is fast, precise, and non-destructive while, in contrast, HRTEM metrology is slow, accurate, and destructive. The first measurement of each structure to be calibrated is electrical measurement of the width. The electrical measurement of the bridge width is performed using the short bridge resistor variant of the cross-bridge resistor. The cross bridge resistor combines a van der Pauw cross, from which the sheet resistance of the conductor is determined, with a bridge resistor, from which the linewidth is determined. The short bridge contains additional features from which the effects of non-zero-width voltage taps are eliminated.

After all samples on the wafer are measured electrically, a number of the CD reference features is selected for calibration of the width with respect to the atomic lattice via HRTEM. To be able to resolve the lattice fringes using HRTEM, and thus measure the width of a feature, the thickness of the sample must be reduced to approximately 20 nm. The edges are protected during this thinning process by a TEOS (tetraethoxysilane) oxide, which is deposited before thinning. After the oxide is deposited, the top surface is polished until the middle of the silicon line is reached. A 2 mm x 2 mm square, centered on feature, is then remove from the chip and the back surface is ground back to a thickness of 100 μm. Next a dimple grind and polish from the back surface thins the feature to approximately 3 μm. Finally, Argon ion milling from the back surface is then used to thin the sample to approximately 20 nm. The HRTEM was performed at 300 kV in a Philips CM30 twin-lens TEM with a LaB₆ source. The sample was oriented so as to excite only the 111-systematic row corresponding to the set of {111}-planes that lie parallel to the line direction (i.e. no cross-fringes in the image).

An example of an HRTEM-imaged line is shown in Figure 1. At this magnification one can see the entire line width, but not the lattice fringes. An enlargement of a portion of this image at the left edge of the line is shown in Figure 2 where one set of {111} lattice-plane fringes is clearly visible. To determine the CD from this image, a procedure was developed wherein the 3.25"x4" negative is digitized at 3000 dpi and the fringes are identified and counted using image processing techniques. The image shown in Figure 1 was photographed at 120 kx magnification in the HRTEM so that 1 mm on the negative equals 8.33 nm and contains approximately 26 (111)-lattice fringes. At 3000 dpi, this equates to approximately 4.5 pixels per fringe. From a region of this digitized image, a profile can be taken showing the locations of the fringes. To ease counting of the fringes, the profile can be differentiated to highlight the fringes. Figure 3
shows the profile before and after differentiation. The fringes were counted and the width of the line was determined to be 582.91 nm.

The uncertainty associated with this calibration procedure has been estimated. For the HRTEM, there are two potential contributions to the uncertainty: the uncertainty in the value of the lattice-fringe spacing and the uncertainty in the lattice-plane count in the transition region between the feature and the TEOS oxide. The lattice constant of silicon is \(0.54310196 \pm 0.00000011\) nm.\(^9\) Since silicon crystallizes in a diamond lattice, the spacing between the (111) planes when viewed from the (110) surface is \(0.31356006 \pm 0.00000006\) nm per fringe. Since 1859 fringes were counted across the feature, the uncertainty in the width measurement due to the uncertainty in the silicon lattice constant is \(0.0001\) nm. For this sample, neither the doping nor the thickness of the thinned film is expected to have a significant effect on the lattice constant. The second source of uncertainty is the transition from the single-crystal silicon to the TEOS oxide. This has been estimated to be less than two lattice planes per edge or an upper limit of 1.25 nm. Therefore, the combined standard uncertainty, with coverage factor \(k = 2\) to provide a conservative upper bound,\(^{10}\) is 2.50 nm.

Transferring the calibration from the HRTEM to the electrical measurement introduces additional uncertainty based on the electrical CD measurements. Since the electrical measurements will be calibrated as an offset from the as-measured electrical CD, only random sources of error need be considered. There are two sources of uncertainty in the electrical measurement. The first is in the lengths of the bridges, which act as the "ruler" for the electrical CD measurement. The lengths of the bridges can vary from structure to structure due either to feature misplacement on the photomask or magnification errors when the features are transferred from the photomask to the wafer. The second source of uncertainty in the electrical measurements is random variations in the electrical measurements; that is in the actual measurements of voltages and currents.

To determine the uncertainty in the width measurement due to the length of the ruler, samples were measured with the NIST Linescale Interferometer\(^{11}\) to determine the range of values that would be expected for this process. The random uncertainty in the length of a feature is less than 1%. If the particular line is measured by an accurate tool, such as the NIST linescale interferometer, this uncertainty in the width due to the voltage tap spacing is reduced to 0.06%.

The applicable uncertainties associated with electrical measurement are random variations in the as-measured currents and voltages used to determine the sheet and bridge resistances. These have been estimated to have an upper limit of 0.03% using instrument specifications and representative measurements. Totaling these uncertainties, the combined uncertainty is 7.1 nm (again, with a coverage factor of \(k = 2\)) for the case where the bridge length is not measured and a combined uncertainty of 5.2 nm (\(k = 2\)) where the bridge length is known.

The uncertainties associated with the different elements of the measurements are summarized in Table 1.
Table 1. Uncertainties associated with the different width measurements

<table>
<thead>
<tr>
<th>Measured Quantity</th>
<th>Uncertainty Source</th>
<th>Uncertainty Value, $\Phi_i$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HRTEM</td>
<td>Silicon Lattice Constant</td>
<td>0.0001</td>
</tr>
<tr>
<td></td>
<td>Fringe Count at Edges</td>
<td>1.25</td>
</tr>
<tr>
<td></td>
<td>Combined standard uncertainty, $2 \sqrt{\sum \sigma_i^2}$</td>
<td>2.50</td>
</tr>
<tr>
<td>ECD (average conducting path width)</td>
<td>Sheet Resistance</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>Bridge Resistance</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>Length (unmeasured)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>Combined standard uncertainty, $2 \sqrt{\sum \sigma_i^2}$</td>
<td>7.1</td>
</tr>
<tr>
<td></td>
<td>Length (measured)</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Combined standard uncertainty, $2 \sqrt{\sum \sigma_i^2}$</td>
<td>5.2</td>
</tr>
</tbody>
</table>

We have demonstrated both the use of HRTEM for primary calibration of CD reference artifacts and a path for providing low-cost CD artifacts by electrical calibration. In order to demonstrate the robustness of the technique we chose as our initial device a feature with a worst case linewidth of 600 nm. Narrower samples will allow for higher HRTEM magnification and thus better resolution and easier counting of the $\{1\ 1\ 1\}$ planes. Work is underway to refine the chip fabrication and measurement processes and complete the statistical analysis needed to fully characterize the features which would make up the calibration standards.

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References:
Figure Captions:

Figure 1. HRTEM image of a segment of [110]-oriented line

Figure 2. Enlarged view of edge of silicon line showing the locations of the silicon lattice planes

Figure 3. Profile of silicon line edge after digitization and differentiation. Each peak is produced at a (111) silicon lattice plane.


Figure 1
Figure 2
Figure 3