Advanced Semiconductor Detector
Development:
Development of a Room-Temperature, Gamma
Ray Detector Using Gallium Arsenide to
Develop an Electrode Detector

prepared by

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THE UNIVERSITY OF MICHIGAN
PRINCIPAL INVESTIGATOR: PROFESSOR GLENN F. KNOLL

1. PROJECT OVERVIEW

The general objective of this project is to advance the development of room temperature semiconductor detectors of ionizing radiation. At the present time, devices fabricated from wide bandgap materials that can be operated without cooling suffer from relatively poor energy resolution and are limited to very small volumes. The difficulties arise largely from the poor mobility of positive charge carriers (holes) that is quite generally observed in compound semiconductor materials. The initial emphasis of our project has been to develop techniques that can overcome some of the limitations normally observed because of this poor hole transport.

Our initial efforts have concentrated on three different device configurations that offer the possibility of overcoming limitations set by poor hole transport. These three configurations are the buried grid-single carrier device (BG-SCD), the trench single carrier device (TSCD) and devices using patterned coplanar electrodes. The first two of these configurations are being fabricated using high resistivity silicon to take advantage of the highly developed processing technology available in silicon. They will be constructed as proof-of-principle devices to demonstrate whether true single carrier response can be achieved. If either or both of these configurations are successful, we will then explore extension of these technologies to wide bandgap semiconductor materials that can potentially be operated at room temperature with large volumes. The third approach of patterned electrodes is being pursued using CdZnTe, one of the materials that is a candidate for large volume room temperature detectors.

In addition to our work in the laboratory, we have also been providing technical support for several activities at the request of Dr. Karl Reinitz. The first of these is participation in the preparation of a report on "Fieldable Nuclear Detectors" currently being supervised by Dr. Charles Dickerman of Argonne National Laboratories. Professor Knoll attended a planning meeting at Department of Energy (DOE) Headquarters in Washington at which preliminary objectives and plans for this report were formulated. He subsequently hosted a visit by Dr. Dickerman to the University of Michigan, at which time tasks were defined for the preparation of the report. Professor Knoll provided a written contribution in two areas: an analysis of the most significant technical developments reported at the 1994 IEEE Nuclear Science Symposium, and a supplemental critique of other advanced technologies that could contribute in both the short and long term to useful devices. These sections have subsequently been incorporated into the final draft of the report. A second area of technical support has been Professor Knoll's service in connection with the "Uranium Transparency" project. He has attended two meetings in 1995 at DOE Headquarters in Germantown, and is serving as a member of a panel chaired by Dr. Hap Lamonds that is evaluating proposals submitted by DOE contractors.

2. PROJECT PERSONNEL

The work described in this progress report has been carried out with participation of the following personnel from the University of Michigan

- A. Professor Glenn F. Knoll, Principal Investigator
- B. Professor David Wehe, Faculty Participant
- C. Zhong He, Post-doctoral Fellow
- D. Ronald A. Rojeski, Graduate Research Assistant

In addition, consultations have been held with a number of individuals regarding semiconductor processing steps, including Professor Fred Terry.

3. TECHNICAL DETAILS

In the two sections that follow, we outline the progress that currently has been achieved in the technical tasks outlined above. We have been investigating the processing steps that are necessary to produce a buried grid-single carrier device, we have taken one batch through the complete cycle of cleaning, oxidation, alignment etching, implantation, diffusion, back etching, and attachment of electrodes. Initial tests have shown excessive leakage current that has prevented a successful demonstration of single carrier behavior with this first prototype. We are therefore carrying out some diagnostics to try to pinpoint the origin of the leakage, and are modifying the processing steps to avoid some unexpected difficulties that were experienced with several of the processing steps. As we gain experience, we hope to avoid these difficulties and to be able to demonstrate signals that are derived almost exclusively from the motion of holes in silicon. For the trench single carrier device, we have completed a set of specifications for the design, and are contracting for the electron cyclotron resonance etching at an off-campus facility. Once this etching has been carried out, we will then complete the fabrication by attaching electrodes and initiate a testing program. For the pattern contact approach, we have obtained a sample of CdZnTe and fabricated our first test device. While this prototype operates as expected as a conventional detector with all strips interconnected, we are as yet unable to test it as a single carrier device since the surface resistivity between adjacent strips is not sufficiently high. We have therefore contracted with Aurora to supply us with three different CdZnTe detectors made to our design. Each of these employs a different choice of electrode patterns and includes both one-sided and two-sided fabrication. We are assured by Aurora that their proprietary fabrication methods will achieve the needed surface resistivity to allow an evaluation of these designs. To allow application of these devices, we have also designed, built, and tested a special preamplifier capable of producing a differential output that is needed to produce the single carrier response.

We have also carried out a theoretical study of the patterned electrode approach. We have been successful in deriving an analytical solution to predict the pulse behavior of these devices and details are given in the following sections. It should be pointed out that this is the first known analytical solution to this problem, and all previous analyses have been carried out using finite element numerical solutions. The analytical result allows a better understanding to be developed of the conditions under which single carrier behavior should be expected.

Attached are two technical sections that provide details on our single carrier work. The first (prepared by Ronald A. Rojeski) gives details on the semiconductor processing that is relevant to both the BG-SCD and TSCD. The second (prepared by Zhong He) gives details of the analytical study underlying the patterned electrode approach, and suggests its generalization to pixellated devices.

Semiconductor Processing

The following describes the processing steps performed for fabrication of three different structures that act as single carrier devices. Two of the device geometries explored are fabricated with silicon. These two structures are the **Buried Grid - Single Carrier Device** and **Trenched Single Carrier Device**. Both of these devices rely on the same principle as a gridded ionization chamber to achieve single carrier charge collection. Of these two, only the BG-SCD has been fabricated. The third device, a coplanar interdigitated electrode structure, is fabricated on CdZnTe. This structure achieves "unipolar sensitivity" by taking advantage of electrode geometries and implementing additional electronics. This is the only device that has been demonstrated to work at this time.

The general considerations for processing silicon center around surface preparation. Associated with this are initial cleaning steps, dicing, packaging, and mounting of the silicon device. Specific to fabricating the BG-SCD, the general processing steps are (see Figure 1):

- 1) Oxide encapsulation
- 2) Alignment etch
- 3) Implantation
- 4) Diffusion
- 5) Epi-growth
- 6) Etch back
- 7) Contact deposition
- 8) Mounting

For the TSCD, the general processing steps are (see Figure 2):

- 1) Oxide encapsulation
- 2) Nickel deposition
- 3) ECR trench etch
- 4) Contact deposition
- 5) Mounting

Naturally, there is some overlap between both processes. The overlap is associated with cleaning procedures, dicing and mounting.

The processing associated with CdZnTe is very specific and not well understood. Therefore, it will be considered after silicon processing is discussed.

General Process Considerations for Silicon

The cleaning of all silicon pieces followed this recipe:

- 1) DI rinse
- 2) TCE rinse
- 3) Methanol rinse
- 4) ACE rinse
- 5) IPA rinse
- 6) DI rinse

Each step was performed for at least five minutes in an ultrasonic bath. The above steps must be followed in order, so that the creation of thin organic films is minimized. (Note that IPA dissolves ACE, ACE dissolves Methanol, and Methanol dissolves TCE.) The samples are placed in the ultrasonic bath to liberate any particles that were created during dicing of the completed silicon substrates.

To properly prepare the surface of the silicon, a CP4A etch is recommended. This is a non selective silicon etch used to create a semi-polished surface; under a microscope, it appears as an orange peel texture. The composition of CP4A (by volume) is:

3 HF, 5 HNO₃, 3 acetic (25μm/minute)

Two other available etches are CP4 and a planarizing etch. Their composition (by volume) is:

CP4: 3 HF, 5 HNO₃, 3 acetic, 0.06 bromine (32μm/minute)

Planar: 2 HF, 15 HNO₃, 5 acetic (3.5-5.5μm/minute)

(49% HF, 70% HNO₃, glacial acetic (100%))

The purpose of using these HF-Nitric solutions is to remove any surface contaminants that may be present after cleaning. As with most HF-Nitric etches where there is an approximately equal volume of HNO₃ to HF, best results are obtained when the etch is diluted with DI and aspirated away before removing the samples. This helps to minimize staining and burning of the silicon surface.

Dicing was performed with a diamond saw that was available outside a cleanroom environment. Therefore, great care must be taken to maintain clean samples upon reentry to the clean room environment. The cleaning steps given above, in addition to the HF-Nitric etches are strongly recommended to maintain cleanliness.

The final devices are mounted in boron-nitride packages. This material was chosen because of the high resistivity of the material (in excess of 10^{16} ohm-cm). The devices are bonded to the boron nitride with a high resistivity epoxy that is doped with boron nitride. Caution must be used in choosing the epoxy so as to minimize possible contamination and/or corrosion from the solvents present in the epoxy.

Processing BG-SCD

The formal steps necessary for fabricating the BG-SCD were given previously. They are explained in turn below.

Oxide Encapsulation

This is the first step necessary to fabricate the BG-SCD. The oxide is grown in a high temperature furnace ($>1100^{\circ}\text{C}$) with water vapor flowing at a controlled rate. The water vapor reacts with the surface of the silicon, producing an oxide. The purpose of this oxide is to act as a protective layer for all subsequent processing steps; this is necessary because these samples use both sides of the substrate as an active part of the device.

Alignment Etch

An alignment etch is performed so that it is possible to align to the buried contact layer after epi-growth. Due to the presence of the potassium ion in the etch, it must be performed prior to all other processing so as to allow thorough cleaning of the substrate. If this were not done, the ionic

contamination would render useless all MOS devices fabricated within the cleanroom. The composition of the KOH etch is:

63.3 ml. DI H₂O
23.4 gm. KOH
13.3 ml. IPA

The etch temperature is 84C, with an etch rate of 1.1 $\mu\text{m}/\text{min}$ for $\langle 100 \rangle$ silicon. The etch ratio between the $\langle 100 \rangle$ and $\langle 111 \rangle$ planes is about 400:1, which gives the appropriate sidewall angle of 54.75° . Since this etch is used only for the generation of alignment marks, poor sidewall geometry is of no consequence

Implantation

Boron is implanted into the silicon sample to create gridlines as previously described for this structure. Typical energies for this step are in the range of 100 - 180keV, with a dose in the range of 10^{13} atoms/cm². This will give a doping concentration in the range of 10^{17} atoms/cm³. Note that after implantation, an activation step must be performed to electrically activate the dopant. Typical temperatures used were 1150C for 10 seconds in an argon ambient.

Diffusion

To create the high concentration of boron necessary to act as a contact/etch-stop, diffusing the dopant species is required. This step is carried out in a high temperature furnace. The furnace run lasts about five hours; the initial temperature at ramp-up is 600C, with a temperature ramp of 5C/min. Deposition time is 10 minutes, and occurs at 1150C. Ramp down is -5C/min until 600C is reached. The samples are then removed.

Epi-growth

The epitaxy layer grown for the BG-SCD was not performed in house. The final parameters for the grown material are a thickness of 20 microns with a measured resistivity $> 100 \text{ ohm-cm}$.

Etch back

Etch back to the boron contact ring was initially attempted with EDP (EthyleneDiamine Pyrocatechol). This etch displays strong selectivity against highly doped boron regions in silicon. The etch rate at 115C is about 0.8 microns/min for $\langle 100 \rangle$ silicon; the etch ratio between $\langle 100 \rangle$ and $\langle 111 \rangle$ planes is in the area of 17, and can be altered by changing the concentration of pyrocatechol. Therefore, it was thought to be an appropriate etch to open contact to the buried boron layers. For reasons not yet understood, the EDP solution did not attack the bulk epi layer. TMAH (TetraMethyl Ammonium Hydroxide) was thus chosen. The etch rate of TMAH is 0.9 microns/min for $\langle 100 \rangle$ silicon at 90C, with an etch ratio between the $\langle 100 \rangle$ and $\langle 111 \rangle$ planes of about 50. TMAH also displays very strong selectivity against highly doped boron regions, so stopping on the buried boron layer is not problematic. With the larger etch ratio, though, the sidewalls of the structure become more pronounced, making it difficult to contact the buried ring and the N^+ region with a single evaporation.

Contact Deposition

Contact deposition for the backside of the BG-SCD was performed by evaporation. Gold was used as the evaporating material. Aluminum was used to contact the buried grid and N^+ region, originally intended to be performed with a single evaporation. Because of more pronounced sidewalls, the regions short together. To remedy the situation, a timed

aluminum etch was performed to remove the sidewall coverage present. This does not correct for the possibility, though, that a silicon-aluminum alloy is created that effectively shorts the two regions together, even after the sidewall aluminum is removed. Other methods of contact deposition to avoid sidewall coverage are being explored.

Processing TSCD

The formal steps necessary for fabricating the TSCD were given previously. They are explained in turn below.

Oxide Encapsulation

This was explained in the process describing the BG-SCD fabrication.

Nickel Deposition

The purpose of nickel deposition is to act as a masking layer for the ECR trench etch. Due to the nature of ECR etching, metals are really the only viable mask available. Nickel happens to be the best metal mask for fabricating the trench structure.

ECR Trench Etch

ECR (Electron Cyclotron Resonance) is a plasma etching system that displays a very high degree of anisotropy; making it very well suited for etching a trench type structure. The sidewall profile can be controlled to the point where vertical sidewalls can be achieved. It is also possible to create an etch profile where the etch hole is smaller in width than the bottom of the trench itself, creating a "dovetail". This characteristic creates a self-aligned process, lending itself very well to contacting two regions of a bulk device with a single evaporation. Etch depths of over 50 microns can be made in silicon, with an aspect ratio greater than ten, without measurable deviation from vertical sidewalls. The current geometries that

will be fabricated are a line width and spacing of 20 microns and 30 microns, with an etch depth of 40 microns.

Contact Deposition

After the trench etch is performed with the ECR, an HF-Nitric dip is recommended to prepare the surface for contact deposition. With the proper etch profile (vertical sidewall or greater), there is no danger of shorting between the two regions, as is present with fabricating the BG-SCD. To reduce the dark current between the peak and valley of the trenches, gold is the suggested contact material.

Processing CdZnTe

Processing CdZnTe can be broken down into three areas. They are:

- 1) Maintenance of surface cleanliness
- 2) Deposition of desired electrode geometry
- 3) Mounting of CdZnTe

What is known about processing this material has been suggested, but not necessarily verified, by those working in industry.

Surface Cleanliness

It has been recommended that no solvent other than methanol be used to clean the surface of CdZnTe. No reasons have been given as to why. Just prior to electrode deposition, a etch for about 5 minutes is suggested by others in a 5% bromine/methanol solution. The reason for this is unclear, as the surface etch pit density does increase after this step. As soon as the etch-clean is performed, electrode deposition should occur immediately. The reason, it is supposed, is to avoid the formation of an oxide between the electrode material and the CdZnTe.

Deposition of Electrode

The method developed for electrode deposition relies on fabricating shadow masks of appropriate geometries from a polyimide. A polyimide can be thought of as a very thick photoresist that can be used as a structure itself, because of its high degree of cross linking upon exposure and baking. Taking advantage of this, it becomes possible to make physical structures of polyimide with fairly small features, such as a shadow mask. Shadow masks were fabricated from Probimide 7020, a commercially available polyimide. The final thickness of the polyimide was measured to be 15 microns. The structure created was a negative of coplanar interdigitated electrodes with a line width and spacing of 100 microns. The shadow mask was placed directly onto the sample, held in place by photoresist. 2000 angstroms of gold was evaporated onto the CdZnTe. The shadow mask was removed by a rinse in ACE and IPA.

Mounting of Sample

Due to many unknowns associated with processing CdZnTe, it is suggested that mechanical mounting only be used to mount these devices.

Other Considerations

The following is a list of commercial recommendations to achieve the best results.

- 1) No high temperature steps greater than 75C
- 2) A mid-temperature bake should be performed in ambient at 55C for 24 hours to insure good contact formation
- 3) Sputtering of the contact material should be performed; note, though, that good contact formation will be highly dependent upon the type of gas, gas flow rates, DC bias level, and RF power

Single Carrier Device Process Flow - Buried Structure

Encapsulation of wafer
with silicon dioxide

Pattern and etch
alignment marks; regrow
encapsulation layer

Pattern grid lines; perform
first implant (P+)

Pattern contact ring;
perform diffusion (P+)

Strip top encapsulation
layer; grow 20 microns
high-resistivity epi; grow
thin layer N+ material

Pattern epi layer for
selective etch to P+
contact ring; implant P+
backside; evaporate Al
contacts and wirebond

FIGURE 1

Single Carrier Device Process Flow - Trench Structure

FIGURE 2

First Progress Report on Room-Temperature Semiconductor Detectors

(1) Theoretical Approach

Semiconductors having high atomic numbers and wide band-gaps have long been under development as potential room-temperature γ -ray detectors. Among those, HgI_2 , CdTe and CdZnTe detectors have attracted most of the attention. Although these semiconductors have been successfully employed in various applications, the widespread use of these devices has been hindered by their charge trapping and polarization problems. Continuing effort has been given to improve the characteristics of the materials, but the energy resolution achieved using conventional planar electrodes is still far worse than what people could expect. Good energy resolutions were obtained by applying different signal processing techniques at the expense of complexity of the electronic system or severe loss of detection efficiency. Recently, significant progress has been reported by Luke [1, 2] which could lead to a major change in the design of readout systems of room-temperature semiconductor detectors. Luke's method is based on the principle of Frisch Grids [3] commonly employed in gas ion chambers, but uses parallel coplanar strip electrodes. The strips are connected in an alternate manner to give two sets of inter-digital grid electrodes. By reading the difference signal between these two sets of electrodes, pulses induced by one type (electrons or holes) of charge carriers can be obtained. For commonly used semiconductor detectors, signals from electrons produced by γ -ray interaction can be picked out so that the hole trapping problem can be eliminated. Following Luke's work, Barrett et al. [4] have suggested that the single-polarity charge sensing can also be approached by segmenting one side of conventional planar electrodes into small elements to form a 2-D electrode array, and to read signals individually from each of the square electrode pixels.

We have obtained the analytical form of the field distribution for more generalized configuration of coplanar strip electrodes. The results can be easily extended for 2-D segmented electrode arrays. This analysis could help to have a better insight into the configuration of the electric field within the detector and provides a simpler method for calculating both the operating field and weighting field potentials. Therefore, the induced charge on corresponding electrodes as a function of time can be easily estimated.

The section view of a Luke's device is shown in Fig.1 and the corresponding potential distribution $\varphi(x, y)$ within the detector can be described by the following equation:

$$\varphi(x, y) = a_0 \cdot \left(\frac{y}{D}\right) + \sum_{n=1}^{\infty} a_n \cdot \cos \frac{2\pi n}{P} x \cdot \left(\frac{\sinh \frac{2\pi n}{P} y}{\sinh \frac{2\pi n}{P} D}\right) \quad (1)$$

$$a_0 = \frac{1}{P} \int_0^P \varphi_D(x) dx \quad a_n = \frac{2}{P} \int_0^P \varphi_D(x) \cdot \cos \frac{2\pi n}{P} x \cdot dx$$

where $\varphi_D(x)$ is the potential distribution at $y = D$ surface of the detector, which is only determined by the applied voltages and the configuration of anode electrodes.

In practice, the spatial period P usually satisfies the condition $P \ll D$, and equation (1) approaches:

$$\varphi(x, y) \approx a_0 \left(\frac{y}{D}\right) + \sum_{n=1}^{\infty} a_n \cdot \cos \frac{2\pi n}{P} x \cdot \exp\left(-2\pi n \cdot \frac{D-y}{P}\right) \quad (2)$$

As one can see, a_0 and a_n are Fourier-Transform coefficients of $\varphi_D(x)$. The potential $\varphi(x, y)$ is then just the inverse Fourier-Transform having each a_n multiply an exponential factor, with the exception of a_0 multiplying a linear term of y . At any particular y , the first term in equation (2) accounts for the average of $\varphi(x, y)$ over x , and the second term gives the deviation from the average value. It is evident that the deviation from the average at any y is modulated mainly by the exponential factor corresponding to $n = 1$. At $y = D - P/2$ and $y = D - P$, the amplitudes of deviations are reduced to about $\exp(-\pi)$ and $\exp(-2\pi)$ compared to that at $y = D$,

which are about 4.3% and 0.2% respectively. This is consistent with the results obtained using finite element analysis [1, 2].

Fig.2 shows the operating potential distribution, when space charge is not significant, within a semiconductor detector calculated using equation (1) under following conditions: strip electrodes and gaps between electrodes have the same width, the collecting electrodes are at 100 V and the non-collecting electrodes are at 80 V. The current i induced on an electrode due to the movement of a charge Q can be calculated using Ramo-Shockley theorem [5, 6]:

$$i = Q \vec{v} \cdot \vec{E}_w \quad (3)$$

Where $\vec{v}$ is the instantaneous velocity of charge Q , and $\vec{E}_w = -\nabla \varphi_w(x, y)$ is the weighting field which would exist at the position of Q under the following circumstances: the charge Q removed, the selected electrode at unit potential and all other electrodes are grounded. The weighting potential corresponding to the above detector configuration was calculated using equation (1) and is shown in Fig.3. The results are consistent with that of Luke [1, 2] obtained using finite element analysis. The potential distribution between electrodes on the $y = D$ plane was approximated using linear interpolation.

Some implications of equation (1) are listed below:

- (1) The voltage difference between the collecting and non-collecting electrodes should be set so that the potential difference between the maximum along the field line passing through the center of the non-collecting electrodes and that on the non-collecting electrodes is greater than the kinetic energy of the collecting charge carriers. This will ensure that the electric field can guide selected charge carriers onto the collecting electrodes.
- (2) The widths of collecting and non-collecting strip electrodes have to be the same. This makes the weighting fields of the two electrodes have identical linear terms, so that charge carriers within that region induce same amount of charge on both electrodes. By reading out the difference between the two electrodes, only the signal induced by charge carriers moving within the vicinity ($D - P < y < D$) of coplanar electrodes can be

picked out.

(3) Unipolar charge sensing technique could also be approached by reading out signals from strip electrodes individually. This can be understood from the weighting field distribution of the selected electrode. An example is shown in Fig.4 which assumes electrodes and gaps have the same width. In this case, the space period P in equation (1) was chosen to be 20 times of pitch of electrodes. As one can see, the average value a_0 of $\varphi_D(x)$ of the corresponding weighting field approaches zero as more electrodes are included. Therefore, the linear part of the weighting field can be very close to zero, and the weighting potential rises to 1 rapidly at the vicinity of the selected electrode. In practice, the minimum space period of electrodes is limited by the condition that the charge carriers are mainly collected by a single electrode.

(4) Two dimensional segmented electrode arrays have been used by many groups for γ -ray imaging applications. Barrett et al. [4] have suggested very recently that single polarity charge sensing can be approached by properly choosing the pixel size of two dimensional segmented electrode arrays, and by reading out signals from individual pixels. They have demonstrated both in theory and experiments. One thing in common on these detectors is that all pixels of the electrode array were biased at the same potential. The field distribution in these semiconductor detectors can be assumed to be more general in order to account for cases where electrode elements are connected to slightly different potentials, such as the example shown in Fig.5. It is easy to show that equation (1) can be extended to this three dimensional case, where $\varphi(x, y, z)$ has symmetry and is periodic both in x and y directions. Similar to the case of individual strip read out, the weighting potential of a selected pixel of collecting electrodes is very close to zero in the detector volume and rises rapidly to 1 while it approaches to the pixel within a distance of one space period. It could be advantageous to bias non-collecting electrode at a slightly lower potential to that of the collecting electrodes, in contrast to all electrodes biased at the same voltage: (1) Charge carriers could be guided by the electric field so that the gap effect could be improved. (2) The induced signal on the non-collecting electrode could be used to achieve position-sensing along z axis, and to correct for electron trapping while electrons are collected by collecting electrodes.

(2) Electronic work.

A charge-sensitive pre-amplifier circuit has been built to read out the difference of signals from two groups of electrodes, which is a modified circuit compared with Luke's original one. It has been tested using pulse generator and satisfactory results were obtained.

(3) Noise Analysis.

Research has been carried out in order to locate sources of noise which are critical to the performance of final devices. The results show that the noise is dominated by that of the diaphragm resistor in our current systems. The tests show that, in order to achieve good energy resolution, increasing the resistance between the two groups of anode electrodes to above several hundred $M\Omega$ is needed. This has become a critical requirement on surface resistance of a working device and carefully designed process is needed when patterning the electrodes onto the semi-conductor surface.

References

- [1] P.N. Luke, "Single-polarity charge sensing in ionization detectors using coplanar electrodes", *Appl. Phys. Lett.*, vol. 65(22), pp. 2884-2886, 1994.
- [2] P.N. Luke, "Unipolar charge sensing with coplanar electrodes - application to semiconductor detectors", *Conf. Proc. of IEEE Nuclear Science Symposium and Medical Imaging Conference, Norfolk, Virginia. Oct.30 - Nov.5, 1994.*
- [3] O. Frisch, ", British Atomic Energy Report BR-49, 1944.
- [4] H.H. Barrett et al., "Charge transport in arrays of semiconductor gamma-ray detectors", Private communications. Submitted to *Physical Review Letters*. 1995.

- [5] S. Ramo, "Currents induced by electron motion", *Proc. of the I.R.E.*, vol. 27(9), pp. 584, 1939.
- [6] W. Shockley, "Currents to conductors induced by a moving point charge", *Journal of Applied Physics*, vol. 9, pp. 635–636, 1938.

Fig. 1

Fig. 2

Fig. 4

Fig. 5