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W. Ashmanskas et al.
For the CDF Collaboration

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

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Silicon Vertex Tracker: A Fast Precise Tracking Trigger for CDF

W. Ashmanskas [a], A. Bardi [b], M. Bari [c], S. Belforte [b], J. Berryhill [a], M. Bogdan [a], A. Cerri [b], A.G. Clark [d], G. Chlanchidze [e], R. Condorelli [b], R. Culbertson [a], M. Dell'Orso [b], S. Donati [b], H.J. Frisch [a], S. Galeotti [b], P. Giannetti [b], V. Glagolev [e], A. Leger [d], E. Meschi [b], F. Morsani [b], T. Nakaya [a], G. Punzi [b], L. Ristori [b], H. Sanders [a], A. Semenov [e], G. Signorelli [b], M. Shochet [a], T. Speer [d], F. Spinella [b], P. Wilson [a], Xin Wu [d,1] A.M. Zanetti [c]

[a] *University of Chicago, USA*

[b] *University and Scuola Normale and INFN Pisa, Italy*

[c] *INFN Trieste, Italy*

[d] *University of Geneva, Switzerland*

[e] *Joint Institute for Nuclear Research, Dubna, Russia*

Abstract

The Silicon Vertex Tracker (SVT), currently being built for the CDF II experiment, is a hardware device that reconstructs 2-D tracks online using measurements from the Silicon Vertex Detector (SVXII) and the Central Outer Tracker (COT). The precise measurement of the impact parameter of the SVT tracks will allow, for the first time in a hadron collider environment, to trigger on events containing B hadrons that are very important for many studies, such as CP violation in the b sector and searching for new heavy particles decaying to $b\bar{b}$. In this report we describe the overall architecture, algorithms and the hardware implementation of the SVT.

1 Introduction

With the great success of silicon micro-strip detectors in high energy physics, their application in triggering has been one of the major goals in instrumenta-

[1] Corresponding author

tion development. The main application is to trigger on B hadrons, since the precision of the silicon detector allows measurements of the impact parameter (d) down to $\sim$10 μm, sufficient to detect tracks from decays of B hadrons produced in particle collisions. At hadron colliders, light quarks are produced with a cross section several orders of magnitude higher than that of b quarks. Therefore the capability of precision d measurement at the trigger level is essential for a hadron collider experiment to collect maximum statistics of events containing B hadrons, while avoiding light quarks events saturating the data acquisition system.

The Silicon Vertex Tracker (SVT) [1] is presently under construction for the CDFII [2] detector for the Tevatron Run II data taking period, starting from 2000. It operates at the level 2 of the three level trigger system of CDF. The level 1 trigger is a dead-timeless pipeline system with a latency of 5.5 μs. The readout time of the 400,000 channels of the silicon detector is about 3 μs, making the usage of the silicon information at level 1 impossible. On the other hand it is possible to to use the Central Outer Tracker (COT) at level 1. A device, called XFT, has been designed to reconstruct 2D track candidates above 1.5 GeV/c using COT, with a coarser p_T and ϕ measurements. XFT tracks are then used at level 2 by SVT, together with the silicon information, to reconstruct tracks with precise track parameters: p_T, ϕ and d. SVT tracks are then sent to the level 2 decision logic to select events compatible with B hadrons based on the presence of a secondary vertex or simply tracks with large impact parameters.

2 SVT Architecture

The CDF level 2 trigger is a four buffer system with 20 μs total processing time, among which 10 μs are used by the level 2 decision logic. Therefore only 10 μs are available for SVT to readout the silicon information and reconstruct tracks.

To achieve high speed and provide flexibility, the SVT has adopted the basic architecture of separating the pattern recognition and track fitting into two pipelined stages. As shown in Fig. 1, the pattern recognition is done with the Associative Memory, a highly parallel template matching system. A coarser resolution (super-strip) can be used at this stage to reduce the memory size and to improve tracking efficiency. The roads found by the AM system are passed to the track fitting stage, where the full resolution of the silicon detector is exploited. The transformation between hits and super-strips is done by the Hit Buffer.

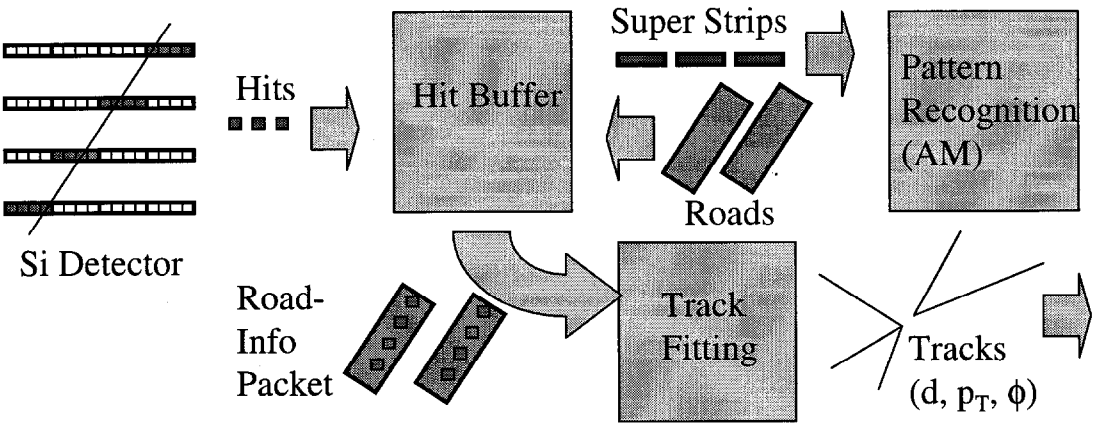

Fig. 1. SVT basic architecture

2.1 Associative Memory

When a track travers a tracker, it leaves a unique pattern of hits on each detector layer. The principle of template matching pattern recognition is to store legitimate hit patterns of all tracks of interest in a memory. Hits from an event are then compared to these pre-stored patterns. If all or a large percentage of hits of a pattern are present, a track candidate (called road) is found. The Associative Memory [3] is a realization of such a pattern memory that can compare each hit with all patterns in the memory in parallel, providing the high speed necessary for trigger applications. With the AM, pattern recognition is complete as soon as the last hit of an event is read. Roads found can then be immediately send out sequentially to the track fitting stage.

A full custom VLSI chip with 0.7 μm technology has been developed for the Associative Memory. It has a die surface of 35 mm^2 and about 180,000 transistors. One AM chip can store 128 patterns of 6 words (layers). Each word is 12 bits. For the application of SVT, 5 layers are reserved for silicon information, while the sixth layer is for XFT. The AM chips has been tested to be operational up to 40 MHz. The specification for SVT is 30 MHz.

The AM chip has a built-in flexibility to fine tune the matching algorithm, for example requiring matching of 5 layers out of 6 instead of 6 out of 6.

2.2 Linear Track Fitting Algorithm

Due to measurement errors, pattern recognition alone cannot give precise track parameters. As matter of fact, in order to have good tracking efficiency, re-

duced resolution hits (called super-strips) are used by AM. Optimization in terms of efficiency, memory size and fake tracks rate gives an super-strip size in the order of 250 μm, while the actual silicon strip pitch is about 60 μm.

In order to reconstruct tracks with high precision, track fitting with full resolution silicon hits is necessary. The SVT adopts a linear approximation of the standard χ^2 method to calculate the precise track parameters: $\vec{p} = (p_T, \phi, d)$.

The standard χ^2 is defined as

$$\chi^2 = (\vec{x} - \vec{x}^t(\vec{p}))^T V^{-1} (\vec{x} - \vec{x}^t(\vec{p}))$$

where $\vec{x}$ are the input measurements (silicon hits and XFT information), $\vec{x}^t(\vec{p})$ are the true values of these quantities for a given $\vec{p}$, and V is the covariance matrix of the measurements.

For tracks of interest for SVT (above 1.5 GeV/c), $\vec{x}^t(\vec{p})$ can be approximated by a linear function in terms of $\vec{p}$: $\vec{x}^t(\vec{p}) = \vec{a}^0 + A\vec{p}$. Since within a road variations of the parameters are small, we can linearly expand $\vec{p}$ around a central value $\vec{p}^0$, thus $\vec{p} = \vec{p}^0 + \delta\vec{p}$. We then have

$$\vec{x}^t(\vec{p}) = \vec{a}^0 + A(\vec{p}^0 + \delta\vec{p}) = \vec{x}^0 + A\delta\vec{p}$$

With this linear approximation, the solution of the minimization yields the fitted parameters as linear function of input measurements,

$$\vec{p} = W(\vec{x} - \vec{x}^0) + \vec{p}^0$$

where W, $\vec{x}^0$ and $\vec{p}^0$ are constants that can be calculated beforehand.

The χ^2 at minimum is used to reject fake tracks. Its calculation can also be linearized. Since three independent parameters are fitted, after rotation and linear approximation, we have

$$\chi^2_{min} = \chi^2_1 + \chi^2_2 + \chi^2_3 = V\vec{x} + \vec{b}$$

where V, $\vec{b}$ are also constants.

Thus the non-linear track fitting problem is reduced to a few calculations of scalar products that can be performed easily by dedicated hardware device. The linear approximation is rather good. In fact a single set of constant matrices W and V can be used for all roads in a 30^o wedge without significant loss of resolution.

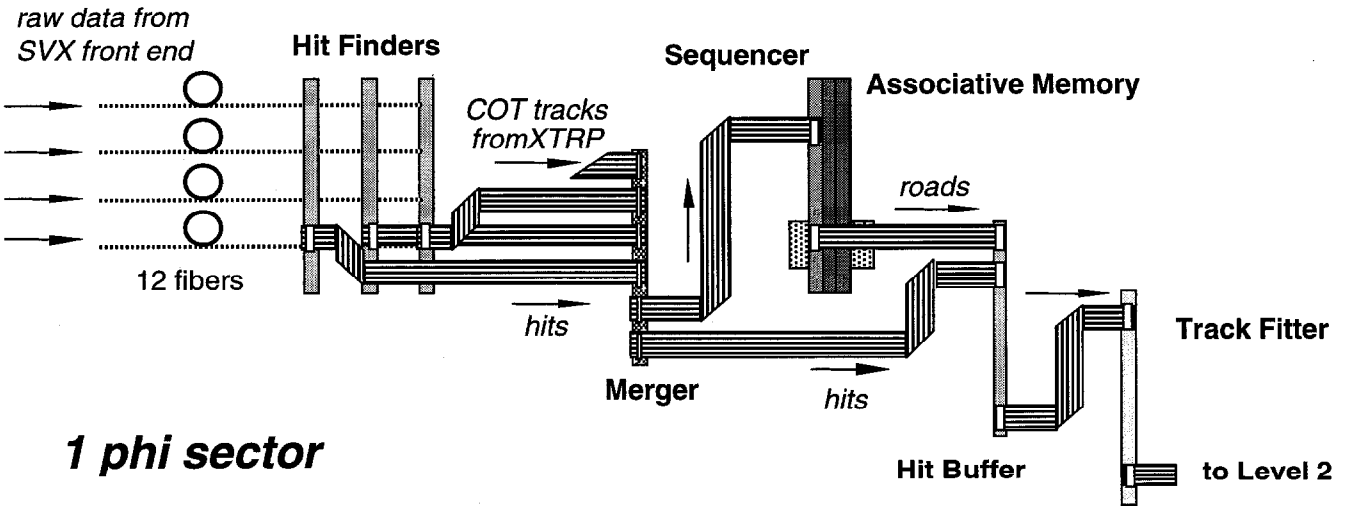

Fig. 2. SVT hardware implementation

2.3 Performance

The pattern recognition and track fitting algorithm of SVT have been tested on actual data from CDF Run I using a bit-level SVT simulation program. The fitted tracks have almost off-line precision. The resolution of impact parameter is about 35 μm for tracks of 2 GeV/c. The resolution of ϕ is 1 mrad, and that of p_T is $0.003p_T^2$ where p_T is in GeV/c.

3 SVT System Implementation

The SVT system has been designed as a data driven system that uses a uniform protocol for high speed (~30 MHz) asynchronous data exchange between different functional blocks within the system. All boards are VME 9U cards. The main functional blocks are: Hit Finder, Hit Buffer, AM system and Track Fitter, as shown in Fig. 2. The complete system consists of 12 identical sectors, each sector treats silicon hits coming from a 30^o ϕ wedge.

3.1 Hit Finder

Sparsified SVX II pulse height digitizations are sent from the front end electronics to SVT via optical links (G-link). Optical signals are converted to electrical signals and received by the Track Fitter board at 53 MHz. The first task of the Hit Finder is to rearrange the input data into 10 parallel synchronized data streams. Data in the same stream comes from strips in the

same layer. All 10 steams go through the clustering process in parallel, after pedestal subtraction and hot channel suppression. The charge center of gravity algorithm is used to find the hit coordinate of a cluster of adjacent hit strips: $x = \sum Q_i x_i / \sum Q_i$. The granularity of the centroid is 4 μm. The hits found are then merged into a single data stream and output to the Merger. Due to the large number of silicon channels, 3 Hit Finders are used for one 30^0 ϕ sector. The outputs of the Hit Finders are sent to the Merger, where 3 data streams are merged with XFT track information, and then sent to the AM system for pattern recognition. An identical copy of data is also sent to the Hit Buffer where hits belonging to roads found can be retrieved later.

The Hit Finder board has been designed and a prototype has been successfully tested up to the specified speed of 30 MHz. It uses mainly ALTERA FLEX10K chips for the logic realization that give the flexibility of changing the clustering algorithm by simply reprogramming the chips on board. The processing time for one event is about $2.0 + 0.03 \times$ (number of output hits) μs.

3.2 AM System

One sector of the AM system consists of one Associative Memory Sequencer (AM Sequencer) and two AM Boards. The AM Sequencer is the interface and manager of the pattern recognition system. It receives hits from the Merger, converts them to coarser resolution super-strips which are downloaded to the two AM Boards through a custom P3 backplane. AM Boards are where the AM chips are located. One AM board houses 128 AM chips in 16 mezzanine cards (called AM plugs). The AM chips are organized in a tress structure such that 2 AM Boards form a homogeneous 32 k pattern memory.

The pattern recognition is controled by the AM Sequencer via a set of opcodes sent to the AM boards. As soon as all super-strips are sent to the AM Boards, the AM Sequencer starts reading out roads found from the AM Boards and sending them to the Hit Buffer.

Both the AM Sequencer and the AM Boards have been designed and tested up to 30 MHz.

3.3 Hit Buffer

The Hit Buffer has two inputs, one is the hits found by the Hit Finders through the Merger, another is the roads found by AM through the AM Sequencer. During operation, hits are received first. They are sorted according to their super-strip numbers and then stored in a structured Hit List Memory, so that

all hits belonging to the same super-strip are stored together. When the AM system completes the pattern recognition, roads are received by the Hit Buffer. Since a road is made up of a unique set of super-strips, one in each detector layer, the Hit Buffer uses the road ID to look up these super-strip numbers from a map and uses them to access the Hit List Memory. Then the road ID and all hits belonging to it are packed in a Road-Info Package and send to the Track Fitter (see Fig. 1).

The Hit Buffer is a dense board with a large amount of memory chips. Protoype board has been designed and tested.

3.4 Track Fitter

The task of the Track Fitter is to calculate the track parameters p_T, ϕ and d, and reject fake tracks with a χ^2 cut, using the linear approximation approach mentioned earlier. Six scalar products are calculated, 3 for the parameters, and 3 for the χ^2.

The Front End processor part of the Track Fitter receives Road-Info Packages from the Hit Buffer and parallelize six input measurements, 4 from silicons (4 silicon points give sufficient precision) and 2 from XFT (p_T, ϕ). When there is more than one combination per road, all combinations are serialized in a FIFO. The Fitter part of the Track Fitter treats each combination at a time, but all six scalar products are calculated in parallel, each utilizing an ALTERA FLEX10K FPGA chip. The Output processor calculates the total χ^2 and rejects tracks that fail a χ^2 cut. Tracks that pass the cut are then sent out to the Level 2 Decision logic where secondary vertices can be formed, and selection can be made to trigger on B hadrons.

The Track Fitter has also been built and tested. The processing time for one events is about 2.0+0.3×(number of combinations) ×(number of roads -1) μs.

3.5 Error Handling

As mention above, the SVT is a data-driven system which gives a great flexibility in system design. However debugging and monitoring such a system is complicated. A strategy of Spy buffers is adopted to facilitate these tasks. All SVT boards, except the AM Boards, are equipped with circular Spy buffers where input and output data through the board are continuously copied. These buffers can be frozen and be readout through VME without interfering with the normal data flow. The AM Boards have synchronous communication with the AM Sequencer thus Spy buffers are unnecessary. The freezing of the

Spy buffers of all boards in a crate is controlled by a Spy Control board. One of the Spy Control is a master that can trigger the freezing of all Spy buffers in the SVT system.

Error conditions, such as FIFO full, parity error, invalid data, are constantly monitored by each board. Four actions can be taken by a board upon error occurrence, setting error bits in a VME register, setting error bits in the End Event word, pulling the local SVT_ERROR line and pulling the global CDF_ERROR line. The proper error handling procedure, for example freeze and readout the Spy buffers or re-initiate the SVT system, is coordinated by the Spy Control boards, which are also responsible for communicating the error conditions with the CDF DAQ. The Spy Control boards have also been designed and tested.

4 Conclusions

A fast online tracking device, the Silicon Vertex Tracker, has been fully designed and simulated. Major components have been prototyped and tested successfully. Production is underway and the full system will be installed in the CDF II detector for the Tevatron Run II data taking in the year 2000. It will provide a powerful tool for CDF in the studies of B physics, especially CP violation in the b sector and B_s mixing, and the search for new particles such the Higgs and SUSY particles.

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