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**Materials Preparation and Fabrication of Pyroelectric
Polymer/Silicon MOSFET Detector Arrays,
Subcontract 9-X61-J4927-1**

Final Report Submitted to:

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ABSTRACT

OBJECTIVES: (1) Develop thinner copolymers with improved pyroelectric coefficients and cast the material on substrates for detector evaluation. Deliver three 1 cm diameter polarized thin PVDF copolymer film detectors cast on substrates supplied by LANL.

(2) Investigate and design a small high density linear integrated pyroelectric polymer/silicon MOSFET array.

(3) Deliver several 64-element linear arrays of pyroelectric elements fully integrated on silicon wafers with MOS readout devices.

(4) Final Report.

STATUS: All tasks have been completed. The Items (1)-(3) have already been delivered to Mr. H. S. Murray at Group MEE-3 at LANL.

INTRODUCTION

We have delivered several 64-element linear arrays of pyroelectric elements fully integrated on silicon wafers with MOS readout devices.

We have delivered detailed drawings of the linear arrays to LANL. We have processed a series of two inch wafers per our submitted design. Each two inch wafer contains two 64 element arrays. After spin-coating copolymer onto the arrays, vacuum depositing the top electrodes, and polarizing the copolymer films so as to make them pyroelectrically active, each wafer was split in half.

We developed a thicker oxide coating separating the extended gate electrode (beneath the polymer detector) from the silicon. This should reduce its parasitic capacitance and hence improve the S/N.

We provided LANL three processed 64 element sensor arrays. Each array was affixed to a connector panel and selected solder pads of the common ground, the common source voltage supply connections, the 64 individual drain connections, and the 64 drain connections (for direct pyroelectric sensing response rather than the MOSFET action) were wire bonded to the connector panel solder pads. This entails $(64 + 64 + 1 + 1) = 130$ possible bond connections per 64 element array.

There now follows our report which details the processing steps and the progress of the individual wafers as they were carried through from beginning to end.

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1. N-CHANNEL ENHANCEMENT TYPE MOSFET

MOS transistors consist of two diodes separated by a gate region. A transistor is used as a voltage-controlled current source. The metal-oxide-semiconductor field effect transistor (MOSFET) is a device made on a semiconductor substrate, typically silicon. There are two regions of semiconductor material called the source and the drain. These regions contain more electrons than does the substrate. The source and drain are connected by a slab of the substrate called the channel. An n-channel transistor uses n-type semiconductors for the channel. The channel is covered by a thin film of oxide which acts as an insulator. On top of the oxide layer is a metal electrode, called the gate. The combination of the channel, oxide layer, and gate acts as a capacitor. The substrate is silicon, the oxide layer is silicon dioxide, and the bottom electrode is aluminum.

Enhancement occurs due to the gate placed over the insulating oxide. The gate acts as a charge collector, and a voltage exists across the gate and causes an electric field in the insulating layer. The electric field is a result of positive charges existing in the gate region. In order to counteract the positive charges, electrons from the source and drain enter the channel, thus giving the channel a negative charge. The electrons are free to move in the channel between the source and drain and therefore, enhance the conductivity between the two.

When a piezoelectric (pyroelectric) sensor is deposited on an extended gate of the MOSFET, the resulting circuit is known as a piezoelectric-oxide-semiconductor field effect transistor (POSFET). A top electrode is on top of the piezoelectric. When exposed to radiation, the piezoelectric causes a modulation on the electric field of the gate region. The greater the voltage produced on the gate due to the piezoelectric modulation, the lower the resistance between the source and drain and the greater the conduction. A cross-sectional view of the POSFET design which we utilized is shown in Figure 1.1. The top electrode used in this study was a sputtered thin gold layer.

2. SILICON WAFER DESIGN

The silicon wafers were designed to have two arrays of transistors. Each array had thirty-two pairs of transistors for a total of sixty-four transistors per array (Figure 2.1). The transistors in a pair are mirror images of each other. The fabrication of the wafers included the design of the different masks required to produce all the layers that would make the transistor array: stopper layer, active layer, poly-silicon layer, contacts layer, and metal 1 or bottom electrode layer. These layers are shown for a single transistor in Figure 2.2. The masks and the actual wafer were fabricated at the University of Pennsylvania's Microfabrication Laboratory from the computer generated mask designs.

Figure 1.1: Cross-section of the piezoelectric-oxide-semiconductor field effect transistor (Reference: Diana Esmail-Zandi, "A P(VDF-TrFE) Based Integrated Ultrasonic Transducer", Masters dissertation, University of Pennsylvania, 1990, p 21).

Figure 2.1: Silicon wafer transistor arrays and transistor pair diagrams.

Figure 2.2: Different layers used in the design of individual transistors.

3. CLEANING THE WAFERS

The first step in fabricating the sensor is cleaning the wafers. It is important that the wafers are cleaned properly; otherwise, the copolymer will not adhere correctly. First, the wafers were placed in a fuming Nitric Acid bath for three minutes. After this step, they were rinsed in deionized water for five minutes. Once the rinsing was done, the wafers were spun dry for twenty seconds at 3000 rpm. It is important to blow air on the back of the wafer so that it is dry enough for the spin coating machine to hold the wafer down. With this procedure finished, the wafers were ready to be coated with the piezoelectric film.

4. COPOLYMER COATING OF SILICON WAFERS

Once the wafers were cleaned, the next step was to coat them with a thin film of the copolymer, P(VDF/TrFE). Twenty percent by weight solutions of copolymer in methyl-ethyl ketone were prepared. The VDF/TrFE molar compositions were: 56/44, 61/39, and 70/30. The film was produced by overcoating several thin layers for the purpose of better control of the thickness and also to avoid any pinholes.

4.1 Spin coating of polymer onto wafer

The wafer was placed on a spin coating machine. The 20% solution of polymer was poured so that the entire wafer was covered. Spinning was started at 100 rpm and linearly increased to 4000 rpm within 10 seconds. The wafer was then spun at 4000 rpm for 50 seconds. The wafer was air dried for 20 to 30 minutes.

4.2 Solvent evaporation

After air drying the wafer, it was placed in a small oven at 90-100°C for 45 minutes. The wafer was then removed from the oven and air cooled for at least 30 minutes.

4.3 Overcoating polymer layers

Once the wafer cooled down, steps (a) and (b) were repeated until 6 layers of polymer had been coated onto the wafer. This produced a total polymer thickness of ~7 μm . However, for the 70/30 composition we also used a more concentrated composition and obtained some 15 μm thick films (samples D6 and C2 on "Flow Chart Listing" attached to this report).

5. GOLD METALLIZATION

A thin gold electrode was coated on top of the polymer film to produce the other contact for the extended gates. The gold was sputtered onto the polymer film.

Figure 5.1: Holding set-up used for gold metallization of top electrode.

5.1 Sputtering set-up

A set-up was devised to produce the electrode pattern on the polymer over the desired area. The set-up included the design of a mask and a holding device. Once the wafer was in place and the set-up secure, the whole assembly was taken to the sputtering machine. This set-up is shown in Figure 5.1.

5.2 Sputtering settings

The wafer was placed in an Argon sputtering machine. The machine was brought down to 25 mtorr before sputtering started. A current of 20 mA was used during sputtering, which lasted 15 minutes. After this step the wafer was removed from the set-up and examined for gold conductivity. A cross-sectional view of the resulting gold layer is shown in Figure 5.2.

Figure 5.2: Cross-sectional view of gold metallization on top of piezoelectric film.

6. ALUMINUM EXPOSURE

To perform the poling of the film and to make contact to the device bonding pads during wire bonding, part of the aluminum on the silicon wafer must be exposed. The only area requiring exposure is the bonding pads for the sources, gates, and drains. The process to expose only this area was the following (see Figure 6.1):

Figure 6.1: (a) Thin layer of photoresist; (b) After photoresist has been exposed and removed; (c) Removal of polymer to expose aluminum bonding pads.

6.1 Photoresist coating

A thin coat of negative photoresist was placed on top of the thin polymer film. It was spun at 3000 rpm for 30 seconds and immediately placed on a hot plate for soft baking at 90° for 15 minutes.

6.2 Photoresist exposure

After all the solvent had been removed through the soft baking, the negative resist was exposed to UV light using a mask aligner. Our intention was to remove the photoresist from the area where the polymer covered the bonding pads. The photoresist also needed to be removed from over the gold metallization that laid on top of the polymer. After exposing the photoresist to UV light, the wafer was placed in an developing solution for 1 minute and then in a photoresist rinsing solution for 30 seconds. The wafer was then dried by spinning it for 20 seconds at 3000 rpm.

6.3 Polymer removal

With the photoresist removed from the gold metallization and the bonding pads area, the next step was to remove the polymer that was still covering the latter area. This was accomplished by using cotton swabs soaked in acetone and carefully dissolving the exposed polymer. The remaining photoresist served to protect the rest of the polymer from being washed away by the acetone. With most of the polymer removed from the selected areas, a cotton swab soaked with ethyl alcohol was able to remove any remaining residue of polymer on the bonding pads and leave the aluminum completely exposed.

7. POLYMER ANNEALING

The wafers were placed in the oven for a period of 1.5 hrs at a temperature of 135°C. After 1.5 hrs the oven was turned off while keeping the wafers inside to allow for a gradual or slow cooling. This type of cooling is preferred because of the different thermal expansion coefficients between the polymer and the ceramic wafer.

8. POLYMER POLING

During poling, contacts to the gold top electrode and to the common electrode of the source-drain-gate (and extended gate) were accomplished via silver paste spheres attached to needle probes to avoid poking the aluminum or the polymer coating as shown in Figure 8.1. Hysteresis poling was carried out using a sinusoidal 0.01 Hz voltage supply up to ± 600 V for the thin films and ± 1400 V for the thicker films (see film preparation above). Higher voltage caused pinhole formation due to burn-through. These pinholes were repaired using small drops of copolymer solution. The

polarization coercive field peaks occurred at ± 350 V (± 770 V for the thicker films). The peaks were very broad for the 56/44 composition and sharp for the 70/30 composition.

Figure 8.1: Polymer poling using Ag balls on the probes to avoid puncturing the film.

9. BONDING PADS ISOLATION

The gate and drain of each transistor were attached to the source to create a common ground for poling purposes. These connections needed to be removed to isolate the source pad, the gate pad, and the drain pad. The aluminum connections that created the common ground had been exposed by removing the polymer on top. The idea was to manually scratch these connections to isolate all the bonding pads. A very sharp needle was used, and the procedure was performed under a microscope. After each wafer was processed, a continuity test was performed to determine whether the procedure had been successful and if rework was required.

10. WAFER CUTTING

Each wafer had two arrays in it. The next step was to cut the wafer to separate the arrays so that they could be assembled separately. With the use of a wafer cutter both arrays were separated as the wafer was broken as shown in Figure 10.1. One important factor in cutting the wafer was to make a close cut parallel to the bonding pads of the array so that wire bonding could be easily performed (wire bonding requires short distances between pads).

Figure 10.1: Wafer cutting to separate individual arrays.

11. PC BOARD DESIGN AND CONSTRUCTION

The array of transistors had to be accessed without the use of microscopic tools. Therefore it was required to develop a board that would allow for easy interaction between the array and measuring instruments. This board was designed and built in the following steps:

11.1 Board design

The board layout was designed using the software UNCLE. Once the design was finished, a 10X ruby of the layout was obtained for photolithographic purposes.

11.2 Layout mask

The 10X ruby was placed in a reduction camera to obtain a 1X copy of the layout. The film used was a Kodak Ortho film, that allows for a transparent copy of the layout (see Figure 11.1). This type of film is commonly used in screen printing board manufacturing. The reduction camera had to be adjusted to obtain an exact reduction to 1X. Once the film was exposed to UV light from the camera it had to be developed chemically. The exposed film was submerged into the developer and the tray was continuously rocked for 1.5 minutes or a little longer until the lines were clearly defined. Following the developer, a rinse bath of 10 seconds was required. The next step was to place the film into a fixer bath while rocking the tray for 5 seconds every 30 seconds. After this, the film was placed in a tray of running tap water for ten minutes and then air dried. Once it was finally dry, the film was a transparent 1X copy of the layout. Several masks were made using this procedure.

Figure 11.1: Negative of the mask used for board etching (2.5X actual size).

11.3 Board cutting and perforation

Large boards with thick copper metallization were available. To use these boards more efficiently they needed to be cut into smaller boards. The size of the smaller boards was 2.25 inches by 1.5 inches. The arrays cut from the original wafer will be mounted on these smaller boards and the bonding pads would be connected to the board layout through wire bonding. The board will then be attached to a flat wire connector. This connector has pins that have to go through the board in order to make physical connection. Two parallel lines of 40 perforations each were made on the boards to attach the flat wire connector. The diameter of the holes was 0.016 inches.

11.4 Board copper cladding thickness reduction

Since the metal layer of the boards was too thick, a shaving process was required. The boards were placed in a Ferric Chloride solution to etch part of the thickness of the metal away until a more desirable thickness was obtained. After this procedure the boards were cleaned with a brillo pad to remove all chemical residues.

11.5 Board exposure

The board was covered with a thin layer of positive photoresist. This was accomplished by covering the entire board with positive resist and then spinning it in a spin coater at 3000 rpm for 20 seconds. After spinning the board was softbaked at 125°C for 3 minutes on a hot plate. The board, now covered with a layer of positive resist, was taken to the mask aligner where the previously made layout mask was ready to be used. The boards were exposed for a period of 6.1 seconds at a wavelength of 400 nm. After exposure, the board was placed into the positive photoresist developer for 65 seconds; then it was bathed in deionized water for 90 seconds; finally it was air dried. From this procedure, a pattern of photoresist was left on the board that would protect the copper from the etching solution and leave the desired pattern on the board.

11.6 Board etching

A plastic container was filled with Ferric Chloride and the exposed photoresist covered board was submerged therein for a period of 12-14 minutes (inspecting the board every 2 minutes). Once the etching was completed, the board was rinsed with water and then inspected under the microscope. The next step was to clean the photoresist from the remaining copper pattern with acetone.

12. WAFER AND BOARD ATTACHMENT

After the board is clean and dry, a solution of an epoxy adhesive is prepared and gently applied on the appropriate spot on the board where the wafer will be located. The adhesive should be uniformly applied and as thin as possible. The wafer is placed onto the desired location and gently pressed to enable a rigid flat seal (Note: this rigid flat seal is essential for the next step which is wire bonding).

13. WIRE BONDING FROM WAFER PADS TO BOARD PADS

Examine the device to verify its flatness by placing it on a flat surface. This is important because the Al wire cannot be bonded onto the device if there is gap that absorbs the force that is required to bond the wire. To eliminate any gaps in the adhesion, put a small amount of superglue in these gaps and press until a full adhesion is obtained. Now the device is ready for wire bonding. On the device there are 64 bonding pads that correspond to the gates, 64 that correspond to the drains, and one bonding pad that corresponds to the common source line. On the other hand, the board has 64 bonding pads to be used for either gate or drain connections, a 65th pad to be used for connecting to the common source line, and a 66th pad reserved for ground connection to the gold electrode; this last pad is located at the left side of the board. A wedge wire bonder is used to connect the aluminum pads on the silicon to the copper pads on the board as shown in Figure 13.1. The pads on the silicon are

Figure 13.1: Wire-bonding from wafer (in this case drain) to printed circuit board.

0.005 inches on a side, the wedge size is 0.004 inches, and the aluminum wire is 0.00125 inches in diameter. The wedge bonder utilized is Kulicke and Soffa's model 4123.

14. FLAT WIRE CABLE CONNECTOR ATTACHMENT

After wire bonding, the perimeters of the holes on the board are inspected for bare spots that could have come from the etching process. Repair of these bare spots was done using silver paste. Now the flat wire cable connector can be gently plugged in, being careful not to disturb the aluminum wire connections.

APPENDIX A

FLOW CHART LISTING OF POSFET ARRAYS

FLOW CHART OF POSFET SENSOR ARRAYS - FROM POLYMER COATING TO POLING AND LEAD CONNECTION

NAME	Copolymer coating	Gold metallization	Bonding pads exposed	*Poling
(1) 61/39 or B2 A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. Sparks @ +775V, repaired B. Sparks @ +650V, repaired
(2) 56/44 A B	Wafer - 7 coats (1-5, 15%; 6-7, 17.5%)	O.K.	O.K.	A. Sparks @ $\pm 527V$, repaired B. $\pm 500V$, O.K.
(3) 70/30 A B	Wafer - 6 coats (1-4, 15%; 5-6, 17.5%)	O.K.	O.K.	A. $\pm 610V$, O.K. B. One spark @ $\pm 525V$, repaired
Test 61/39 A B	Wafer - 6 coats (1-2, 17.5%; 3-6, 20%)	O.K.	O.K.	A. Damaged by voltage jump, not repaired B. Sparks @ $\pm 450V$, not repaired
Test 56/44 A B	Wafer - 6 coats (20%)	Thin and spotty.	O.K.	A. One spark @ $\pm 540V$, repaired B. $\pm 536V$, O.K.
DT2 (61/39) A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. $\pm 550V$, O.K. B. $\pm 550V$, O.K.
C4 (56/44) A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. $\pm 500V$, O.K. B. Sparks @ $\pm 567V$, repaired
D6 (70/30) A B	Wafer - 6 coats (25%)	O.K.	O.K.	A. $\pm 1348V$, O.K. B. Sparks @ $\pm 1400V$, repaired
D7 (61/39) A B	Wafer - 6 coats (20%)	O.K.	Sample "A" broke during processing.	B. Sparks @ $\pm 590V$, repaired
D9 (56/44) A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. Sparks @ $\pm 250V$, not repaired B. Sparks @ $\pm 370V$, not repaired
C2 (70/30) A B	Wafer - 6 coats (25%)	O.K.	O.K.	A. $\pm 1350V$, O.K. B. $\pm 1350V$, O.K.
C3 (61/39) A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. $\pm 550V$, O.K. B. $\pm 550V$, O.K.
DT3 (56/44) A B	Wafer - 6 coats (20%)	O.K.	O.K.	A. Sparks @ $\pm 550V$, not repaired B. One spark @ $\pm 600V$, repaired

* Annealing was performed prior to poling. All wafers were annealed for 1.5 hrs at 135°C without any difficulties.

Note: The five "D" wafers consisted of 1.2um thermal diposition plus 1.8um CVD.

The other eight wafers had 1.2um thermal deposited oxide layer only

NAME

Wafer cuttingBoard attachmentWire bonding

(1) 61/39 or B2	Wafer not yet cut	X X	X X
(2) 56/44 A B	O.K. O.K.	X X	X X
(3) 70/30 A B	O.K. O.K.	A. To board # 6 B. To board # 1	A. Connections were made to gates only <NOT SENT> B. Connections to gates and drains could not be made
Test 61/39 A B	Wafer not worth cutting	X X	X X
Test 56/44 A B	O.K. O.K.	A. To board # 9 B. Broke during attachment	A. Connections were made to gates only <SENT> X
DT 2 (61/39) A B	O.K. O.K.	X B. To board # 4	X B. Connections were made to drains only <NOT SENT>
C 4 (56/44) A B	O.K. O.K.	A. To board # 3 X	A. Connections to gates and drains could not be made X
D 6 (70/30) A B	O.K. O.K.	A. To board # 5 X	A. Connections were made to gates and drains <SENT> X
D 7 (61/39) A B	O.K. O.K.	X B. To board # 8	X B. Connections were made to gates and drains <SENT>
D 9 (56/44) A B	Wafer not worth cutting	X X	X X
C 2 (70/30) A B	Wafer broke while cutting	X X	X X
C 3 (61/39) A B	Wafer broke while cutting	X X	X X
DT 3 (56/44) A B	O.K. O.K.	X X	X X