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A Novel Non-Destructive Silicon-on-Insulator Nonvolatile Memory - LDRD 99-0750 Final Report

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A Novel Non-Destructive Silicon-on-Insulator Nonvolatile Memory - LDRD 99-0750 Final Report

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ABSTRACT

Defects in silicon-on-insulator (SOI) buried oxides are normally considered deleterious to device operation. Similarly, exposing devices to hydrogen at elevated temperatures often can lead to radiation-induced charge buildup. However, in this work, we take advantage of as-processed defects in SOI buried oxides and moderate temperature hydrogen anneals to generate mobile protons in the buried oxide to form the basis of a "protonic" nonvolatile memory. Capacitors and fully-processed transistors were fabricated. SOI buried oxides are exposed to hydrogen at moderate temperatures using a variety of anneal conditions to optimize the density of mobile protons. A fast ramp cool down anneal was found to yield the maximum number of mobile protons. Unfortunately, we were unable to obtain uniform mobile proton concentrations across a wafer. Capacitors were irradiated to investigate the potential use of protonic memories for space and weapon applications. Irradiating under a negative top-gate bias or with no applied bias was observed to cause little degradation in the number of mobile protons. However, irradiating to a total dose of 100 krad(SiO₂) under a positive top-gate bias caused approximately a 100% reduction in the number of mobile protons. Cycling capacitors up to 10⁴ cycles had little effect on the switching characteristics. No change in the retention characteristics were observed for times up to 3x10⁴ s for capacitors stored unbiased at 200°C. These results show the proof-of-concept for a protonic nonvolatile memory. Two memory architectures are proposed for a protonic non-destructive, nonvolatile memory.

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INTRODUCTION

Radiation-hardened nonvolatile memories are used in several Sandia, other DOE, and DoD systems for both program and critical data storage (e.g., B83 common radar, B61 permissive access link, MET, and satellite NuDet systems). Critical data must be retained if power is lost. Using an electrically erasable/programmable read only memory (EEPROM) for program storage has several benefits over using a mask programmable ROM: 1) the program can be easily changed, 2) the IC is not classified until programmed (the IC fabrication is not classified), and 3) the IC can be used in several systems rather than being specific to one system. A number of different commercial non-destructive readout, non-volatile memory EEPROMs are available. However, these devices cannot withstand the harsh radiation environments associated with either a weapon or satellite environment.

Silicon-on-Insulator (SOI) technology is actively being pursued at Sandia for the Sandia/Intel radiation-hardened processor (RHP) and other DP and satellite programs. SOI technology offers many advantages over bulk-silicon technology for improved high dose rate transient and single-event upset (SEU) radiation hardness, and high-speed and low-power operation [1]. Devices with orders of magnitude improvements in high dose rate transient ionizing radiation response have been fabricated [2]. Techniques used to harden memories to single-event upset (e.g., feedback resistors) result in considerably more performance degradation for bulk-silicon circuits than for SOI circuits. For example, feedback resistors are often used to harden SRAMs to SEU. To obtain similar SEU hardness levels, the size of the feedback resistor must be considerably larger for bulk-silicon technologies than for SOI technologies, resulting in considerably larger increases in write times for bulk-silicon devices. In fact, electrical performance advantages gained as bulk-silicon IC technologies advance to smaller and smaller dimensions can be completely lost if circuits are hardened to SEU. This is not necessarily the case for SOI circuits.

Figure 1 is a cross section of an SOI transistor. It consists of a thick silicon substrate, a buried oxide, and a top silicon layer. The top silicon layer is very thin, normally between 50 and 200 nm thick. Transistors are fabricated in the thin top silicon layer. The improved high dose rate transient and SEU radiation hardness for SOI technology results from lower charge collection volumes due to the fact that SOI transistors are built on an insulating layer. Two types of SOI transistors are partially-depleted and fully-depleted transistors. In a partially-depleted transistor, the depletion region underneath the gate does not extend completely through the top silicon layer. Conversely, for a fully-depleted transistor, the depletion region extends completely through the top silicon layer. Because the entire silicon layer is depleted for a fully-depleted transistor, the top-gate is electrically coupled to the back-channel Si/SiO₂ interface. This makes fully-depleted transistors more sensitive to charge buildup in the buried oxide (e.g., induced by total dose ionizing irradiation) than partially-depleted transistors.

Figure 1: Cross section of an SOI transistor.

In previous work [3-6], we showed that a post-processing anneal in a hydrogen-containing ambient (e.g., forming gas, $N_2:H_2$; 95:5) above 500°C triggers the formation of mobile, positively charged protons (H^+) in the buried oxide of an SOI substrate. As illustrated in Fig. 2, the protons can drift toward either the top or bottom buried oxide/silicon interface by applying a bias to the bottom silicon substrate or the top silicon layer. If a negative bias is applied to the top silicon layer, the mobile protons will collect near the top buried oxide/silicon interface producing a net positive charge at the interface. In theory, this positive charge can invert the back channel of a n-channel transistor causing an increase in the source-to-drain current, I_{DS} , of a partially-depleted SOI transistor, or decrease the top gate threshold voltage of a fully-depleted SOI transistor (turning it to low resistance state, normally ON). Similarly, by applying a positive bias to the top silicon layer, the mobile positive charge will drift to the bottom interface and the transistor will be returned to its standard (charge neutral) normally OFF condition. In this manner, by switching the bias on the top silicon layer from positive to negative, the back channel can be switched from a low resistance (ON) to a high resistance (OFF) state. A device formed by fabricating SOI transistors on a hydrogen-annealed SIMOX buried oxide, integrated with CMOS readout circuitry, has the potential to function as a radiation-hard, low-power, non-destructive nonvolatile memory. The memory transistor can be read or written by applying an appropriate bias to the gate electrode of the transistor.

In this LDRD, we explore the potential of protonic motion to form an SOI non-destructive readout nonvolatile memory. Capacitors and transistors were fabricated and annealed in hydrogen at moderate temperatures. A large part of this work was devoted to optimizing the number of mobile protons during processing. The results of this effort are described. The effects of total-dose irradiation, long-time storage, and voltage cycling on mobile proton density are presented. Although we did not fabricate a memory circuit, two circuit architectures for a memory circuit are presented. The feasibility of forming a non-destructive memory by a hydrogen anneal is discussed.

Figure 2: Illustration of protonic memory concept for a fully-depleted SOI transistor. Positive charge in the buried oxide near the top Si/SiO₂ interface will cause a negative shift in threshold voltage turning the transistor to an “ON” state (high leakage at $V_{GS} = 0$ V). Positive charge in the buried oxide near the back Si/SiO₂ interface will have little effect on the threshold voltage and the transistor will be in an “OFF” state (low leakage at $V_{GS} = 0$ V).

EXPERIMENTAL DETAILS

The buildup of mobile protons in both separation by implanted oxygen (SIMOX) and Unibond (a trademark of SOITEC) substrates was investigated. Two types of SIMOX substrates were used — standard dose and supplemental dose. Standard dose SIMOX substrates were created by implanting p-type silicon wafers with 190-keV O⁺ ions to a dose of $1.8 \times 10^{18} \text{ cm}^{-2}$ followed by a subsequent anneal at 1320°C in Ar + 1% O₂, resulting in a 150-nm silicon layer on top of a ~400-nm buried oxide. To fabricate supplemental dose substrates, standard dose substrates were given an additional oxygen implant at a much lower level than the first implant and then annealed at 1100°C. Unibond substrates are formed using a bonded technique. Normally a thick oxide is grown on a silicon p-type wafer, and hydrogen is implanted through the oxide into the silicon. The hydrogen implant creates microvoids in the silicon. The oxidized wafer is bonded to another silicon wafer and annealed at moderate temperatures (200 to 600°C). The moderate temperature anneal cracks the implanted wafer at the peak of the implant profile, forming a thin top-silicon layer. A high temperature anneal (~1100°C) is used to strengthen the wafer bond, and the surface quality is improved using a chemical-mechanical touch polish. Note

that, for both SIMOX and Unibond SOI substrates, the fabrication sequence includes a high-temperature anneal. Because of the high-temperature anneal, the buried oxide can contain numerous defects, most of which are related to oxygen vacancies [7]. When exposed to ionizing irradiation, these defects can induce significant charge buildup in the oxide and at the top and bottom Si/SiO₂ interfaces, degrading an SOI transistor by generating radiation-induced back-channel leakage current. However, as discussed below, when these defects are exposed to hydrogen during fabrication, they can produce mobile protons. The goal of this LDRD is to take advantage of these mobile protons to demonstrate the feasibility of a novel non-volatile memory transistor based on protonic motion in an SOI buried oxide.

Capacitors were fabricated in Dept. 1812's laboratory at the Advanced Materials Laboratory (AML), and transistors and capacitors were fabricated in Sandia's Microelectronics Development Laboratory (MDL). The AML is a research-type laboratory permitting rapid and wide ranging experiments to be performed. However, the largest wafer size that can be accommodated in the anneal furnaces is approximately 3x3 cm². Thus, all experiments were performed on pieces of six-inch diameter wafers. The MDL is a state-of-the-art R&D clean-room processing facility. Fully-processed complex integrated circuits can be fabricated within the MDL. Process conditions are considerably more controlled in the MDL than in the AML. A successful display of protonic transport in capacitor and/or transistor test structures in the MDL would help to demonstrate the commercial viability of protonic memory circuits.

The process and test sequence for the first sets of capacitors fabricated in the MDL consisted of fabricating capacitors using a prescribed anneal cycle, depositing aluminum metallization, removing the wafers from the MDL, and characterizing the capacitors. Using this sequence, additional anneals could not be performed due to the low melting temperature of the aluminum metallization and because of contamination issues that prevented the return of wafers to the MDL. Because the turnaround time for fabricating capacitor lots was normally more than two months, this severely limited the number of anneal variations that could be studied.

To greatly enhance the number of variations of anneal cycles, a TiSi₂ process was developed for this work. For this process, aluminum contacts were replaced with TiSi₂. The TiSi₂ metallization contacts can withstand post-annealing treatments up to 900°C. Forming gas anneals were performed after metallization, and then capacitors were tested in-line. Thus, wafers did not have to be removed from the clean room environment. After capacitance-voltage (C-V) testing, capacitors were given different anneal treatments and recharacterized. In this manner, we could rapidly determine the effect of different anneal treatments on protonic hysteresis. Note that prior anneals were not found to have significant effect on the results of subsequent anneals.

For the capacitors fabricated in the MDL, two photolithographic mask sets were designed and fabricated. The first mask set is for fabrication of capacitors for C-V measurements, capacitors for point-contact transistor I-V measurements, and test structures for electron paramagnetic resonance (EPR) measurements. The second mask set is for fabrication of memory transistors using a standard IC process flow. Most of the data presented on MDL devices are for capacitors fabricated using the first mask set. Software was written for performing the C-V and point-contact transistor measurements.

Figure 3: Schematic diagram of the point-contact pseudo-MOSFET technique.

Capacitors were characterized by measuring the threshold voltage shift using a point-contact pseudo-MOSFET transistor technique [8] and by standard C-V techniques. A schematic diagram of the point-contact transistor technique is shown in Fig. 3. Two metal probes are placed on the top silicon layer to form source and drain point contacts. The bottom substrate and the buried oxide act as the gate and gate oxide, respectively, of a standard MOS transistor. (Note that, although the point-contact transistor technique simulates a real transistor by artificially creating a source and drain, we still refer to the device as a capacitor to distinguish it from a full transistor as discussed below.) The pseudo-MOSFET technique is most sensitive to proton buildup near the top silicon/buried oxide interface. The C-V measurements were used to characterize protonic effects close to the substrate/buried oxide interface. Thus, by combining pseudo-MOSFET and capacitor measurements, information on protonic effects near both the top and bottom silicon/buried oxide interfaces can be obtained.

Transistors were fabricated using a modified version of Sandia's CMOS6rs technology. This technology employs TiSi_2 metallization contacts. In contrast to standard ICs, no aluminum interconnect metallization was used. (Each transistor was individually connected to probable bond pads and no interconnect metallization was required.) As such, moderate temperature hydrogen anneals could be performed as the last step of the process. Note from Fig. 1 that each SOI transistor structure inherently includes two transistors — a top-gate transistor and a back-

gate transistor. Similar to the point-contact measurements on capacitors, a back-gate transistor is composed of the bottom substrate (gate), buried oxide (gate oxide), and the top-gate source and drain. Transistors were characterized by taking I-V curves of the back-gate or top-gate transistor after poling protons to either the top or bottom buried oxide/silicon interface and measuring the amount of hysteresis voltage shift.

NVFET EXPERIMENTAL RESULTS

The majority of the experimental results were taken on capacitors, including data demonstrating a protonic memory's radiation hardness, fatigue, and retention properties. The results from the capacitor measurements are presented first. In the last part of this section, experimental results taken on transistors are presented.

Mobile Proton Generation

A simplified schematic diagram for the process flow for generating mobile protons in the buried oxide is shown in Fig. 4. The high-temperature anneals used to form SIMOX and Unibond substrates create numerous neutral oxygen vacancies (strained silicon-silicon bonds) in the oxide caused by the outdiffusion of oxygen [9]. Similar defects can be created in a standard MOS thermal gate oxide after exposing the oxide to a high-temperature anneal. If exposed to molecular hydrogen, these strained Si-Si bonds can act as H₂ cracking sites in the buried oxide [10] to generate atomic hydrogen. If the atomic hydrogen releases its electron to the silicon conduction band, especially at elevated temperatures ($T > 450^{\circ}\text{C}$), in a forming gas environment, a free mobile proton is created. Thus, the key step to generate mobile protons in SOI buried oxides is to expose SOI substrates to hydrogen at elevated temperatures. It is possible that the high-temperature annealed Si/SiO₂ interfaces result in relatively stable sites (non-trapping), of unknown origin, for the protons. Hence, the mobile protons remain between the Si/SiO₂ interfaces and are free to drift between the interfaces under an applied field.

Figures 5 and 6 illustrate the hysteresis caused by mobile protons in the buried oxide measured by the point-contact transistor I-V and capacitor C-V curves, respectively. The arrows in the figures indicate the direction of the I-V or C-V sweep. The I-V curves were taken on capacitors fabricated on Unibond substrates in the AML, and the C-V curves were taken on capacitors fabricated on SIMOX substrates in the MDL. Mobile protons were generated in the capacitor for the I-V curves by annealing the capacitors at 600°C in forming gas (e.g., N₂:H₂; 95:5 by volume) for 5 min. Mobile protons were generated in the capacitor for the C-V curves by annealing the capacitors at 700°C in forming gas for 15 min. The I-V curves were taken by applying a +50 V bias to the top-silicon layer for 5 min. to move the protons towards the bottom buried oxide/silicon interface, sweeping the bias from +10 to -50 V, applying a -50 V bias to the top-silicon layer for 5 min. to move the protons towards the top buried oxide/silicon interface, and sweeping the bias from -50 to +10 V. Similarly, the C-V curves were taken by applying a +20 V bias to the top-silicon layer for 2 min. to move the protons towards the bottom buried oxide/silicon interface, sweeping the bias from +20 to -20 V, applying a -20 V bias to the top-silicon layer for 2 min. to move the protons towards the top buried oxide/silicon interface, and sweeping the bias from -20 to +20 V. The magnitude of the threshold voltage shift is directly

Figure 4: Simplified flow-chart for generating mobile protons in the buried oxide of an SOI capacitor.

proportional to the number of mobile protons. These shifts are sufficient to fabricate a nonvolatile memory.

One data set that strongly supports the hypothesis that the drifting specie is a mobile proton is a comparison of the rate of decay of the drain current versus temperature for capacitors exposed to hydrogen and to deuterium. Figure 7 is a plot of the decrease in drain current as a function of time ($\Delta I_D/\Delta t$), normalized to the initial drain current times the temperature (T), versus $1000/T$. The drain current was measured using the point-contact transistor method. The capacitors were annealed in either forming gas ($N_2:H_2$; 95:5) or deuterated forming gas ($N_2:D_2$; 95:5) at 600°C . After anneal, the ions were drifted towards the top Si/SiO₂ interface by applying a positive bias to the substrate. The ions were then drifted towards the bottom interface at different temperatures by applying a negative bias to the substrate. The activation energy, E_A , is

Figure 5: Typical I-V curve measured using the point-contact transistor technique for a forming gas annealed capacitor.

obtained from the slopes of the curves. The difference in the absolute values between the two curves in Fig. 7 represents a difference in a prefactor of 1.5 in good agreement with the theoretically expected difference in ion mass for the ionic mobility. This provides strong evidence that the drifting specie is hydrogen [5].

A large portion of this work was devoted to the determination of the anneal conditions for optimizing the number of mobile protons in the buried oxide. This work was performed in both the AML and the MDL. Several different types of hydrogen anneals were performed. These included standard furnace anneals, rapid thermal anneals (RTA), and vacuum anneals. In each case, hydrogen was introduced using forming gas, a mixture of hydrogen and nitrogen. In all cases, the hydrogen anneal was the last process step.

One process condition that was found to have a large effect on the voltage hysteresis was the rate at which devices were pulled from the furnace. Figure 8 is a plot of the mobile proton density versus cool-down rate. The capacitors were fabricated on Unibond substrates in the AML and annealed at 600°C for 20 min. This anneal time is sufficiently long to allow the buildup of protons to reach their equilibrium value at 600°C. The mobile proton density was measured from the reversible part of the hysteresis voltage shift at midgap. As is evident from the figure, a fast cooling rate must be used to optimize mobile proton density. For cooling rates below 1 K/s, there is a large reduction in the number of mobile protons. This is consistent with anneals performed in the MDL. The largest hysteresis voltage shifts were obtained using rapid

Figure 6: Typical C-V curve showing hysteresis effect.

thermal anneals (RTA) with a fast ramp down. No significant mobile proton density generation was observed for standard furnace anneals where the cooling rate is less than 0.1 K/s. Specifically, the maximum hysteresis voltage shift (~ 3 V) for capacitors fabricated on SIMOX substrates in the MDL was obtained for a 700°C, 15 min. RTA anneal on a small piece of a wafer (<1 in.²).

To investigate the method for hydrogen incorporation, forming gas annealed samples were characterized after repeated C-V measurement/etch cycles. This is illustrated in Figs. 9-11. Figure 9 is a drawing of the capacitor structures. Capacitors with a uniform top silicon layer across the buried oxide (Fig. 9a) and capacitors with the center silicon layer wet etched to the buried oxide (Fig. 9b) were fabricated. Both sets of capacitors were annealed at 700°C in forming gas for 10 min. The capacitors were then wet etched to form small silicon island capacitors as illustrated in Fig. 9c, and C-V measurements were performed. In this manner, we could explore the extent of lateral hydrogen diffusion (proton buildup) underneath the silicon or vertical hydrogen diffusion through the top silicon. Figure 10 shows the lateral mobile proton density after etching the small silicon islands for the capacitor where the anneal was performed with a uniform top-silicon layer. Figure 11 shows the lateral mobile proton density after etching

Figure 7: Decay of normalized drain current versus $1/T$ for forming gas and deuterated forming gas annealed capacitors.

the small silicon islands for the capacitor where the anneal was performed with the center silicon region removed [11]. For both sets of capacitors, the mobile proton density is high near the edges of the original capacitor (at the time the anneal was performed) and decreases rapidly toward the center of the capacitor. These measurements show that the reactive hydrogen species, which trigger the proton generating reaction, enter the oxide from the edges of the capacitor and diffuse laterally along the oxide layer. Hence, the amount of the reactive species reaching the oxide by diffusion through the silicon overlayer is negligible in SOI material, and the rate of the reaction(s) that generates the mobile protons is likely to be diffusion limited (through the oxide). As a result, in a full IC, it is critical that the edges of the buried oxide of the memory transistor are not covered with material (e.g., silicon, silicon nitride, etc.) that can retard the diffusion of hydrogen to the buried oxide. On the other hand, one may selectively fabricate non-memory transistors on the same wafer as memory transistors by covering the edges of the buried oxide of the non-memory transistor with a material (e.g., silicon nitride) that halts the flow of hydrogen.

Because the generation of mobile protons depends on the rate of diffusion of molecular hydrogen through the buried oxide, the rate of buildup of mobile protons will depend on time. Figure 12 shows the buildup of mobile protons in capacitors fabricated in Unibond substrates

Figure 8: The effect of cooling rate (the rate samples were pulled from the furnace) on mobile proton density. The samples were annealed at 600°C for 20 min.

versus time. The capacitors were annealed in forming gas at 600°C. The buildup is relatively fast, reaching 60% of the saturation level in less than 250 s [12].

Although large hysteresis shifts could be obtained from isolated capacitors, the uniformity across a wafer was poor (1 to 3 V, typical). This was true for whole wafers (six-inch in diameter) and for small pieces of wafers ($\sim 1 \text{ in.}^2$) for capacitors fabricated in the MDL. However, recent results by Devine [13] suggest that better uniformity can be obtained. Many different gas flow patterns and rates, wafer sizes, and anneal temperatures, times, and ramp rates were examined, but no combination resulted in large hysteresis voltage shifts uniformly across a wafer. Unless the factors that enabled Devine to obtain reproducible and controllable hysteresis voltage shifts can be identified and replicated in other laboratories, this will be a significant deterrence for protonic memory circuit fabrication. This problem must be solved before protonic memories can be realized at the MDL. Because of problems with uniformity and reproducibility of results in the MDL, we did not attempt to fabricate complete IC memories, and instead focused on investigating the effects of anneal conditions on mobile proton generation.

Figure 9: Capacitor test structures for investigating the kinetics of mobile proton buildup. 9a) Capacitor with a uniform top silicon layer across the entire sample. 9b) Capacitors with the center region wet etched. 9c) Small silicon island capacitors formed from capacitors 9a) and 9b) after annealing in forming gas.

Proton Activation by Hydrogen Implantation

An alternate method for introducing protons in the buried oxide is by ion implantation. If successful, this technique could be advantageous over a forming gas anneal, because implantation could be used to selectively protonate transistors. To explore this, Unibond SOI substrates were implanted with protons at an energy of 40 keV to fluences of 0.5, 1.0, and $4.0 \times 10^{14} \text{ cm}^{-2}$. TRIM-90 simulations show that the vast majority of the protons are stopped inside the buried oxide layer. Some samples were annealed in pure argon or in forming gas at 600°C for 5 min. after proton implantation. Figure 13 shows point-contact transistor I-V curves for a) an untreated capacitor, b) the same capacitor as "a)" after implanting with protons, and c) the same capacitor as b) after an additional 600°C forming gas anneal. The proton implant produces a small negative shift and some broadening of the I-V characteristics relative to the non-implanted device [14]. However, the proton implant does not induce any detectable I-V hysteresis (i.e., mobile protons) in this capacitor. The broadening of the I-V dip (distance

Figure 10: Lateral buildup of mobile proton density for the capacitor of Fig. 9 (a) after annealing in forming gas and etching small silicon island capacitors.

between flatband and threshold voltage) suggests an increase in the density of interface traps [15,16]. The data demonstrate that the amount of trapped positive charge in the oxide is only a small fraction of the implanted dose (about 10^{11} cm^{-2} vs. $5 \times 10^{13} \text{ cm}^{-2}$). This implies that the vast majority of the implanted protons trap an electron during the stopping process.

Several proton-implanted capacitors were subjected to a 600°C post-implantation anneal in argon for 5 min. The argon anneal did not result in an increase in I-V hysteresis and produced only a slight decrease in threshold voltage. Thus, the argon anneal did not activate the interfacial proton generation reaction as in a standard forming gas anneal. Finally, a few of the implanted capacitors were subjected to a 600°C forming gas anneal. The hydrogen anneal resulted in a large hysteresis similar to that shown in Fig. 5. Hence, the dynamics of hydrogen incorporation into the buried oxide via implantation is different than that via a forming gas anneal. As a result, based on the implant and anneal conditions investigated in this work, it does not appear that hydrogen implantation is a viable approach for fabricating a protonic memory. However, it is possible that other hydrogen implant conditions may yield better results.

Figure 11: Lateral buildup of mobile proton density for the capacitor of Fig. 9 (b) after annealing in forming gas and etching small silicon island capacitors.

Response to Total-Dose Ionizing Irradiation

Considerable work has been performed that strongly suggests that hydrogen plays a key role in radiation-induced charge buildup in MOS oxides [17]. As such, it is not unreasonable to expect that irradiation may adversely affect the retention and switching characteristics of a protonic memory. To investigate the effects of irradiation on the switching and retention characteristics, capacitors were irradiated with 10-keV x rays. Figure 14 shows the effects of different bias conditions on the change in threshold voltage hysteresis. The capacitors were fabricated on SIMOX substrates and mobile protons were introduced into the buried oxide by annealing pieces of a wafer in forming gas at 600°C for 30 min. Samples were irradiated at a dose rate of 4 krad(SiO_2)/s with no bias (floating), positive top-gate bias from 0 to 100 krad(SiO_2) and negative top-gate bias from 100 to 200 krad(SiO_2), or negative top-gate bias from 0 to 100 krad(SiO_2) and positive top-gate bias from 100 to 200 krad(SiO_2). The biased irradiations were performed with an electric field of 0.5 MV/cm. Protons were *prepoled*

Figure 12: Buildup of mobile protons versus anneal time. The capacitors were fabricated on Unibond substrates and annealed at 600°C in forming gas.

(positioned) near the top (negative top-gate bias) or bottom (positive top-gate bias) interface. With no bias applied during irradiation, a negligible decrease in the hysteresis was observed. Even after irradiating to 1 Mrad(SiO_2) there was no substantial loss in hysteresis (data not shown) [6]. Irradiating capacitors initially with a negative top-gate bias also resulted in little or no change in hysteresis voltage shift. However, further irradiation of the capacitors with a positive top-gate bias resulted in nearly 100% of the protons being trapped near the bottom Si/SiO_2 interface reducing the hysteresis voltage shift to near zero [5]. Similarly, irradiating the capacitors initially with a positive top-gate bias caused almost a 100% reduction in the voltage hysteresis; however, the threshold voltage hysteresis recovered after further irradiation under a negative top-gate bias. The threshold voltage hysteresis shift is caused by mobile H^+ ion drift. A positive top-gate bias causes protons to drift to the bottom Si/SiO_2 interface and a negative top-gate bias causes protons to drift to the top Si/SiO_2 interface. The magnitude of the threshold voltage hysteresis shift is proportional to the number of mobile protons in the buried oxide. Thus, Figure 14 indicates that protons can be trapped at the bottom interface during irradiation. The data also suggest that the trap properties in the buried oxide are asymmetric as noted by proton trapping near the bottom Si/SiO_2 interface but not near the top Si/SiO_2 interface.

Figure 13: I-V curves measured using the point-contact transistor technique for a) an as-fabricated capacitor (no implant or forming gas anneal), b) after implanting with hydrogen, and c) after implanting with hydrogen and then annealing in forming gas.

The protons trapped after irradiating to 100 krad(SiO_2) with a positive top-gate bias are not permanently trapped. The protons can be detrapped by exposing the capacitors to an elevated temperature anneal or by re-irradiating the capacitors with a negative bias on the top gate (Fig. 14). Fig. 15 shows the hysteresis voltage shift measured at flatband for capacitors irradiated to 100 krad(SiO_2) with a positive top-gate bias and then subjected to a postirradiation anneal. Prior to irradiation, the hysteresis voltage shift was approximately 32 V. Irradiation caused the hysteresis voltage shift to decrease to near zero. After irradiation, the capacitors were subjected to a 100°C anneal with a negative top-gate bias. Fig. 15 shows that as the anneal time is increased, the number of mobile protons increases. This indicates that the proton traps are relatively shallow. After annealing to 100°C, nearly 100% of the “trapped” mobile protons have been released [5]. However, if the anneal temperature is reduced to room temperature, the

Figure 14: Change in threshold voltage hysteresis versus total dose for capacitors irradiated unbiased, with the bias switched from negative to positive, and with the bias switched from positive to negative.

hysteresis shift decreases with time during repeated cycling (not observed preirradiation). These data suggest that the proton traps are not permanently annealed.

In actual device operation, irradiating under a positive top-silicon bias (negative substrate bias) corresponds to irradiating a memory transistor while writing it to the OFF state. Most of the time, memory transistors will be unbiased during irradiation. For transistors irradiated unbiased, the number of protons trapped during irradiation is small for total doses up to 1 Mrad(SiO₂). Thus, degradation will occur primarily during the time that the memory transistor is being written to a write state. This will depend on system conditions. Because the amount of time that the memory transistor will be written to the OFF state is small, the total dose level that a protonic memory should be able to function to in a space environment could be relatively high.

One of the most confusing properties of the mobile protons generated by a moderate temperature anneal is that they do not result in any significant buildup of interface traps. EPR measurements showed that the hydrogen anneal creates a very small concentration of P_b centers

Figure 15: Effect of irradiation and postirradiation anneal on the hysteresis voltage shift.

(interface traps) and no measurable E' centers. There is overwhelming evidence in the literature that shows that hydrogen ions (protons) released during exposure to ionizing are either directly or indirectly involved in radiation-induced interface-trap buildup [17].

Several experiments were performed to better understand this apparent discrepancy between the nature of protons created by a hydrogen anneal and by ionizing irradiation. Figure 16 is a plot of the buildup of the areal density of mobile protons versus forming gas anneal time for a) capacitors that were previously subjected to a high-vacuum 670°C , 6 hour anneal and then subjected to a forming gas anneal, and b) capacitors subjected to a forming gas anneal but without a previous high-vacuum anneal (control). The forming gas anneal was performed at 600°C for 30 min. EPR measurements show that the high vacuum anneal maximizes the density of P_b centers by releasing hydrogen bonded with interface traps [5,18,19]. As such, there are fewer interface traps passivated with hydrogen after a vacuum anneal. It is clear from Fig. 16 that the generation of mobile protons is delayed in the capacitor subjected to a vacuum anneal (high initial interface-trap density), as compared to the capacitor that was not subjected to a vacuum anneal. Point-contact transistor measurements and EPR data (not shown) show that the buildup of mobile protons occurs on the same time scale as the decrease in interface-trap density for the capacitor that was subjected to a high-vacuum anneal. A simple calculation of the time that it takes for hydrogen to diffuse through the edges of the capacitor shows that it should take

Figure 16: Increase in mobile proton density versus time for capacitors annealed in forming gas with and without (control) a pre-vacuum anneal.

approximately 25 min. at 600°C for the buried oxide to be saturated with H_2 . This time is in excellent agreement with the time required to generate mobile protons in the capacitor that was not subjected to a vacuum anneal. Note that interface traps in this capacitor are passivated with hydrogen prior to the forming gas anneal. In these hydrogen passivated capacitors, the generation of mobile protons is diffusion limited. In the vacuum-annealed (depassivated) capacitor, all of the hydrogen that reaches the buried-oxide interfaces during the forming gas anneal is initially consumed by the interface trap passivation mechanism. Not until all the interface traps have been passivated does the buildup of mobile protons begin to occur. This explains the delayed buildup of mobile protons in Fig.16. Thus, it is likely that the interface-trap passivation reaction has a lower activation energy than the mobile proton formation reaction [19-21], or perhaps more likely, the mobile proton formation reaction cannot even occur until all of the other available sites for the hydrogen to occupy are saturated [22].

Fully-Processed Transistor Characteristics

A special 7-layer mask set was designed for fabricating fully-processed NVFET transistors in the Sandia's Microelectronics Development Laboratory (MDL). The mask set

included standard transistors and transistors without a top gate. The standard transistor is illustrated in Fig. 1. Each transistor structure inherently includes two transistors — a back-gate transistor and a top-gate transistor. The back-gate transistor is formed by the bottom substrate of the SOI wafer (gate contact), buried oxide (gate oxide), and the source and drain of the top-gate transistor. The top gate transistor has a thermally grown gate oxide and should be relatively defect free. As such, exposure of the top-gate oxide to hydrogen should not generate mobile protons. For NVFET operation using partially depleted transistors, mobile proton transport in the buried oxide is used to control the leakage current state of the top-gate transistor. As a result, I-V measurements of the back-gate transistor contain information on the amount of mobile proton charge available for memory operation. The devices without top-gate transistors still had source and drain contacts, but the polysilicon gate was replaced with a nitride. This transistor structure was fabricated to determine if proton motion could be controlled solely by the source and drain contacts.

Partially-depleted n-channel transistors were fabricated in the MDL using a modified version of Sandia's hardened CMOS6rs (SOI) technology. The CMOS6rs technology has an effective gate length of 0.5- μm , a gate-oxide thickness of 12 nm, and a hardened shallow trench for transistor isolation. The gate width varied from 0.75 to 20 μm . (Transistors with gate lengths from 0.35 to 2.3 μm were also fabricated and analyzed. However, the data do not reveal any new insight into protonation effects and the data are not reported here.) Standard dose SIMOX wafers with a buried oxide thickness of ~ 370 nm and a top silicon thickness of 150 nm (post processing) were used. A very large hysteresis (>20 V) was observed in the back-gate transistor I-V curves for transistors without a top gate *prior* to exposing them to a hydrogen anneal due to leakage in the bottom corner of the trench oxide. Unfortunately, the hysteresis was in the wrong direction for protonic transport, i.e., positive threshold voltage shift after applying a positive bias to the back-gate contact. As a result, no further experiments were performed on these transistors and all transistor data reported here is for standard transistors with a top gate. To generate mobile protons in the buried oxide, wafers were cut into individual die and the die were annealed in forming gas (Ar:H₂; 95:5 by percent volume) at 600°C for 30 min. This was the last step in the process. (As mentioned previously in the experimental details section, transistors were individually connected to bond pads and aluminum interconnect metallization was not required. This allowed the use of moderate temperature anneals as the last process step.)

Figure 17 illustrates the effects of a forming gas anneal on the top-gate I-V curves. The top-gate transistor was measured with the source, body, and back-gate grounded and with a top-gate voltage sweep of +4 to -4 V. The drain-to-source voltage during measurement was 1 V and the transistor gate width was 8 μm . Fig. 17 shows a large negative shift in the I-V curves after the anneal for top-gate transistor. This negative I-V curve shift is caused by the generation of positive fixed charge in the top gate oxide after the anneal. In many instances, this buildup of fixed charge was large enough to turn a normally OFF top-gate transistor into the ON state (as shown in Fig. 17). As a result, when fabricating a memory IC, the threshold voltage of the top-gate transistors will have to be increased during processing to ensure that the transistors can be written to the OFF state. The forming gas anneal also causes a large increase in leakage current for the top-gate transistor. This leakage current is likely caused by the generation of fixed charge in the buried oxide after the anneal (undesired) and/or the generation of mobile protons in the buried oxide (desired). Note that the buried oxide was not prepoled with the mobile protons

Figure 17: Effect of a hydrogen anneal on the I-V characteristics of the top-gate transistor.

either near the bottom or top buried oxide/silicon interface. As such, the mobile protons could be distributed throughout the buried oxide.

The large amount of fixed charge in top-gate oxide generated by the forming gas anneal will have a large impact on the back-gate I-V characteristics. This is illustrated in Fig. 18 where back-gate I-V curves are shown before and after a forming gas anneal. The back-gate transistor was measured with the source, top-gate, and body grounded and with a back-gate voltage sweep of +70 to -20 V. The drain-to-source voltage during measurement was 1 V and the transistor gate width was 8 μm . A large leakage current is observed in the I-V characteristics after the forming gas anneal. Again, this leakage current causes the top-gate to be ON even though the top-gate voltage is zero.

The memory properties of the top-gate transistor were characterized by measuring the hysteresis voltage shift of the back-gate transistor. The hysteresis voltage shift is directly proportional to the number of mobile protons in the buried oxide. Hysteresis voltage shifts were observed for all back-gate transistors characterized. As expected, no hysteresis voltage shifts were observed for the top-gate transistors. A typical set of I-V curves illustrating the observed

Figure 18: Effect of a hydrogen anneal on the I-V characteristics of the back-gate transistor. $V_{GS} = 0$ V

back-gate transistor hysteresis is shown in Figure 19. To reduce the effects of fixed charge in the top-gate oxide, these curves were taken with a top-gate bias of -8 V. This gate voltage is sufficiently large to “turn off” the top-gate even with the large concentration of fixed charge in the top-gate oxide, and thus, eliminate (or reduce) the large leakage current observed in the back-gate transistor I-V curves shown in Fig. 18. The data for Fig. 19 were taken by poling the protons to the bottom buried oxide/silicon interface by applying a -40 V bias for 60 s to the bottom substrate and sweeping the back-gate voltage from -20 to +70 V, and then by poling the protons to the top buried oxide/silicon interface by applying a +40 V bias for 60 s to the bottom substrate and sweeping the back-gate voltage from +70 to -40 V. These I-V curves show good hysteresis characteristics. The hysteresis voltage shift for this transistor is ~1.8 V.

The amount of hysteresis varied considerably between transistors (0.8 to 10.2 V) similar to that presented previously for capacitors. Figure 20 is a plot of the hysteresis voltage shift for gate widths from 0.75 μm to 20 μm . The transistors were taken from two parallel test strips located on a test die. The smaller gate width transistors (0.75 to 5 μm) were on one test strip and the larger gate width transistors (6 to 20 μm) were on another test strip with the gate widths in a numerically increasing sequence. The test strips were physically oriented with the 5- μm gate width transistor next to the 20- μm gate length transistor and both of these transistors were

Figure 19: I-V curves for a back-gate transistor illustrating the hysteresis caused by mobile protons in the buried oxide. The top-gate bias was -8 V.

located at one edge of the die. The largest hysteresis voltage shift (10.2 V) was measured on the 20- μm transistor. This hysteresis shift is large enough to fabricate a nonvolatile memory IC. For each test strip, the hysteresis voltage shift increased from the smallest gate-width transistor to the largest gate width transistor. However, the hysteresis voltage shift measured on the 5- μm gate width transistor located on the first test strip was much larger than the hysteresis voltage shift measured on the 6- μm transistor located on the second test strip. This suggests that at least a large part of the variation in hysteresis voltage shift for the different gate width transistors is due to variations in the manner that hydrogen is incorporated into the buried oxide caused by the location of the transistor on the test strip rather than the gate width of the transistor.

The final demonstration of the proof-of-concept of a protonic nonvolatile memory is to show that mobile proton transport in the buried oxide can be used to control the leakage current of the top-gate transistor. Figure 21 shows top-gate transistor I-V curves taken after applying either a -40 V bias for 60 s or a +40 V bias for 60 s to the bottom substrate. The I-V curves were taken with a -4 to +4 V gate sweep. Applying a -40 V bias will pole the mobile protons to the bottom buried oxide/silicon interface. This should result in the lowest leakage current level as is observed in Fig. 21. Applying a +40 V bias will pole the mobile protons to the top buried oxide/silicon interface. This should result in the largest leakage current as the protons invert the

Figure 20: Hysteresis voltage shift versus transistor gate width.

back-channel interface. The gate width of the transistors was 20 μm to maximize the observed effect. (Similar results were obtained for other gate-width transistors, but as expected, the difference between the leakage currents was smaller.) Hence, we have switched the leakage current state from an OFF condition by poling the mobile protons to the bottom buried oxide/silicon interface to an ON condition by poling the mobile protons to the top buried oxide/silicon interface. For a memory transistor, the threshold voltage of the top-gate transistor will have to be increased during processing to ensure that the leakage current at a gate-to-source voltage of zero is small when the transistor is in the OFF condition. In any case, these I-V curves demonstrate the proof-of-concept of a protonic nonvolatile memory.

Memory Properties - Fatigue and Retention

The hysteresis effect described above can be used to fabricate a nonvolatile memory. For instance, an n-channel transistor can be changed from a normally "OFF" state to a normally "ON" state by applying a negative top-gate bias to drift the mobile protons from the bottom interface to the top interface. Similarly, an n-channel transistor can be changed from a normally "ON" state to an "OFF" state by applying a positive top-gate bias. For a memory device, this can be interpreted as writing the device to a bit state "1" or "0", respectively. To read the device,

Figure 21: Top-gate I-V curves taken after poling the bottom substrate with either a -40 or $+40$ V bias. These curves show that the leakage current of the top-gate transistor can be controlled by mobile proton transport in the buried oxide. This is a proof-of-concept for a protonic nonvolatile memory.

the zero bias drain current can be measured (high current corresponds to a logic state “1”, and low current corresponds to a logic state “0”). This is a non-destructive measurement, i.e., the charge state in the buried oxide is not disturbed during a read operation. Two important memory properties are the number of times a device can be cycled from a “1” to “0” state (fatigue) and the time that a memory will stay in a preprogrammed state (retention).

To investigate the fatigue properties, some capacitors (370-nm gate oxide) were stressed with a 20 V AC signal for up to 10^4 cycles. No loss in hysteresis voltage shift was observed during the cycling. To investigate the retention characteristics, some capacitors were characterized with the protons poled at either the top or bottom interface and periodically characterized using point-contact transistor I-V measurements. Figure 22 shows retention data (I_{DS} versus time) taken on SIMOX capacitors preprogrammed into either a “1” (protons near the top Si/SiO₂ interface) or “0” (protons near the bottom Si/SiO₂ interface) state. The capacitors were stored at 200°C, and I_{DS} was periodically measured. No change in source-to-drain current was observed for capacitors poled with the protons at either the top or bottom interface for times

Figure 22: Retention data on a SIMOX capacitor programmed with the protons at the top (squares) and bottom (circles) Si/SiO₂ interfaces and then heated to 200°C under a floating bias condition.

up to 3×10^4 s at 200°C. This provides a proof-of-principle demonstration of the retention capabilities of the devices [6].

H₂ ANNEAL FOR IMPROVED BURIED OXIDE QUALITY – A NEW TECHNIQUE

During the course of this work, we also observed that moderate temperature hydrogen anneals can improve the quality of SIMOX buried oxides. Annealing substrates in H₂ was observed to dramatically reduce buried oxide leakage current and reduce the number of low-field breakdown capacitors. For example, Figs. 23 and 24 are breakdown field histograms for SIMOX substrates formed with an implant dose of 4.1×10^{17} cm⁻² without and with a 600°C forming gas furnace anneal (low cool rate), respectively [23]. Note that this implant level is well below that used to form the standard dose SIMOX capacitors discussed above and can lead to numerous defects that can cause high leakage currents throughout the buried oxide. However, this implant level is being actively pursued to reduce the cost of SIMOX substrates. (A major contributor to the cost of SIMOX substrates is the time required to implant the wafers with oxygen. Thus, lowering the oxygen implant dose level will substantially lower processing costs. However, before low-dose SIMOX substrates can become a commercially viable product, techniques must

Figure 23: Buried oxide breakdown field histograms for SIMOX substrates formed with an implant dose of $4 \times 10^{17} \text{ cm}^{-2}$.

be developed to improve the quality of low-dose SIMOX substrates.). No significant H_2 induced positive charge was generated in these oxides. For the substrates annealed in forming gas, none of the capacitors broke down at a field of less than 2 MV/cm. Because the leakage current and the number of low-field breakdown capacitors can be reduced by a H_2 anneal, these data strongly suggest that pipes (silicon filaments in the buried oxide shorting the top and bottom substrates together) are not a major source of defects in these substrates. H_2 tends to disassociate weak Si-Si bonds ($\equiv\text{Si-Si}\equiv + \text{H}_2 \rightarrow \equiv\text{Si-H} + \text{H-Si}\equiv$) [10]. It is possible that buried oxide conduction is enhanced by (or related to) weak Si-Si bonds (or silicon clusters) created by the high-temperature anneal used to form SIMOX substrates, and that a H_2 anneal reduces the number of weak Si-Si bonds, thus reducing the amount of defect conduction.

SOI NVFET MEMORY ARCHITECTURE

Two memory architectures have been developed for the SOI NVFET. The first is an EEPROM cell that consists of an NVFET and an NMOS access transistor. Figure 25 shows the cross section of a single memory cell, while Table 1 lists the bias conditions for the various operations. During the read, mode the gate is grounded so that there is no risk of upsetting the data in the cell. Because the gate is not used to select which cell to read, an access transistor is required. To read a cell, the access transistor is turned on. Some of the assumptions behind this architecture are: 1) both transistors have standard gate oxide, 2) the buried oxide in memory array is the memory oxide, 3) substrate contacts are required for the memory transistor, and 4) full depletion/inversion operation. Figure 26 shows the schematic of a 2x2 array, and Table 2 lists the bias conditions for the memory array.

Figure 24: Buried oxide breakdown field histogram for SIMOX substrates that were formed with an implant dose of $4 \times 10^{17} \text{ cm}^{-2}$ and subjected to a 600°C forming gas furnace anneal.

The second option is a flash architecture. The advantage of this approach is that an access transistor is not required, only one NVFET per cell. The disadvantage is that the gate of the NVFET is biased during read operations. This may cause problems with upsetting the data in the cell. A low voltage, fast read is required to avoid this – fortunately, that is exactly what one would like to do! Figure 27 shows the cross section of a memory cell, and Table 3 lists the bias conditions. A 2x2 memory array is shown in Fig. 28 with the bias conditions listed in Table 4. For the flash approach to work, the “erase” threshold voltage (V_{th}) must be greater than 0 but less than the read voltage (e.g., $V_{GS} = 2 \text{ V}$). The “program” V_{th} must be greater than the read voltage. The flash approach does have the potential problem of over erasing the memory (i.e. a V_{th} less than zero). To use this approach, the programming logic must ensure that the cell is erased but not over erased. This adds complexity compared to the EEPROM architecture, but allows for twice the array density.

DISCUSSION AND CONCLUSIONS

Voltage hysteresis levels large enough to fabricate a nonvolatile memory have been obtained on test transistors and capacitors. The number of mobile protons was found to remain stable for unbiased and negative top-gate bias irradiations, cycling up to 10^4 cycles, and preprogrammed storage at 200°C for times up to $3 \times 10^4 \text{ s}$. Memory architectures have been developed that can utilize the observed hysteresis voltage shifts for fabricating a protonic

Table 1: Buried oxide SOI EEPROM array biasing.

Mode	MG0	NG0	Sub0	SL0	BL0	MG1	NG1	Sub1	SL1	BL1
Erase Row0	0v	0v	-10v	0v	Float	0v	0v	0v	0v	Float
Prg "10"	+10v	0v	0v	+10v	Float	0v	0v	0v	0v	Float
Erase Row1	0v	0v	0v	0v	Float	0v	0v	-10v	0v	Float
Prg "01"	0v	0v	0v	0v	Float	+10v	0v	0v	+10v	Float
Read Row0	0v	5v	0v	0v	Sense Amp	0v	0v	0v	0v	Sense Amp

Figure 25. SOI buried oxide EEPROM cell.

memory. These results demonstrate the proof-of-concept of a protonic non-destructive, nonvolatile memory.

However, before a radiation-hard protonic memory can be realized, some problems must be overcome. The biggest problem observed in this work was that the magnitude of the threshold voltage hysteresis was found to be extremely non-uniform. Many anneal conditions were examined, but none led to uniform threshold voltage hysteresis shifts across a wafer as has been observed by others [13]. Until anneal methods are found that can lead to uniform threshold voltage hysteresis shifts, it is highly unlikely that a protonic memory IC can become a commercially viable product. There is little radiation-induced degradation in the number of mobile protons except when a positive top-gate bias is applied during irradiation. This corresponds to a write operation. Most of the time a memory transistor will be unbiased. Thus, significant radiation-induced degradation may occur only if the memory transistors are continually written to.

The final issues that must be addressed before a protonic memory can be realized are process integration issues. We have not attempted to discuss these issues in this work. However, it is conceivable that there could be many competing factors in a full IC process that

Table 2: Buried oxide SOI EEPROM cell bias conditions.

Mode	MG	NG	SL	BL	Sub	Backgate
Erase ("0")	0v	0v	0v	Float	-10v	0v
Program 1	+10v	0v	+10v	Float	0v	0v
Program 0	+10v	0v	0v	Float	0v	0v
Word Line Program Inh	0v	0v	+10v or 0v	Float	0v	0v
Read	0v	5v	0v	Sense Amp	0v	0v
Standby	0v	0v	0v	Float	0v	0v

Figure 26: 2x2 memory array for an EEPROM cell.

could either enhance or subtract from the amount of mobile protons [24]. In addition, device layout and process topography (e.g., silicon nitride layers over trench sidewalls) could substantially retard hydrogen diffusion and reduce the buildup of mobile protons. Thus, although the proof-of-concept for a protonic nonvolatile memory has been demonstrated, we are still far from realizing a commercially viable product.

Table 3: Buried oxide flash cell bias conditions.

Mode	MG	SL	BL	Sub	Backgate
Erase ("0")	0v	0v	Float	-10v	0v
Program 1	+10v	+10v	Float	0v	0v
Program 0	+10v	0v	Float	0v	0v
Word Line Program Inh	0v	+10v or 0v	Float	0v	0v
Read	2v	0v	Sense Amp	0v	0v
Standby	0v	0v	Float	0v	0v

Figure 27. SOI buried oxide flash cell.

Table 4: Buried oxide SOI flash array bias.

Mode	MG0	Sub0	SL0	BL0	MG1	Sub1	SL1	BL1
Erase Row0	0v	-10v	0v	Float	0v	0v	0v	Float
Prg "10"	+10v	0v	+10v	Float	0v	0v	0v	Float
Erase Row1	0v	0v	0v	Float	0v	-10v	0v	Float
Prg "01"	0v	0v	0v	Float	+10v	0v	+10v	Float
Read Row0	2v	0v	0v	Sense Amp	0v	0v	0v	Sense Amp

Figure 28: 2x2 memory array for a flash cell.

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- 1 MS-0612 Review & Approval Desk, 4912
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