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FAST AND SLOW BORDER TRAPS IN MOS DEVICES

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Abstract

Convergent lines of evidence are reviewed which show that near-interfacial oxide traps (border traps) that exchange charge with the Si can strongly affect the performance, radiation response, and long-term reliability of MOS devices. Observable effects of border traps include capacitance-voltage (C-V) hysteresis, enhanced 1/f noise, compensation of trapped holes, and increased thermally stimulated current in MOS capacitors. Effects of fast (switching times between ~ 10^{-6} s and 1 s) and slow (switching times greater than ~ 1 s) border traps have been resolved via a dual-transistor technique. In conjunction with studies of MOS electrical response, electron paramagnetic resonance and spin dependent recombination studies suggest that different types of E' defects (trivalent Si centers in SiO_2 associated with O vacancies) can function as border traps in MOS devices exposed to ionizing radiation or high-field stress. Hydrogen-related centers may also be border traps.

I. Defect Location and Electrical Response

Defects at or near the Si/SiO_2 interface communicate with the Si over a wide range of time scales. For example, a relatively large amount of 1/f noise is commonly observed in MOS devices [1-3], as illustrated in Fig. 1. On the time scale of the noise measurements, 0.01 - 1 s, the defects responsible for the noise are near-interfacial oxide traps that exchange charge with the Si [1-4]; that is, "border traps." If there were no border traps, there would be much less noise in this frequency range [3,4]. Border traps with similar time constants have also been identified in AC conductance measurements [5], and in frequency-dependent charge-pumping studies [6-9]. Because defects exchange charge with the Si over a wide distribution of times, the traditional Deal committee nomenclature [10] used to describe MOS electrical response in terms of oxide traps (presumed not to exchange charge with the Si during typical electrical measurements) and interface traps is often inadequate to provide a complete description of MOS electrical response [11,12].

One possible modification to the Deal nomenclature that separates terms referring to the defect location from terms used to describe the electrical response is illustrated in Fig. 2 [12]. The physical location of the defects is shown in Fig. 2(a), where the extent of the hatched region in which border traps are found is determined by the time scale of the measurements. The slower the measurement, the more time traps in the oxide have to exchange charge with the Si. This determines whether their charge states are fixed during electrical measurements, or whether their charge states can switch, as illustrated in Fig. 2(b). For example, during a typical set of MOS subthreshold current-voltage measurements, the measuring time is on the order of a few seconds. If the charge exchange between the Si and the border traps occurs via tunneling, the hatched region of the oxide in which oxide traps function as switching states is ~ 2.5 nm in Fig. 2 [11-13]. For consistency, the nomenclature of Fig. 2 will be used in this review, though some results were presented using different (equivalent) terminologies when originally published.

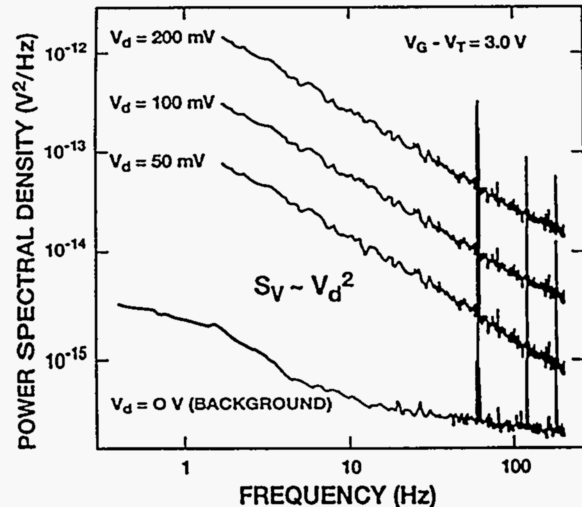

Figure 1: Noise power vs. frequency for an unirradiated nMOS transistor with a 45-nm oxide. The gate length is 3 μm, and width is 16 μm. The spikes at 60 Hz and harmonics are extraneous pick-up, and are neglected in analysis of 1/f noise spectra. (After Ref. [2].)

That defects located within the oxide can sometimes communicate very rapidly with the Si is illustrated in Fig. 3. Here we show spin-dependent-recombination experiments at GHz frequencies performed on irradiated hard and soft oxides by Jupina and Lenahan [14]. In addition to the P_{b0} center due to interface traps that was expected, they also found a signal due to an E' center, which is an oxide trap [14,15]. This reinforces the point

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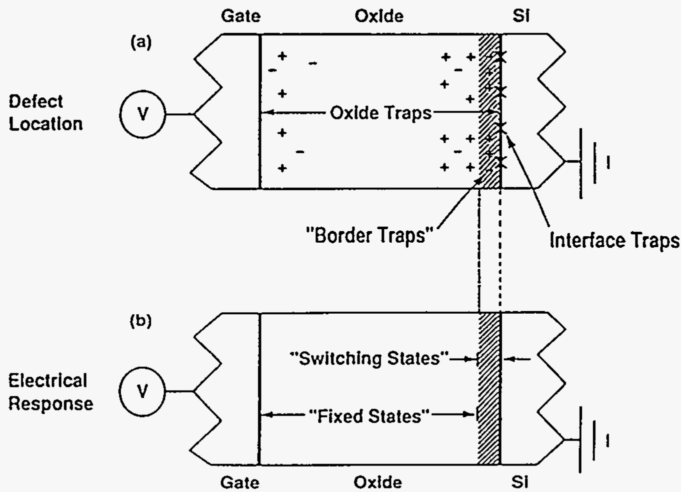

Figure 2: Schematic illustration of defects in MOS devices. Border traps are near-interfacial oxide traps that exchange charge with the Si during the measurements. (After Refs. [11,12].)

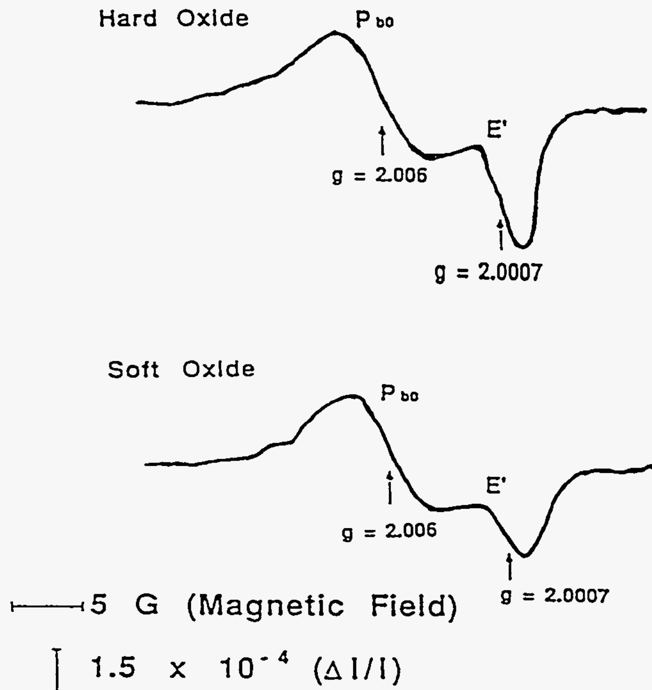

Figure 3: P_{b0} and E' spin dependent recombination (SDR) spectra for MOSFETs with hard or soft 37-nm oxides exposed to 5 Mrad(SiO_2) Co-60 irradiation at +5 V. The SDR measurement frequency was ~ 9.5 GHz. (After Ref. [14]; reprinted by permission.)

that one cannot always presume that defects that communicate with the Si during fast electrical measurements are interface traps. Time-resolving methods and/or techniques sensitive to defect microstructure are required to determine whether "switching states" in a given study are interface or border traps [11,12,16].

II. C-V Hysteresis

The Deal committee nomenclature notwithstanding, it has long been recognized that the "slow states" responsible for C-V hysteresis are oxide traps. This is one measure of the effective density of border traps with charge exchange times greater than or equal to ~ 1 s. An example of C-V hysteresis is provided in Fig. 4 for irradiated MOS capacitors; similar hysteresis due to border traps is also observed for capacitors subjected to high-field stress [17]. The asterisks are the C-V curves swept from accumulation to inversion; the triangles are the curves from inversion to accumulation; and the dots (lower peaked curve) are the differences in capacitance between the forward and reverse curves, which is proportional to the border-trap energy distribution [16,17].

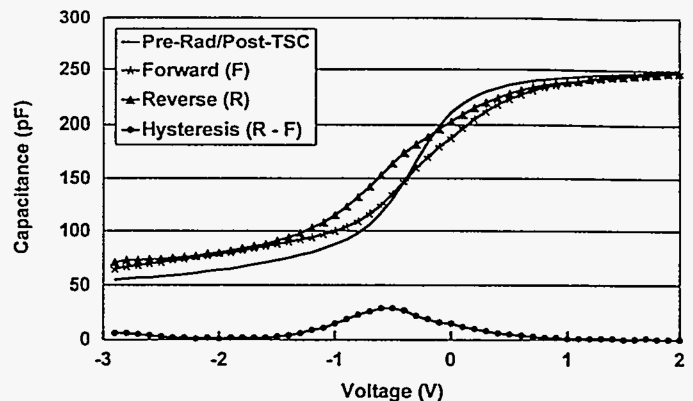

Figure 4: High-frequency C-V curves at a ramp rate of 0.5 V/s for 0.0013 cm^2 n-substrate capacitors with 17-nm thermal oxides irradiated to 2 Mrad(SiO_2) with 10-keV x rays at +4 V. (After Ref. [17].)

The effects of changing the ramp rate during the high-frequency C-V measurement on the measured C-V hysteresis are shown in Fig. 5 for a different type of device. Slowing the ramp rate allows defects further from the interface to exchange charge with the Si during the sweep. The linear increase of the hysteresis voltage with the logarithmic decrease in ramp time is consistent with border traps communicating with the Si via tunneling or thermally activated processes [5,6,13,16,18].

Figure 6 shows a correlation between the C-V hysteresis and E_γ' center density measured via electron paramagnetic resonance (EPR) in hole-injected oxides that had received a high-temperature N_2 anneal to increase their oxygen vacancy density [19]. The increase in C-V hysteresis, attributed to border traps, exactly mirrors the increase in E_γ' center density. This suggests that E_γ' centers can function as slow border traps. The unusual increase in border-trap and E_γ' density with anneal time is due to the conversion of E_δ' centers, which are metastable bulk oxide traps, into E_γ' centers [19]. Some E_γ' centers act as bulk oxide traps. Others, closer to the interface, serve as border traps, though with slower charge exchange times than the SDR-active centers in Fig. 3.

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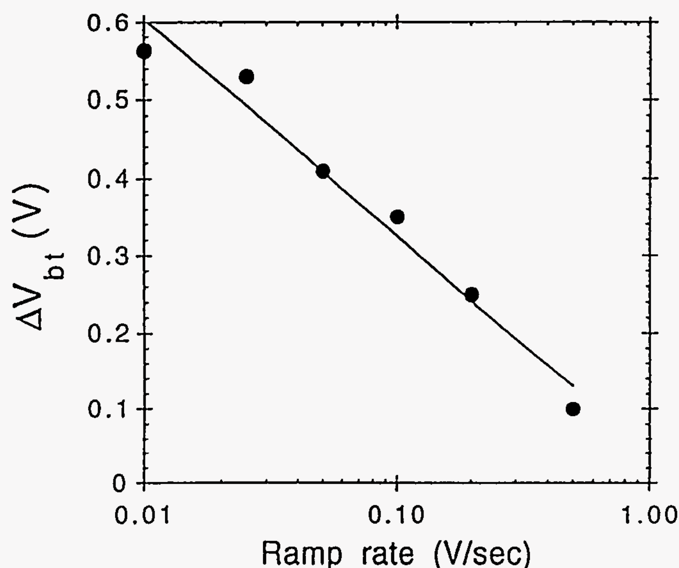

Figure 5: Hysteresis in C-V midgap-voltage as a function of ramp rate for capacitors with 45-nm soft oxides irradiated to 2 Mrad(SiO_2) with 10-keV x rays at +5 V bias. (After Ref. [16].)

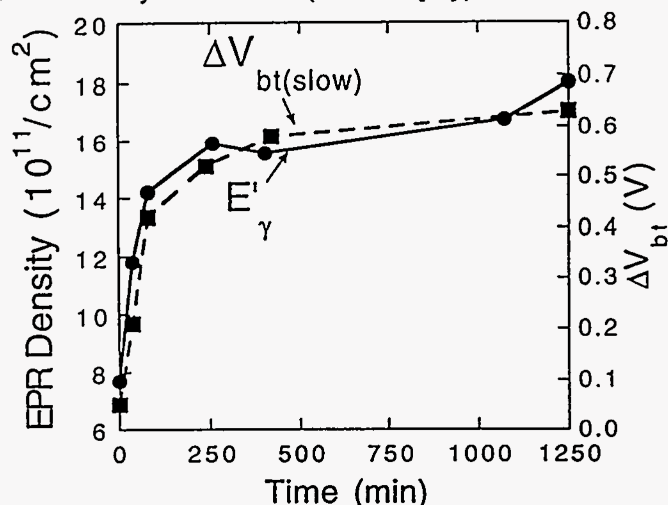

Figure 6: Density of E_γ' centers (left-hand scale) measured via electron paramagnetic resonance and midgap C-V hysteresis (right-hand scale) for oxides injected with ~ 6 x 10^{12} cm^{-2} holes. Samples were unbiased at room temperature throughout the duration of the anneal. (After Ref. [19].)

III. Thermally Stimulated Current (TSC)

TSC measurements are useful in determining the total density of trapped positive charge in the oxide and its energy distribution [20,21]. Critical information about the nature of border traps can be determined from Fig. 7, in which the total integrated TSC charge is determined as a function of the bias applied during the TSC measurement. The net oxide-trap charge determined from C-V midgap voltage shifts, Q(CV), is also shown for comparison. For large negative bias, the TSC charge is constant, showing that all of the holes that detrap and transport across the oxide are being counted. The total TSC charge is much larger than would have been predicted from midgap C-V shifts, in the absence of compensating electrons [20,21]. The fall-off in TSC at smaller negative bias is due to space-charge effects that cause some holes to transport into the Si instead of across the oxide and into the gate, reducing the measured TSC [20]. Finally, very little TSC is observed under positive bias because electrons in border traps cannot overcome the barrier for injection into the bulk of the oxide. Thus, they do not contribute significantly to the TSC [20,22]. Trapped holes near the interface move only a short distance under positive bias before entering the Si, and also do not cause significant TSC [20]. We conclude from Fig. 7 and related TSC experiments that the electrons which compensate the trapped-hole charge are primarily located in border traps that are only present in large densities when holes are trapped in the oxide [12,20-22], and not in bulk electron traps.

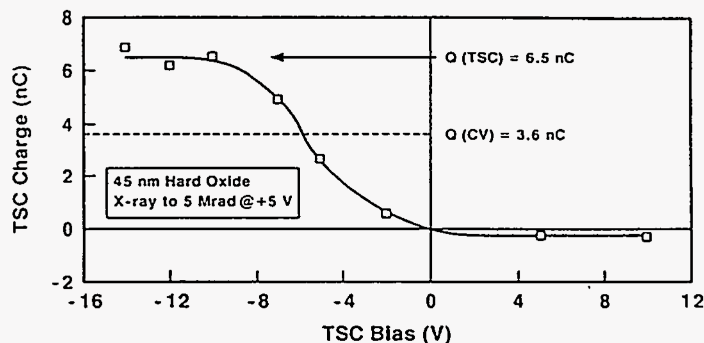

Figure 7: TSC charge vs. TSC bias for n-substrate capacitors with 45-nm radiation-hardened oxides, irradiated to 5 Mrad(SiO_2) with 10-keV x rays. The TSC was measured during a temperature ramp from 20°C to 350°C in 1 h, and the postirradiation TSC was corrected for background sources of leakage. (After Refs. [20,22].)

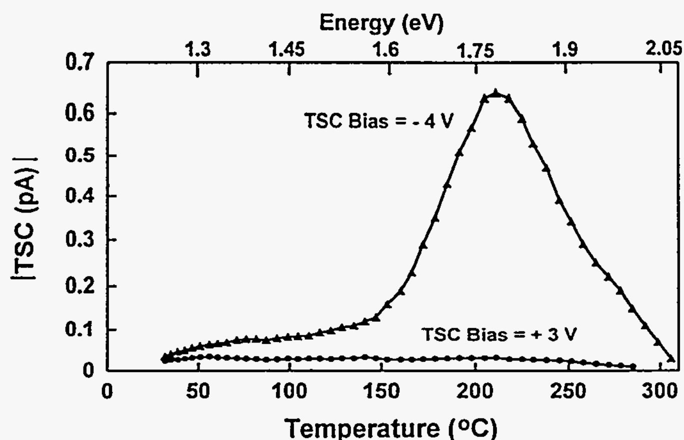

Figure 8: TSC corrected for background leakage vs. TSC bias for 0.0013 cm^2 n-substrate capacitors with 17-nm oxides exposed to 10 mC/cm^2 constant-current Fowler-Nordheim injection. The total trapped hole density was ~ 2.7 x 10^{12} cm^{-2}, with ~ 74% of the holes compensated by electrons in border traps. The sign of the TSC is positive for -4 V bias, and negative for +3 V. (After Ref. [17].)

That the results of Fig. 7 are not unique to ionizing radiation exposure is shown in Fig. 8. Here we show the TSC for capacitors with 17-nm oxides that were subjected to 10 mC/cm^2 constant-current Fowler-Nordheim stress under positive gate bias. For -4 V TSC bias, the current is large and positive, showing that a large number of holes trapped during the high-field stress are emitted and transport across the oxide during the TSC measurements. Moreover, the shape of the curve shows that the energy distribution of holes trapped during high-field stress is similar to that of holes trapped during radiation exposure [17]. Despite the large density of compensating electrons in border traps ($\sim 2 \times 10^{12}$ cm^{-2}), very little TSC is observed under positive bias. So, as for radiation exposure, most of the electrons in the oxide after modest high-field stress are in border traps, and not bulk electron traps [17]. Thus, conclusions drawn about the nature of the predominant border traps in irradiated oxides are likely to apply to oxides subjected to high-field stress as well. This reinforces the importance of border traps to MOS long-term reliability [16,17].

IV. Fast Border Traps

TSC and C-V hysteresis methods to estimate border-trap densities are primarily sensitive to defects that exchange charge with the Si on time scales greater than ~ 1 s. Faster border traps are not usually distinguishable from interface traps in standard subthreshold current-voltage (I-V) and C-V techniques [12,23]. However, methods have been developed to take advantage of the fact that border traps, which lie in the oxide, must exchange charge with the Si on a slower time scale than interface traps, which are in direct communication with the Si [5-8,11,13]. For example, a dual-transistor border-trap (DTBT) method has been developed at Sandia that combines fast (~ 1 MHz) charge pumping (CP) and slow (~ 1 Hz) threshold-voltage (Vth) measurements to separate the effects of interface traps and faster border traps [24,25]. During the CP measurements, it is primarily the interface traps that exchange charge with the Si [5-8]. During Vth measurements, interface traps and border traps with time constants between ~ 1 μs and ~ 1 s exchange charge with the Si. The difference between these fast and slow estimates of switching-state density provides a useful estimate of the fast border-trap density [16,24,25].

Figures 9(a) and (b) show values of the bulk oxide-trap charge density (ΔN_{ot}), interface-trap density (ΔN_{it}), and fast border-trap density (ΔN_{bt}) for MOS transistors with hardened 25-nm oxides with two different length-to-width (L/W) ratios. Comparing Figs. 9(a) and (b), it can be seen that border traps are much more significant for the 1.2-μm-long device than the 50-μm-long device. These results are consistent with 1/f noise estimates of border-trap density on the same time scale [24]. This illustrates that transistor geometry can have a large effect on the density of border traps in a given device, perhaps due to differences in the near-interfacial stress. Therefore, it may not be simple to predict MOS radiation response and 1/f noise in submicron devices on the basis of simple scaling laws [26].

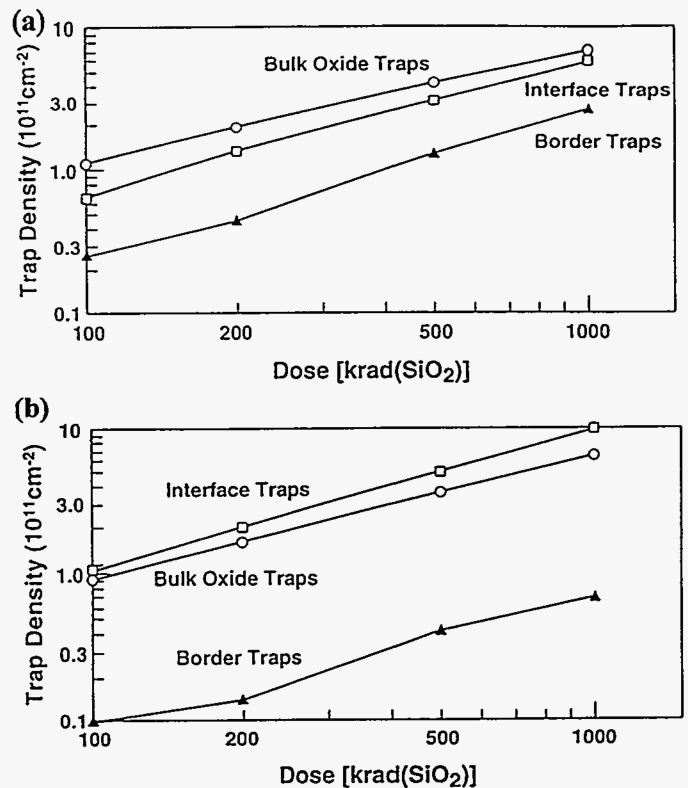

Figure 9: Bulk-oxide-trap, interface-trap, and border-trap charge densities vs. dose for MOS transistors with hardened 25-nm oxides irradiated with 10-keV x rays at a bias of 5 V: (a) L/W = 1.2 μm/50 μm, and (b) L/W = 50 μm/50 μm. (After Ref. [24].)

DiMaria et al. have also compared charge pumping estimates of ΔN_{it} with C-V estimates of the total "switching-state" density (N_s) in transistors with 24.5 nm oxides subjected to high-field stress [27]. Results are shown in Fig. 10. The C-V estimate, sensitive to both interface traps and border traps, shows a large increase in N_s at low injected fluence levels that is not present in the CP measurements. This is not observed unless a significant density of net positive charge (N_p, in Fig. 10) is also present in the oxide. Thus, the work of DiMaria et al. [27] suggests that there are border traps in

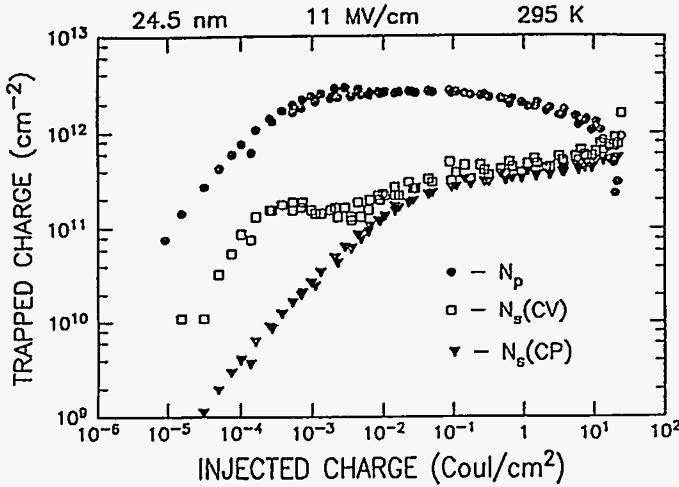

Figure 10: Net trapped-positive-charge density (N_p) and fast and slow switching-state densities (N_s) estimated via CP and C-V techniques for MOS transistors with 24.5-nm oxides. The decrease in N_p at large fluences is due to electron trapping at oxide traps created by the high-field stress. (After Ref. [27]; reprinted by permission.)

these stressed oxides, and that the border traps are associated with the trapped holes. Similar defects have been observed by Roh et al. in devices with 67.5 nm oxides subjected to high-field stress [28], and by Weber et al. in CP studies of hot-carrier effects [29]. Thus, dominant border traps in irradiated and stressed oxides are often associated with the presence of trapped positive charge, and it is likely that these are metastable electron traps associated with trapped holes [12].

V. Switched-Bias Annealing

In Sections III and IV, we discussed electrons in fast and slow border traps associated with trapped holes. Most of the work in the literature on this topic has been associated with attempts to understand the reversibility of the net positive charge in the oxide, and/or interface-trap densities, after irradiation or high-field stress [12,23,25,30-45]. In the first observation of the reversibility of radiation-induced trapped-positive-charge annealing by Schwank et al., the switching in ΔN_{ot} was attributed to electrons filling metastable traps in the near-interfacial oxide region (i. e., border traps) under positive bias, and leaving the traps under negative bias [30]. This picture was focused more sharply by Lelis et al. [34,35], who proposed a microscopic model in which an E_γ' center reversibly exchanges an electron with the Si. It has also been suggested that "anomalous positive charge (APC)," which is a slow donor state that is not associated with trapped holes, may lead to similar switching effects, especially in the absence of a significant density of trapped holes [33,40,42,44].

In a recent study at Sandia, effects of fast border traps on switched-bias annealing response were separated from interface trap effects for the first time [25]. The fast border trap density was estimated via the DTBT method, and the slower border-trap density was estimated from reversibility in "bulk" oxide-trap charge density. One example of these effects is shown in Fig. 11. An important point in Fig. 11 [25] is that fast border traps change less with biased annealing than slow border traps, suggesting they may be different defects, as discussed further below. The reader is directed to Ref. [25] for additional discussion of this and related work.

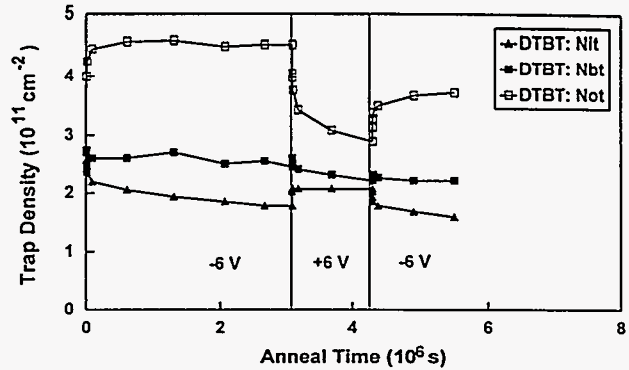

Figure 11: ΔN_{it}, ΔN_{bt}, and ΔN_{ot} for MOS transistors with soft 45-nm oxides irradiated with 10-keV x rays to 45 krad(SiO_2). Devices were annealed at +6 V for 8 weeks at room temperature and 6 weeks at +6 V at 80°C before the anneal bias was switched to -6 V here. The anneal temperature was 80°C. (After Ref. [25].)

VI. Border-Trap Models

A. O-Vacancy Related Defects.

Evidence that the slower border trap in Fig. 11 may be an E_γ' center is provided by the C-V hysteresis and EPR measurements of Warren et al. in Fig. 6 above [19]. Moreover, Conley et al. have recently shown that the E_γ' density can show a dramatic reversibility similar to that of the net oxide-trap charge [45], as shown in Fig. 12. This strongly reinforces the idea that E_γ' centers can serve as slow border traps. The earlier SDR data of Jupina and Lenahan (Fig. 3) also suggest that a type of E' center may also be responsible for the fast border traps [14], though it may not be an E_γ' center.

Figure 13 shows a schematic illustration of interface traps and fast and slow border traps based on electrical, EPR, and SDR data reviewed here, as well as much other related work [25]. The interface trap is the well-known P_b center discussed extensively in the literature [15,36,46,47]. Thus, site (1) in Fig. 6 is a Si dangling

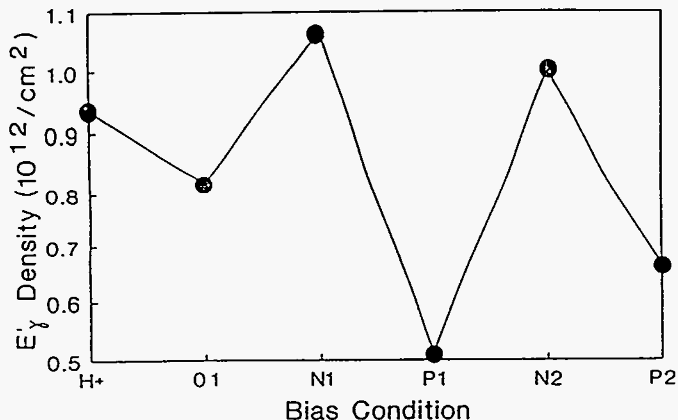

Figure 12: E_γ' center density measured via EPR for oxides subjected to alternating negative and positive bias anneals following vacuum ultraviolet hole injection. (After Ref. [45]; reprinted by permission.)

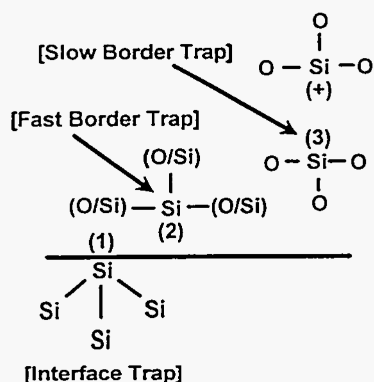

Figure 13: Schematic illustration of interface traps (P_{b0} defects), and possible fast ($O_{3-x}Si_xSi$ •) and slow (E_γ') border traps in SiO_2. The E_γ' without Site (3) is a bulk oxide trap. Sites (1) and (2) are amphoteric, and are charged positively at large negative bias and negatively at large positive bias. Site (3) is neutral at large negative bias and negative at large positive bias. (After Ref. [25].)

bond at the interface, which is an amphoteric defect [15,47]. The slow border trap depicted in Fig. 13 is the version discussed by Lelis et al. in 1989, where the defect may be altered by strain near the interface [35,43,45]. The very large electric fields near the interface may also assist in maintaining the dipolar nature of these slow border traps, by inhibiting a stable reformation of the broken bond between the two Si atoms [25]. The model of the E_γ' defect pictured in Fig. 13 also seems to be consistent with energy level calculations by O'Reilly and Robertson [48] and Chu and Fowler [49].

One candidate for the fast border trap in Fig. 13 is the $O_{3-x}Si_xSi$• family of defects [25]. For x = 0, the Si atom above Site 2 in Fig. 6 is surrounded by three O atoms. This is the E_s' defect [50], which is essentially one half of the E_γ' center (see Fig. 13). This center is known to have gap states, which are emphasized by O'Reilly and Robertson to be similar to those of the E_γ' center [48,51]. For x = 3, the Si atom above Site (2) is surrounded by three Si atoms, forming the D center [52], which is a Si cluster in the oxide that looks very much like a P_b. So it should not be surprising that such a defect might act like an interface trap, only switching more slowly since it is in the near-interfacial oxide instead of at the interface. Cases for x = 1 or 2 are similar to structures invoked by Poindexter et al. to describe the P_{b1} center at the (100) Si/SiO_2 interface [53], though this hypothesis remains somewhat controversial.

The $O_{3-x}Si_xSi$• family of defects show EPR signals only when neutral. The E_s' defect shows a resonance quite similar in line-shape to the E_γ' [50]. Thus, it may be the E_s' that was observed by Jupina and Lenahan via SDR in Fig. 3 [14], a technique that should *only* be sensitive to interface traps and the fastest border traps. Before irradiation, it is likely that $O_{3-x}Si_xSi$• defects are passivated by H or OH bonds [54,55]. These can be broken by processes similar to those leading to interface-trap formation [36,47]. Thus, just as Si dangling bond defects at the interface can serve as interface traps, Si dangling bond defects distributed into the oxide evidently can function as fast or slow border traps, depending on their distance from the interface.

B. H-Related Defects.

Much of the switching response often observed in MOS devices after irradiation or high-field stress [30-45] is similar to classic bias-temperature instabilities in SiO_2. These are often attributed to the polarization and subsequent decomposition of water near the interface [56], suggesting some reversibility in net oxide- and interface-trap charge may also be due to the motion of charged H-related species–e.g., $(OH)^-$, $(H_3O)^+$, and/or H^+–liberated by bond breaking during irradiation. These may be exchanged between the near-interfacial oxide and near-surface Si during switched-bias anneals. This process is also consistent with the association of hydrogen with APC in many studies [33,37,40,44].

VII. Conclusions

A wide variety of experimental techniques demonstrate that border traps can significantly affect MOS 1/f noise, radiation response, and long-term reliability. Because different process treatments may be required to optimize the quality of the Si/SiO_2 interface, the near-interfacial region of the oxide in which border traps are found, and the bulk of the oxide, it is important to assess

the relative importance of border traps in the devices of interest. Border traps will be increasingly important in thinner oxides, simply because the number of truly "bulk-like" oxide traps will be reduced [11,13]. For a thin enough oxide (e. g., less than ~ 3-6 nm), all oxide traps will be border traps! Moreover, transistor geometry can significantly affect the density of border traps in a given device [26]. So it may not be simple to predict MOS radiation response and 1/f noise in submicron devices on the basis of simple scaling laws derived from larger devices. Therefore, it will be important to improve our understanding of how best to estimate the densities of border traps in MOS devices, and to mitigate their impact on device electrical response.

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