OCT 29 1999

SANDIA REPORT

SAND99-2127

Unlimited Release

Printed October 1999

RECEIVED
NOV 02 1999
OSTI

Reliability Impact of Stockpile Aging: Stress Voiding

David G. Robinson

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia Corporation,
a Lockheed Martin Company, for the United States Department of
Energy under Contract DE-AC04-94AL85000.

Approved for public release; further dissemination unlimited.

Sandia National Laboratories

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

NOTICE: This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government, nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors, or their employees, make any warranty, express or implied, or assume any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represent that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government, any agency thereof, or any of their contractors or subcontractors. The views and opinions expressed herein do not necessarily state or reflect those of the United States Government, any agency thereof, or any of their contractors.

Printed in the United States of America. This report has been reproduced directly from the best available copy.

Available to DOE and DOE contractors from
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Prices available from (703) 605-6000
Web site: <http://www.ntis.gov/ordering.htm>

Available to the public from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Rd
Springfield, VA 22161

NTIS price codes
Printed copy: A03
Microfiche copy: A01

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

SAND 99-2127

Unlimited Release
Printed October 1999

Reliability Impact of Stockpile Aging: Stress Voiding

David G. Robinson
Systems Reliability
Sandia National Laboratories
P.O. Box 5800
Albuquerque, NM 87185-0746
drobin@sandia.gov

Abstract

The objective of this research is to statistically characterize the aging of integrated circuit interconnects. This report supercedes the stress void aging characterization presented in SAND99-0975, "Reliability Degradation Due to Stockpile Aging," by the same author. The physics of the stress voiding, before and after wafer processing have been recently characterized by F. G. Yost in SAND99-0601, "Stress Voiding during Wafer Processing". The current effort extends this research to account for uncertainties in grain size, storage temperature, void spacing and initial residual stress and their impact on interconnect failure after wafer processing. The sensitivity of the life estimates to these uncertainties is also investigated. Various methods for characterizing the probability of failure of a conductor line were investigated including: Latin hypercube sampling (LHS), quasi-Monte Carlo sampling (qMC), as well as various analytical methods such as the advanced mean value (AMV) method. The comparison was aided by the use of the Cassandra uncertainty analysis library. It was found that the only viable uncertainty analysis methods were those based on either LHS or quasi-Monte Carlo sampling. Analytical methods such as AMV could not be applied due to the nature of the stress voiding problem. The qMC method was chosen since it provided smaller estimation error for a given number of samples. The preliminary results indicate that the reliability of integrated circuits due to stress voiding is very sensitive to the underlying uncertainties associated with grain size and void spacing. In particular, accurate characterization of IC reliability depends heavily on not only the first and second moments of the uncertainty distribution, but more specifically the unique form of the underlying distribution.

Contents

Abstract.....	4
1. Stress Voiding	4
1.1 Notation	4
1.2 Model Summary.....	5
2. Reliability-based Aging Analysis.....	7
2.1 Cassandra Uncertainty Library	7
2.2 Distribution Assumptions.....	8
2.3 Summary of Results	9
2.4 Sensitivity Analysis.....	11
3. Discussion	13
4. Acknowledgements	14
References	14

Figures

Figure 1. Time to Failure versus λ and $\bar{l}$	6
Figure 2 Time to Failure versus λ and s_o	7
Figure 3 Probability Density Functions for Random Variables	8
Figure 4 CDF for Various Mean Void Spacing	9
Figure 5 CDF for Various Mean Grain Sizes	10
Figure 6 Void Spacing PDF versus Time to Failure	10
Figure 7 Sensitivity of CDF to Random Parameters.....	11
Figure 8 Sensitivity of CDF to Distribution Selection	12
Figure 9 Impact of Process Control on Interconnect Reliability	13

Tables

Table 1 Statistical Properties	8
Table 2 Test Cases.....	1

Reliability Impact of Stockpile Aging: Stress Voiding

Abstract

The objective of this research is to statistically characterize the aging of integrated circuit interconnects and supercedes the stress void aging characterization presented in SAND99-0975, "Reliability Degradation Due to Stockpile Aging," by the same author. The physics of the stress voiding, before and after wafer processing have been previously characterized by F. G. Yost in SAND99-0601, "Stress Voiding during Wafer Processing". The current effort extends this research to account for uncertainties in grain size, storage temperature, void spacing and initial residual stress and their impact on interconnect failure after wafer processing. The sensitivity of the life estimates to these uncertainties is also investigated. Various methods for characterizing the probability of failure of a conductor line were investigated including: Latin hypercube sampling (LHS), quasi-Monte Carlo sampling (qMC), as well as various analytical methods such as the advanced mean value (AMV) method. The comparison was aided by the use of the Cassandra uncertainty analysis library. It was found that the only viable uncertainty analysis methods were those based on either LHS or quasi-Monte Carlo sampling. Analytical methods such as AMV could not be applied due to the nature of the stress voiding problem. The qMC method was chosen since it provided smaller estimation error for a given number of samples. The preliminary results indicate that the reliability of integrated circuits due to stress voiding is very sensitive to the underlying uncertainties associated with grain size and void spacing. In particular, accurate characterization of IC reliability depends heavily on not only the first and second moments of the uncertainty distribution, but more specifically the unique form of the underlying distribution.

1. Stress Voiding

Yost has previously characterized void growth kinetics in Al interconnects during and after wafer processing [Yost, 1999]. The results were shown to be consistent with both experimental observations and published literature. Of particular note was the conclusion that interconnects with higher void density had a longer expected life. This is a bit counter-intuitive since a high void density is generally indicative of a 'dirty' manufacturing process. It should be remembered however, that the quenching process during manufacturing inhibits the initiation and growth of voids during manufacturing but results in a high residual stress on the conductor lines after processing. Further, this residual stress is concentrated at the few void locations on the conductor line and the stress is relieved through the subsequent growth of the voids during storage. The fewer the number of voids, the faster and further each must grow to relieve the residual manufacturing stress.

1.1 Notation

The notation is consistent with that prescribed by Yost [Yost 1999].

$A(t)$ void area (μm^2)

$\sqrt{A(t)}$ void length (μm)

k Boltzman's constant = 1.30658×10^{-23} J/°K

Ω	atomic volume for Aluminum = 1.723246×10^{-21} cm ³
Q_v	bulk diffusion activation energy (eV)
δD_b	grain boundary diffusion coefficient (cm ³ / s)
Q_b	grain boundary diffusion activation energy (eV/mole)
δD_{ob}	constant from literature (10^{-10} cm ³ / s)
λ	grain size (μ m)
t	time
$\bar{l}$	average void spacing (μ m)
b	line width (μ m)
$s(t)$	conductor line stress (MPa)
T_k	absolute temperature ($^{\circ}$ K)
T_c	temperature ($^{\circ}$ C)
R	ideal gas constant 8.314 (J / mole - K)
E	modulus of elasticity (MPa)
D_{ov}	pre-exponential factor (cm ² / s)
D_v	pre-exponential factor (cm ² / s)
$\dot{\epsilon}$	total strain rate = $\dot{\epsilon}_p + \dot{\epsilon}_d$
$\dot{\epsilon}_p$	plasticity component of strain rate
$\dot{\epsilon}_d$	diffusive component of strain rate
μ	shear modulus
Λ	experimentally determined constant = 3.4×10^6
m	experimentally determined constant = 4.4
v_b	magnitude of Burger's vector (= 4.05×10^{-8} cm)

1.2 Model Summary

The following highlights the model development by Yost. It is assumed that voids initiate at roughly the same time during the manufacturing process and that the voids are uniformly distributed across the conductor line with an average spacing of $\bar{l}$. In addition, it is assumed that the components containing the interconnects are stored in an isothermal environment.

Grain Boundary Diffusion Activation Energy

$$Q_b = 0.944 - \frac{0.609}{\sqrt{\lambda}} \quad (\text{eV / atom})$$

Grain Boundary Diffusion Coefficient

$$\delta D_b = \delta D_{ob} \exp\left(-\frac{Q_b}{RT_k}\right) \quad (\text{cm}^3 / \text{sec})$$

Young's Modulus

$$E(T_c) = 71393 - 3922T_c$$

 Figure 1. Time to Failure versus λ and $\bar{l}$

Strain Rate Equation

$$\frac{dA(t)}{dt} = \bar{l} \{b - \sqrt{A(t)}\} \dot{\epsilon}$$

where:

$$\dot{\epsilon} = \dot{\epsilon}_p + \dot{\epsilon}_d$$

$$\dot{\epsilon}_p = \Lambda \frac{D_v \mu v_b}{kT_k} \left[\frac{s(t)}{\mu} \right]^m$$

$$\dot{\epsilon}_d = \left[\frac{10}{\lambda^2} D_v + \frac{148}{\lambda^3} \delta D_b \right] \frac{\Omega s(t)}{kT_k}$$

Assuming existence of initial stress, s_o , and an isothermal environment the following equations result:

$$\sqrt{A_o} - \sqrt{A(t)} - b \ln \left[\frac{b - \sqrt{A(t)}}{b - \sqrt{A_o}} \right] = \frac{\bar{l}}{2E} [1 - \exp(-\Psi E t)]$$

$$s(t) = s_o \exp(-\Psi E t)$$

where:

$$\Psi = \frac{148 \delta D_b \Omega}{\lambda^3 k T_k} (\text{MPa} \cdot \text{s})^{-1}$$

With the use of the above equations, a deterministic analysis of the expected life of an integrated circuit can be accomplished. Figures 1 and 2 depict the expected life as a function of void spacing, grain size and initial stress.

2. Reliability-based Aging Analysis

2.1 Cassandra Uncertainty Library

The Cassandra uncertainty library [Robinson, 1999] consists of a number of software routines that permit the user to select a variety of methods for including uncertainty in their analyses. A number of first and second order techniques, max-likelihood and a variety of other analytical methods are available for application. In addition, there are options for using a number of pseudo- and quasi-Monte Carlo methods. Specific methods are constantly being updated and improved. Cassandra is written completely in C/C++ making the engine very portable; it has been used with Win95, WinNT, Power Macintosh, Sun, Silicon Graphics and DEC operating systems. In addition, the software has been ported to one of the large tera-flop computers at Sandia.

Access to the Cassandra uncertainty analysis engine is gained via the CRAX interface. The CRAX graphical user interface (GUI) is based entirely on the Tool Command Language (Tcl) and the associated Tool Kit (Tk). The graphical user interface is also platform independent and provides a great deal of flexibility in using the Cassandra uncertainty engine.

All analyses were performed using quasi-Monte Carlo sampling technique within the Cassandra library [Robinson and Atcitty, 1999].

2.2 Distribution Assumptions

Table 1 summarizes the means and coefficients of variation that were assumed for the initial analysis. Since all variables are naturally defined on a positive support (only take on positive values), the underlying probability density function for each variable was logically assumed to be either lognormal or Weibull (Figure 3). The sensitivity of the results to the specific distributional form was also investigated and is discussed later.

Variable	Mean	Coefficient of Variation
Grain Size	1.5 (μm)	0.21
Initial Stress	550 (Mpa)	0.1
Storage Temperature	293 ($^{\circ}\text{K}$)	0.05
Void Spacing	700 (μm)	0.1

Table 1. Statistical Properties

2.3 Summary of Results

The following results are based on an interconnect line with width $b = 2 \mu\text{m}$. Failure is assumed to occur when the void propagates to a width equal to $0.85b$. Figure 4 depicts the impact of various underlying mean void spacing (keeping all other statistical characteristics constant). Clearly the characterization of void spacing is critical to understanding the reliability impact of stress voiding. The association of decreasing failure probability with decreasing mean void spacing is rather counter-intuitive since a smaller void spacing represents a 'dirtier' integrated circuit production environment.

A similar investigation into the impact of various mean grain size values is summarized in Figure 5. It is interesting to note that in this case the mean grain size does not impact the long term storage reliability of the integrated circuit. However, it does impact the initial reliability by inhibiting void growth – larger grain size is associated with slower void growth.

Figure 5. CDF for Various Mean Grain Sizes

It is important to observe that each of these cumulative distribution curves are not asymptotic to 1.0; not pictured is the instantaneous jump to 1.0 at $t = \infty$. To appreciate why the probability of failure increases so rapidly at $t \rightarrow \infty$, it is informative to observe the relationship between the deterministic void growth function and the probability density function for void spacing. As can be seen in Figure 6 the likelihood of small void spacing in the lower regions leads to a very substantial decrease in the probability of failure (for temperature = 293K, grain size = 6 μm). In summary, what is happening is, for a given spacing of voids, there is a time at which the stress

Figure 6. Void Spacing PDF versus Time to Failure

has decreased to such a level that the voids cease to grow. If the voids have not already reached a critical level, then the voids will never reach a critical level and the interconnect can not fail.

2.4 Sensitivity Analysis

The contribution of each variable to the cumulative probability of failure is depicted in Figure 7. These sensitivities represent the importance of each random variable to the probability of failure as the system ages. Often as the system ages, the sensitivity of the system to parameter uncertainty will also change; this does not appear to be the case in this situation as the sensitivities remain fairly constant. The sensitivity values can range from -1 to 1 . The larger in magnitude, the more contribution the particular random variable makes to the probability of failure. The sign of the sensitivity for a random variable relates to which portion of the associated underlying probability density function is contributing to the probability of failure. Negative sensitivities, in general, indicate that the lower portion of the density function is important. These are often referred to as 'stress' variables. Alternatively, positive sensitivities are associated with those random variables whose dominate contribution to the probability of failure comes from the upper tail. In a similar fashion, these variables are referred to as 'strength' variables. This stress/strength generalization is complicated by the possible interaction between the mean and variance of the underlying distribution, as occurs when the underlying probability density function is assumed to be lognormal.

Ignoring the sign of the sensitivity values, it is clear that, as the interconnect ages, the random

Figure 7. Sensitivity of CDF to Random Parameters

nature of the grain size is the most critical parameter in characterizing the life of the interconnect. To a lesser extent (but still important), the reliability of the interconnect depends on the void spacing and the residual stress.

Apart from the mean and the variance of the underlying distribution, a critical element in assessing the reliability is the actual form of the distribution. As noted earlier, the sensitivity analysis (positive and negative values) indicates which portion of the underlying probability

density function is critical to the analysis. To better understand the implications of the sensitivity analysis on distribution selection, three separate cases are investigated (Table 2) and summarized in Figure 6. Case 1 is the original problem but with a mean void spacing of 600 μm . Case 2 involves the same mean and coefficient of variation as Case 1, but assumes that the underlying distribution for the void spacing is Weibull rather than lognormal. From the sensitivity analysis (Figure 7), the results are seen to be sensitive to the lower tail of the distribution. Since the Weibull distribution assumption increases the area in the lower tail (Figure 3), it is expected that the probability of failure would also increase. The resulting analysis depicted in Figure 8 confirms this insight. As a second example, from the sensitivity analysis it is clear that the assumption of underlying distribution for the storage temperature should not significantly impact the final analysis: the lower tail area is indifferent to the assumption of the underlying distribution. An examination of Figure 8 again confirms this conclusion.

The implication of this is that, when characterizing the reliability of the interconnects, it is critical to have sufficient data to justify the selection of an underlying distribution for void

Variable	Case 1			Case 2			Case 3		
	PDF	Mean	CoV	PDF	Mean	CoV	PDF	Mean	CoV
Grain Size	lognormal	1.5 (μm)	0.2	lognormal	1.5	0.2	lognormal	1.5	0.2
Initial Stress	lognormal	550 (Mpa)	0.1	lognormal	550	0.1	lognormal	550	0.1
Temperature	lognormal	293 ($^{\circ}\text{K}$)	0.005	lognormal	293	0.005	Weibull	293	0.005
Void Spacing	lognormal	600 (μm)	0.1	Weibull	600	0.1	lognormal	600	0.1

Table 2. Test Cases

spacing.

Figure 9. Impact of Process Control on IC Reliability

It is generally desired to have a manufacturing process under strict statistical process control. This will logically result in a decrease in the variation of void spacing of the interconnects. To appreciate the impact of improving process control on the reliability of the interconnect, the coefficient of variation of the void spacing is explored over a wide range in Figure 9. For illustration purposes, assume a mean void spacing of $550 \mu\text{m}$ while maintaining all other parameters as described in Table 1. As can be seen, the initial, short-term reliability is improved. However, tightening the process control limits can severely degrade the long term reliability of the integrated circuit.

3.0 Discussion and Recommendations

The above analysis provides a foundation for an extremely counterintuitive result: as the manufacturing process becomes more 'corrupt' the storage reliability characteristics of the component improve. As the mean void spacing drops below approximately $60 \mu\text{m}$ the reliability of the interconnect becomes extremely difficult to characterize. At roughly this point, the dominate portion of the void space distribution is below the critical level at which there is insufficient residual stress to cause the voids to grow to an appreciable length (see Figure 6). The probability of failure of the interconnect in this situation, for this failure mode, is then essentially zero.

As noted in section 2.5, the predicted reliability of the interconnect is very sensitive to the assumed underlying probability density functions. To accurately characterize interconnect reliability in a storage environment, it will be critical to collect adequate information to justify the assumption of a particular distribution. Simple mean and standard deviation estimates will not be sufficient for accurate life-length prediction.

Accurate reliability predictions will require a formal set of experiments based on the objective of statistically characterizing the underlying probability distributions of the important factors such

as grain size and void spacing. Statistical information regarding weapon system storage conditions is being pursued as part of a parallel corrosion effort.

The sensitivity of the results to grain size is clear from Figure 7. In addition, accurate characterization of the grain boundary diffusion activation energy, Q_b , as a function of grain size, λ , is essential for confident reliability estimates. Unfortunately, the relationship used in the above analysis was based on only three data points, acquired from a variety of sources. Additional experimentation in this area is essential to validate the functional relationship.

4.0 Acknowledgements

This research was conducted with support from the Sandia National Laboratories Enhanced Surveillance Program. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000. The author wishes to particularly thank Lee Eubanks GRAM, Inc. who did the majority of the programming associated with the above analyses and Dr. Yost for his insight into issues associated with this problem.

References

- Robinson, D., 1998, "A Survey of Probabilistic Methods Used in Reliability, Risk and Uncertainty Analysis: Analytical Techniques I," SAND98-1189, Sandia National Laboratories, Albuquerque, New Mexico, June.
- Robinson, D., C. Atcitty, 1999, "Comparison of Quasi- and Pseudo-Monte Carlo Sampling for Reliability and Uncertainty Analysis," AIAA 99-1589, AIAA Structures, Structural Dynamics and Materials Conference, St. Louis, MO, 12-15 April.
- Robinson, D., "CRAX/Cassandra Reliability Analysis Software," AIAA 99-1594, AIAA Structures, Structural Dynamics and Materials Conference, St. Louis, MO, 12-15 April, 1999.
- Yost, F.G., 1999, "Stress Voiding During Wafer Processing," SAND 99-0601, Sandia National Laboratories, Albuquerque, New Mexico, March.

Distribution

1	MS 1407	(1805)	R. J. Salzbrenner
1	MS 1411	(1834)	F. G. Yost
1	MS 0746	(6411)	R. M. Cranwell
1	MS 0747	(6412)	A. L. Camp
1	MS 0746	(6411)	D. J. Anderson
1	MS 0746	(6411)	L. A. Swiler
15	MS 0746	(6411)	D. G. Robinson
1	MS 0747	(6412)	G. D. Wyss
1	MS 9102	(8402)	M. W. Perra
1	MS 0819	(9231)	T. G. Trucano
1	MS 0439	(9234)	D. R. Martinez
1	MS 0829	(12323)	K. V. Diegert
1	MS0830	(12335)	J. M. Sjulín
1	MS 9018	(8940-2)	Central Technical Files
2	MS 0899	(4916)	Technical Library
1	MS 0612	(4912)	Review & Approval Desk for DOE/OSTI

TOTAL COPIES = 31