ADVANCED TECHNOLOGY FOR SOURCE DRAIN RESISTANCE REDUCTION IN NANO SCALE FINFETS

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Dual gate MOSFET structures such as FinFETs are widely regarded as the most promising option for continued scaling of silicon based transistors after 2010. This work examines key process modules that enable reduction of both device area and fin width beyond requirements for the 16nm node. Because aggressively scaled FinFET structures suffer significantly degraded device performance due to large source/drain series resistance ($R_{S/D}$), several methods to mitigate $R_{S/D}$ such as maximizing contact area, silicide engineering, and epitaxially raised S/D have been evaluated.
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LIST OF ABBREVIATIONS

ALD - Atomic layer deposition
AMAT - Applied Materials
AmSi - Amorphous silicon
BARC - Back anti-reflection coating
BOE - Buffered oxide etch
BOX - Buried oxide
BSE - Backscattered electron
CD - Critical dimension
CD-SEM - Critical dimension scanning electron microscope
CESL - Contact etch stop layer
CMOS - Complementary metal-oxide semiconductor
CPU - Central processing unit
c-Si - Crystalline silicon
CVD - Chemical vapor deposition
DG - Dual gate
DIBL - Drain induced barrier lowering
DUT - Device under test
EOT - Effective oxide thickness
FWHM - Full width at half maximum
GAA - Gate all around
GIXRD - Grazing incidence X-ray diffraction
GtD - Gate to drain
HDD - Heavily doped drain
HKMG - High-k metal gate
HM - Hard mask
IC - Integrated circuit
IL - Interlayer
ILD - Inter-layer dielectric
I_{OFF} - Off state drain current
ISSG - In-situ steam generation
ITRS - International Technology Roadmap for Semiconductors
LDD - Lightly doped drain
L_{eff} - Effective gate length
LER - Line edge roughness
Lg - Gate length
LPCVD - Low pressure chemical vapor deposition
LWR - Line width roughness
MOS - Metal-oxide semiconductor
MOSFET - Metal-oxide semiconductor field effect transistor
MugFET - Multiple gate field effect transistor
PECVD - Plasma enhanced chemical vapor deposition

PETEOS - Plasma enhanced TEOS

PVD - Physical vapor deposition

RCO - Contact resistance

RIE - Reactive ion etch

R_S - Sheet resistance

R_S/D - Source drain resistance

R_SP - Spreading resistance

RTP - Rapid thermal processing

S/D - Source/drain

SCE - Short channel effect

SE - Secondary electron

SEM - Scanning electron microscope

SIMS - Secondary ion mass spectrometry

SMU - Source monitor unit

SOI - Silicon on insulator

SPM - Sulfuric peroxide mixture

SRAM - Static random access memory

STI - Shallow trench isolation

SWT - Sidewall transfer

TEM - Transmission electron microscope
TEOS - Tetraethoxysilane

$T_{Si}$ - Silicon thickness

$V_{ds}$ - Potential difference between source and drain

$V_{TH}$ - Threshold voltage

WIW - Within wafer

WTW - Wafer to wafer
1. INTRODUCTION

1.1 Transistor Scaling

Following Jack Kilby’s revolutionary invention of the integrated circuit (IC) in 1958, the number of components in semiconductor microchips has increased exponentially resulting in cutting edge IC chips boasting more than 1.5 billion transistors per central processing unit (CPU). This increase is driven primarily by aggressive scaling of device dimensions and has led to dramatic reductions in both cost-per-operation and gate delay. These scaling trends have only recently altered course after more than 4 decades of close adherence to Gordon Moore’s law: IC complexity doubles every two years [1]. The dominant factors contributing to slowed device miniaturization include both lithographic and material property limitations. The following sections provide a brief overview of MOSFET operation and performance limitations that arise from aggressive scaling.

1.1.1 MOSFET Operation

Metal-oxide-semiconductor field-effect transistors (MOSFETS) rely on modulation of a thermal barrier between the oppositely doped channel and source/drain regions as illustrated in Figure 1.
For a zero gate bias and reasonable operation temperatures, the potential barrier at the source-channel and drain-channel junctions limits the magnitude of source-drain current and renders it independent of the potential difference between source and drain ($V_{ds}$). This situation represents an off-state for the device. Switching to the on-state requires a sufficient bias on the gate electrode to create an inversion layer in the channel thereby lowering the thermal barrier for carrier transport between source and drain. Bias conditions for flat band, accumulation, depletion, and inversion states across the metal oxide semiconductor (MOS) region are depicted in Figure 2.
Figure 2: band diagrams for various gate bias conditions in ideal p-type (left) and n-type (right) MOS structures where $E_f =$Fermi level energy , $E_c =$conduction band energy, $E_v =$Valence band energy, $V_g =$gate bias [2]

Unfortunately, maintaining this ideal “long channel” behavior for an identical (same dielectric, channel doping, $V_{ds}$ etc…) device with a reduced gate length is no longer feasible due to the short channel effect (SCE) which results in threshold voltage ($V_{TH}$)
As physical gate length ($L_g$) decreases, the depletion width near the S/D junctions comprises a larger portion of the channel region as depicted in Figure 3.

This depleted region already has a lower thermal barrier to carrier transport (see Figure 2: depletion condition) and its carrier population is no longer modulated by the gate electrode. Moreover, the portion of the channel still capacitively coupled to the gate electrode has been reduced to an effective gate length ($L_{eff}$) whose dimensions depend on the bias at the S/D electrodes, dopant concentration, and dopant distribution. The three primary side effects of this short channel behavior can be understood as follows:
• \( V_{TH} \) roll-off: a portion of the channel is already depleted and hence the gate electrode does not have to alter the potential at the dielectric interface near the source-drain junction as much to invert the channel \( \Rightarrow V_{TH} \text{ is reduced} \)

• S/D off state leakage: as the depletion width increases further into the body/channel area, a large \( V_{ds} \) results in carriers traversing through the body rather than the channel from source to drain, a phenomenon commonly referred to as “punch through” \( \Rightarrow I_{OFF} \text{ increases} \)

• DIBL: As the drain bias is increased to ensure velocity saturation of carriers in the channel, the depletion region near the drain electrode creeps further into the channel and undermines or replaces gate control of the transistor with drain control \( \Rightarrow I_{ds} \text{ becomes independent of } V_{gs} \)

1.1.2 Short Channel Effect

There are several means by which the device engineer can reign in the SCE including reduction of S/D junction depth, increasing dopant concentration in the channel, and decreasing the effective oxide thickness (EOT) of the gate dielectric. In addition to these process based solutions to control SCE for shrinking device dimensions, there exist fundamental limitations on device size that will be addressed in the following section.

Decreasing the S/D junction depth and increasing dopant concentration in the channel are techniques that almost exclusively apply to planar MOSFET structures and hence will not be treated here except to comment that for aggressively scaled 3D devices, the active area silicon volume is so miniscule that even high dose implants may result in only a few dopant atoms residing in the channel region. In addition, the inherent
variability of both position and number of dopant atoms in the channel would render device characteristics, such as $V_T$ and mobility, uncontrollable. The S/D junction depth in 3D MOSFET structures is typically based on a horizontal dopant front rather than a vertical one making uniform fin doping and activation of a much greater concern due to the narrow active volume in the S/D regions.

Reducing EOT results in increased capacitive coupling between the gate electrode and channel region. This implies a greater ease in altering the surface potential at the dielectric-channel interface that leads to inversion. EOT scaling progressed for many years simply by reducing the thickness of the gate dielectric thereby increasing its capacitance. At some point (<20Å) the electric field across very thin SiO$_2$ results in Fowler-Nordheim (in addition to direct) tunneling of carriers through the dielectric. This leads to unacceptable levels of gate leakage current that cause joule heating and higher power consumption [3-4]. The industry’s response to this apparent roadblock was to substitute a dielectric with a higher k-value such that comparable EOT can be achieved with a larger physical thickness to reduce tunneling probability. Nitridation of SiO$_2$ staved off the issue of gate leakage for some time but even this material caused mobility degradation as the carriers scattered off the newly introduced fixed charge that accompanied Nitrogen in the dielectric [5-7]. Moreover, the large band offset offered by a silicon-SiO$_2$ interface that limits Fowler-Nordheim tunneling is compromised when the gate dielectric is changed to Si$_3$N$_4$ or HfO$_2$ as shown in Figures 4 and 5 [8].
As with SiO₂, further reduction of gate dielectric thickness even for high-k materials will only exacerbate the gate leakage due to higher tunneling probability.

The current solution to maintain EOT < 10Å and simultaneously limit gate leakage involves the use of high-k gate dielectrics which are predominantly hafnium (Hf)
based [9-10]. These materials are much more sensitive to high temperature conditions
during subsequent processing and often require interface engineering to overcome
scattering mechanisms resulting from interfacial fixed charge [11]. It is interesting to
note that high-k gate dielectrics almost never come in contact with the channel. A
spontaneous and very thin SiO₂ interlayer (IL) will form between the high-k and silicon
channel despite attempts to remove any oxide prior to deposition. This IL is a mixed
blessing because it forms a very stable low defect density interface to the channel surface
that spatially separates carriers from fixed charge in the high-k that act as potential
scattering sites while at the same time increasing EOT. It should also be noted that the
channel surfaces in 3D devices may not necessarily be the silicon (100) plane and hence
may result in different interface state densities within the IL.

Another means of reducing EOT requires the use of metallic gate electrodes rather
than conventional polysilicon gates. In the same way that depletion occurs at the S/D
junctions, biasing a polysilicon gate results in the formation of a depletion region at the
dielectric interface. This depleted polysilicon now acts as a capacitor in series with the
gate dielectric and reduces EOT. Cutting edge devices at the 45nm node utilize both
high-k and metal gate (HKMG) material systems such that gate leakage is minimized for
operation voltage of ~1V [12]. Moreover, metal gate work function (φ₀) can be tuned by
a number of methods to lower the V_TH of the device [13]. In general, pMOS friendly
metals must have a large φ₀ such that the built-in potential one must overcome to invert
the channel is reduced while the reverse is true for nMOS metals [14]. Even though the
move to HKMG required millions of research dollars and tremendous efforts by hundreds
of scientists and engineers, nature’s fundamental gift to the semiconductor industry, the SiO₂/silicon interface, is still the core of device functionality.

1.2 Multiple Gate MOSFET

Shrinking device dimensions for successive planar transistor technology nodes require ever smaller EOT and channel doping to limit SCE. Current technology is near the limit due to mobility degradation in highly doped channels as well as I²R power dissipation due to excessive gate and S/D junction leakage. Clearly, new device designs that can perform with lower channel doping and reduced gate voltage are required. While fully depleted devices can be built on SOI wafers with a very thin silicon body, multiple gate MOSFET (MugFET) devices offer better scalability and layout efficiency [15]. In addition to improved mobility afforded by the use of an intrinsic channel, MugFET devices are expected to operate in full channel volume inversion due to enhanced gate control and quantum confinement effects, scenarios that could potentially increase both mobility and drive current [16].

1.2.1 MugFET Varieties

Multiple Gate Field Effect Transistors show great promise as an alternative to planar CMOS technologies below L₉=15nm as evidenced by endorsement from the International Technology Roadmap for Semiconductors (ITRS) [17]. Several designs depicted in Figure 6 have been proposed including planar, vertical, fin, tri-gate, and gate all around (GAA) that all make use of enhanced gate control due to the action of multiple electrodes surrounding the channel.
Figure 6: various MugFET structures [18]

The key operation differences and technological issues for each device type are summarized in Table 1 [19].

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<td></td>
<td></td>
<td>to substrate</td>
</tr>
<tr>
<td>vertical</td>
<td>_</td>
<td></td>
<td>to substrate</td>
</tr>
<tr>
<td>tri-gate</td>
<td></td>
<td></td>
<td>to substrate</td>
</tr>
<tr>
<td>GAA</td>
<td></td>
<td></td>
<td>or _</td>
</tr>
</tbody>
</table>

Table 1: operation characteristics and design considerations for various multiple gate devices
Multiple gate devices do not require any channel doping to reduce the depletion width (and subsequent decrease in $L_d$) as this parameter is defined primarily by the active volume. Moreover, the S/D junction depth is similarly defined by the silicon body thickness ($T_{Si}$) and shifts the onus from developing complicated Halo/LDD doping schemes to ensure uniform body-doping profiles with appropriate activation anneals to control diffusion near the gate edge. While the manufacturability of MugFETs remains challenging due to their 3D structure, most utilize self-aligned gate electrodes amenable to conventional planar CMOS process modules [20-22].

Of the varieties discussed above, the FinFET and tri-gate are reported to be the most manufacturable [23-24]. However, a 3D scaling paradigm that forms channel width perpendicular to the substrate requires building MugFETs as tall as possible (>50nm) to maximize the channel width per die area benefit. If tri-gate device height is increased accordingly, the body thickness to height ratio must migrate away from 1:1 toward ratios typically seen on FinFETs to maintain channel control. In this scenario, the top gate is no longer playing an important role and the device behaves as a dual gate (DG) FET [25]. Hence, the best channel control, manufacturability, scalability, and channel width per die area can be achieved with the FinFET structure.

1.2.2. Theoretical Scaling Limitations

In order to control short channel effects in aggressively scaled MOSFETs, the device engineer must ensure that the ratio of body thickness to gate length is sufficient to ensure both low off state leakage and full gate control over the channel. Intuitively, the silicon thickness requirement serves to eliminate any portion of the channel not directly
controlled by the gate electrode. It is easy to understand why multiple gate structures, which exhibit enhanced channel control, have a relaxed requirement for $T_{Si}/L_g$ [26-27]. A comparison of these fundamental ratios is shown for several MOSFET types in Figure 7.

![Diagram of MOSFET types with T_{Si}/L_g ratios](image)

Figure 7: theoretical body thickness to gate length ratios required to minimize SCE and SS degradation in various MOSFET structures with targeted $L_g=10$nm [adapted from 26-27]

The process advancements that permit $L_g$ reduction below 10nm are accompanied by competing device constraints that may hinder device performance. For very small gate lengths, a combination of band-to-band tunneling, quantum mechanical tunneling, and thermionic emission lead to dramatic increases in $I_{OFF}$ [28]. Body thickness can be further reduced to eliminate leakage paths and comply with ITRS leakage requirements for high performance devices, although increasing S/D resistance may severely degrade
device performance. Similarly, smeared S/D junction doping profiles limit the impact of DIBL but add an additional S/D resistance component that reduces on-state current.

1.2.3 Basic FinFET Process Flow

In order to familiarize the reader with the established methods of FinFET device fabrication and to illustrate the compatibility with current planar CMOS processing techniques, a simplified process flow is discussed in the following section. Excluding lithography required to integrate both pMOS and nMOS devices on the same wafer (CMOS) this flow utilizes four non-self aligned process modules including active, gate, contact, and metal level patterning. The spacer, implant and silicide process modules are all self aligned as in standard planar CMOS processing.

The starting material is a (100) surface oriented silicon on insulator (SOI) wafer. Active area patterning of the SOI material by reactive ion etching (RIE) results in fin structures with (100) top and (110) side surfaces sitting on top of the buried oxide (BOX) layer as shown in Figure 8.
Figure 8: top down view of a long channel MugFET after active level patterning

The fin sidewalls are somewhat roughened due to the RIE and are often exposed to surface treatments to reduce line edge roughness (LER). Following ash and wet clean of the patterned active area to remove residual photoresist, the gate stack deposition sequence is as follows:

1. ~2nm high-k deposition by atomic layer deposition (ALD)
2. high-k interface engineering
3. metal electrode deposition by ALD
4. poly-silicon cap deposited by rapid thermal processing (RTP)
5. gate stack planarization
6. BARC and photoresist

The second RIE step utilizes reticle alignment marks to ensure overlay accuracy of the gate level to active level patterns (see Figure 9).
Figure 9: top down view of a long channel MugFET after active and gate level patterning

Spacer formation on the gate is the first of the self-aligned process modules for transistor formation. Blanket deposition of insulating materials (typically Si$_3$N$_4$, SiO$_2$ or a combination) is followed by anisotropic dry etching to remove the spacer material everywhere but adjacent to the gate. The difficulty of removing spacer material from one vertical surface (fin) while leaving it intact on another (gate) should not be underestimated by the reader and will be addressed in subsequent sections. S/D implantation and activation follow spacer formation with additional lithography defined hard masks required for CMOS integration to form nFET and pFET transistors on the same wafer. Nickel salicide (self aligned silicided) completes the front end process sequence and enables preliminary device testing (see Figure 10).
Figure 10: top down view of a long channel MugFET after spacer formation, S/D implant, and salicide

The beginning of back end metallization begins with blanket deposition of the contact etch stop layer (CESL) and interlayer dielectric (ILD). These materials are lithographically patterned and the contact holes are formed by RIE. The contact liner is deposited into the vias by physical vapor deposition (PVD) followed by the tungsten plug. Planarization of the W plug back to the ILD surface prepares the contacts for wiring at the metal level (see Figure 11).
Industry standard AlCu alloy is then deposited over the wafer and lithographically patterned to finalize the test structure which stops at the first metallization level as compared to the 7-12 levels of metallization typically employed for the most advanced IC and system on chip (SOC) applications (see Figure 12).
1.3 Source-Drain Resistance

Even though multiple gate field effect transistors (MugFETs) escape some of the stringent geometric scaling requirements of their planar counterparts, they suffer large parasitic resistance owing to the extremely narrow source drain regions. Dixit et al. have conducted several simulations of MugFET device S/D resistance [29-31]. Their work attempts to modify the planar model for S/D parasitic resistance by taking into account 3D structure as shown in Figure 13.

![Figure 13: FinFET type structure used in simulations by Dixit et al. (a) top view, (b) cross section through A-A’, (c) cross section through B-B’ [29]]

The most severe shortcoming of this model is the block-type silicided portion of the device depicted as a dashed box in Figure 13. This geometry fails to capture the 3D nature of silicidation over a raised structure as observed for the silicon fins on BOX pedestals shown in Figure 14.
The structures shown in Figure 14 were fabricated by depositing differing amounts of PVD nickel over silicon fins, applying a 5 minute soak anneal at moderate temperature, removing un-reacted nickel using sulfuric acid + hydrogen peroxide (SPM), and finally applying a shorter final anneal at higher temperature. Clearly, the silicide profile is concave and resembles the expected PVD deposition profile over a raised surface. Because very little nickel (150Å case) is required to almost completely consume the fin body, it may be advantageous to decrease the amount of Ni used to form the silicide such that contact area between the silicide and HDD can be maximized (closer to 50Å case).

Irrespective of the 3D nature of the silicide front, the authors provide insight into the factors contributing to large S/D resistance in MugFETs. Specifically, they show that the contact resistance between silicided and doped fin dominates $R_{S/D}$ for FinFET type structures. This is due primarily to the reduced contact area through which current
traverses the junction between silicide and HDD. Figure 15 shows a FinFET structure with a narrow fin body (under the gate) and thicker fins in the S/D regions with the same block type silicide with two interfaces to the doped silicon portion of the fin depicted as planes A and B.

Figure 15: current density in A/cm² for linear operation (V_{gs}=1V, V_{ds}=0.05mV) through two silicide-HDD junctions in a FinFET type structure [29]

Figure 15 highlights the need to minimize direct contact between the silicide and fin extension (plane A) to prevent both current crowding and miniscule contact area that contribute to increased spreading (R_{SP}) and contact (R_{CO}) resistances respectively. This separation could conceivably be achieved with a controlled silicide depth on epitaxially thickened S/D regions. Finally, the authors suggest that decreasing spacer width and increasing fin extension doping somewhat mitigates R_{S/D} for this structure. It is important to note that this simulation exaggerates the series resistance problem by
modeling in the linear operation regime where the most severe current degradation occurs for high gate voltage and low S-D bias as shown in Equation 1 [adapted from reference 2].

\[
R_{ch}(linear) \equiv \frac{V_{ds}}{I_{ds}} = \frac{L}{\mu_{eff} C_{ox} W (V_{gs} - V_T - mV_{ds} / 2)}
\]

Where \( m \equiv 1 + \frac{3t_{ox}}{W_{dm}} \)

Equation 1: linear channel resistance; \( L = \) channel length, \( W = \) channel width, \( \mu_{eff} = \) effective mobility, \( m = \) MOSFET body effect coefficient, \( t_{ox} = \) oxide thickness, \( W_{dm} = \) maximum depletion layer width [adapted from 2]

This linear bias configuration results in low channel resistance (see denominator when \( V_{ds} \) is small) and hence \( R_{S/D} \) is a much larger proportion of total device resistance.

The conclusion that contact resistance dominates \( R_{S/D} \) especially for advanced transistor nodes is corroborated by M. Ozturk et al. who estimate its contribution to total device resistance at 25% for the 45nm node and climbing rapidly as shown in Figure 16 [32].
Figure 16: increasing contribution of contact resistance between silicide and HDD to total
device resistance as a function of technology node [32]

This finding implies that the best method of attacking the $R_{\text{S/D}}$ issue is to reduce the
contact resistance between silicide and HDD. The general expression for contact
resistivity between metal and heavily doped silicon is given in Equation 2.

$$\rho_c \propto \exp\left(\frac{4\pi\phi_B}{qh} \sqrt{\frac{m^*e_{Si}}{N_d}}\right)$$

Equation 2: dependence of contact resistivity between metal and heavily doped silicon on
barrier height and surface doping concentration [2]

The above relation indicates that the surface doping concentration of the HDD region and
the barrier offset between the silicide and doped silicon are the only controls that can be
used to decrease the contact resistivity. However, 3D device architecture may allow for
increasing the contact area through novel contact schemes and provide another means of
decreasing $R_{\text{CO}}$ independent of the contact resistivity. Conventional MOSFET devices
that utilize a mid-gap silicide (NiSi) on heavily doped silicon can aspire to reach $\rho_c \sim 10^{-7} \, \Omega/cm^2$ with further reduction limited by dopant solid solubility limits. This implies that pushing the required DG device contact resistivity below $10^{-8} \, \Omega/cm^2$ for 22nm node and beyond will necessitate either dual silicidation with lower barrier height for n+ and p+ HDDs or dramatically increasing the dopant concentration at the silicon surface.
### 1.3.1 Source Drain Resistance Components in FinFETs

A list of source drain resistance components starting from the contact via and migrating toward the channel is given in Table 2 to clarify further discussion.

<table>
<thead>
<tr>
<th>resistance component</th>
<th>symbol</th>
<th>dependence</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>contact resistance between via and silicide</td>
<td>$R_{\text{CON}}^\text{via to silicide}$</td>
<td>contact area, barrier height between liner and silicide</td>
<td>industry standards are Ti/TiN (W plug-Al backend) and Ta/TaN (Cu damascene)</td>
</tr>
<tr>
<td>sheet resistance of the silicide</td>
<td>$R_s^\text{silicide}$</td>
<td>silicide resistivity, thickness, and x-y dimensions</td>
<td>can be dominated by device layout (i.e. gate to drain distance) or 3D structure</td>
</tr>
<tr>
<td>spreading resistance due to transition between S/D pad and 3D silicide over fin</td>
<td>$R_{\text{SP}_{\text{sil}}}^\text{pad to fin}$</td>
<td>contact area and relative volume differences between pad silicide and fin silicide</td>
<td>only present for fin arrays with S/D pads</td>
</tr>
<tr>
<td>contact resistance between silicide and doped fin extension</td>
<td>$1R_{\text{CON}}^\text{silicide to HDD}$ or $2R_{\text{CON}}^\text{silicide to ext}$</td>
<td>contact area between silicide and silicon fin, barrier height between silicide and doped fin, surface dopant concentration</td>
<td>may be modulated at the interface via dopant or impurity pileup, can exist at multiple junctions (HDD or ext)</td>
</tr>
<tr>
<td>sheet resistance of the HDD fin</td>
<td>$R_s^\text{HHD fin}$</td>
<td>doping concentration, dopant activation efficiency, fin dimensions</td>
<td>dopant solid solubility limit conventional implant issue reduced with epitaxial S/D portion of fin</td>
</tr>
<tr>
<td>spreading resistance between HDD and fin extension under the spacer</td>
<td>$R_{\text{SP}_{\text{fin}}}^\text{HHD to ext}$</td>
<td>% cross section reduction from S/D to ext under the spacer, dopant concentration gradient</td>
<td>spread from un-silicided HDD to fin extension ≠ spread from epitaxially thickened HDD to fin extension</td>
</tr>
<tr>
<td>resistance of fin extension</td>
<td>$R_{\text{ext}}$</td>
<td>dopant concentration and activation</td>
<td>lateral diffusion profile post activation anneal determines gate overlap/underlap</td>
</tr>
</tbody>
</table>

Table 2: S/D parasitic resistance components for one side of a generic transistor
The components listed in Table 2 are visually depicted in Figures 17-19 for various FinFET structures used in this work.

Figure 17: S/D resistance components in FinFET transistors with conventional S/D pads

Figure 18: S/D resistance components in padless FinFET transistors with slot contacts
Figure 19: S/D resistance components in padless FinFET transistors with epitaxially thickened HDD and slot contacts

From the above figures, one can observe a reduction in the number of series resistance components by moving to a pad-less fin structure and again by the use of S/D epitaxy. The absolute magnitude of total $R_{S/D}$ reduction through elimination of certain components is not obvious from these images and will be addressed in later sections.

1.3.2 $R_{S/D}$ Reduction Techniques

The contact resistance between via and silicided S/D region is dominated by contact area and work function difference between the two metallic conductors. Contact scaling has been paramount to the increased performance seen over the past few transistor nodes and contact diameter continues to shrink so rapidly that they often land partially over shallow trench isolation (STI), rather than device active area, in small pitch structures like memory. Given that device dimensions must continue to shrink, reducing
the contact resistance by increasing the contact area is not an option. This situation leaves the device engineer with only one option: decrease the work function difference between the contact liner material and the silicide. For AlCu alloy metal backend with W plugs, a bi-layer Ti/TiN layer is typically employed to prevent W precursor intrusion into the interlayer dielectric (ILD), hinder W plug oxidation by oxygen diffused from the ILD, decrease contact resistance to the silicide, and improve W plug adhesion [33]. In this structure, carriers must traverse three interfaces: from W to TiN, from TiN to Ti, and from Ti to silicide. Comparative work function offsets for this set of materials is shown in Figure 20.

![Figure 20: work function for materials in the via structures used in this study, values were taken from [34-35]](image_url)

Although the differences in work function are small in this film stack, it is important to note that continued scaling of the liner thickness will alter the work function of the materials as observed by K. Choi et al. [35]. Their work highlighted a reduction of TiN...
work function when thickness was decreased below 100Å. The physics behind this phenomenon is not completely understood but from elementary solid state one can imagine a lower barrier for electrons to escape to the vacuum as the ‘surface volume'/total volume ratio in the film approaches unity. In any case, the thicknesses of the films employed in this work are slightly higher (2-4x) than the observed window for meaningful work function modulation (<100Å). Although the barrier offsets depicted for the film stack in Figure 20 are small, the contribution to total device resistance can potentially be reduced through the use of alternate materials. The W/TiN/Ti/NiSi film stack is almost exclusively utilized for the vias in this study but permutations of W plug liner materials and NiSi capping layers that lead to resistance changes and/or contact reliability are explored and detailed in subsequent sections.

The silicide sheet resistance is dominated by the parent material of choice for current salicide processing, NiSi. This material offers numerous advantages over its precursors TiSi2 and CoSi2 including: less silicon consumption that enables smaller junction depth, no line width dependence for sheet resistance (single phase), low temperature processing, and amenable mid-gap work function for both n and p-type silicon contacts [36]. Literature values reported for bulk NiSi resistivity annealed below ~ 450°C are less than 15 Ohm-cm, the lowest for silicides used to date in CMOS manufacturing [37]. Many researchers have modified the properties of NiSi via alloying or implantation in hopes of reducing the barrier height for carrier injection into the HDD regions of nMOS or pMOS transistors [38-43]. Most of these novel silicides exhibit a wider process window in terms of thermal budget compared to NiSi which begins to form
the high resistance NiSi$_2$ phase above 500°C. Electron barrier height modifications attempted by alloying NiSi with a low work function metal (i.e. Er or Yb) are plagued by rapid diffusion of the modifying metal away from the silicide-silicon junction thus rendering barrier height modification ineffective. Efforts to modify the hole barrier height with high work function materials (i.e. Pt, Ir, Pd) are generally successful as these species diffuse much slower than Ni but the increased thermal budget during silicidation and additional process complexity/contamination concerns required to safely etch the un-reacted portion of these materials somewhat undermines the utility of this approach. Finally, sheet resistance of novel silicides is comparable to NiSi but almost always larger with little or no data on line width resistivity dependence due to multiple phase formation or contact resistance to conventional W plug or Cu damascene liner materials. Several permutations of multilayer and implanted silicides are detailed in later sections.

The spacer width determines two important parameters for the geometry of the device: gate to drain (GtD) distance and Gate to S/D overlap/underlap. The gate to drain distance will ultimately dictate the length of silicided active material between the via and fin extension. As this distance increases, carriers are able to conduct through the silicide over a longer distance and drop less voltage through a metallic conductor before breaking across the silicide-active junction. Hence, reduced spacer width allows carrier transport in the S/D through a greater metallic conductor (silicide) path length. Minimal fin width reduces the effectiveness of LDD doping schemes for aggressively scaled MugFET devices and hence doping near the S/D edge is typically done after spacer formation. Because the spacer effectively shields the fin body from implant, the subsequent anneal
must drive diffusion of dopants up under the spacer toward the gate edge. The degree to which the dopant front falls short of or shoots past the gate edge determines the amount of gate underlap or overlap respectively. Overlapped structures are inherently problematic due to SCEs as discussed in section 1.1.1. For underlaped structures, there exists a benefit for SCE because \( L_g \sim L_{\text{eff}} \). In addition, the direct and inner fringe contributions to the overlap capacitance are nullified leaving only outer fringe capacitance between the gate electrode and underlaped active. The outer fringe capacitance is based on the proximity of gate and S/D electrodes as well as the intervening dielectric (in this case the spacer material) and hence is less disruptive to AC device performance compared to the inner fringe capacitance that depends upon the gate dielectric thickness and higher permittivity silicon channel. Therefore, reducing spacer width limits the volume of HDD that carriers must traverse to reach the channel at the same time reducing the thermal budget impact of the dopant activation anneal because controlled diffusion under a narrower spacer necessitates shorter time to form the more favorable underlaped transistor structure.

Thickening the HDD region of aggressively scaled pad-less FinFET structures provides two important benefits:

- Greater capture cross section for dopants \( \rightarrow \) lower HDD sheet resistance
- Larger contact area between silicide and doped silicon \( \rightarrow \) lower silicide contact resistance

It is crucial that the gate spacer material be cleared from the fin sidewalls to allow selective epitaxial growth over the whole of the fin body. Depending on the process
conditions (temperature, pressure, etc.) and starting surface (crystalline orientation, pre-
clean, surface termination) the epitaxial profile may be altered to increase the doping
efficiency and contact area.

As carriers traverse from the partially silicided HDD fin region into the silicon fin
under the spacer (fin extension), the silicided volume begins to taper off quickly. The
resulting current crowding at least partially motivates carriers to suffer a “premature”
voltage drop across the NiSi-silicon interface and begin to conduct through the more
resistive doped silicon. However, an epitaxially thickened S/D fin as in Figure 19 could
potentially prevent any silicide formation under the spacer and reduce the probability of a
metallic conductor protrusion through which current crowding might occur. If the
silicide thickness is less than the selective epitaxy thickness then no silicide should exist
in the fin extension. This requires all current to drop across a “large” NiSi-silicon contact
area and effectively eliminates any silicide spreading resistance contribution to $R_{S/D}$. It
should be noted that this process scheme increases the risk of bridging the gate to S/D
especially for thick epitaxy. Structures with and without silicon fin epitaxy have been
formed to evaluate the magnitude of silicide spreading resistance.

Current crowding from an epitaxially thickened HDD region to the narrower
extension is inevitable for process schemes that utilize such structures. The magnitude of
this contribution is unattainable without numerical simulation and even these results
would have to be based on process simulations to account for lateral doping profiles in
the fin as there are no characterization techniques available to verify dopant distribution
in nanoscale fin structures. Nonetheless, test structures simulating the transition between
HDD and fin extension are measured and evaluated in hopes of providing some insight and an empirically-based model.

1.4 Summary

The introductory sections highlight some of the major process integration, materials selection, and device design issues surrounding realization of FinFET transistors with critical dimensions appropriate for the 16nm technology node. Specifically, the silicon fin width, S/D doping methodology, silicide material properties, and contact scheme must be altered within the framework of conventional planar MOSFET processing to advocate the utilization of FinFET devices to achieve high performance transistors for IC applications during the second decade of the 21\textsuperscript{st} century.

Even the most aggressive 193nm lithography options including immersion and high numerical aperture lenses cannot directly pattern narrow/small pitch silicon fin structures to meet the body thickness requirements for aggressive MugFET scaling. Section 1.2.2 established the criterion of \( \frac{L_g}{T_{Si}} = 1 \) to ensure full channel volume inversion implying that 10nm fin width would be required to manufacture a SCE immune FinFET with \( L_g=10\text{nm} \). An alternative to photon based exposure of photoresist, electron beam lithography, is capable of patterning very small features but the wafer throughput, excessive cost, and commercial availability of these systems are critical manufacturing barriers that have seen little improvement over the past decade. For these reasons, a process sequence that makes use of standard 193nm lithography tools to reliably pattern small features is desirable. The first section of Chapter 3 establishes several viable
options to achieve $W_{\text{fin}} < 10\text{nm}$ while doubling channel width per device area using the sidewall transfer process.

To maintain the attractive area scaling benefits of FinFET devices, the layout of the device must migrate away from the pervasive “dog bone” structure toward pad-less fin structures to significantly reduce device area footprint as shown in Figure 21.

Figure 21: top down view of FinFET layout options

Interestingly, the use of a sidewall transfer process to reduce $W_{\text{fin}}$ is amenable to this change and actually motivates the transition to pad-less structures to bypass costly additional lithography steps. Once the large S/D areas are removed either by design or processing, the ramifications for S/D doping must be dealt with. Pad-less fin structures with very narrow fins possess insufficient dopant capture cross section even with high angle implants that are inapplicable to high aspect ratio tight pitch features. The most attractive and manufacturable option is to increase the fin width in the S/D regions to enable a high dose zero degree (normal to wafer surface) implant. This would provide excellent control over the S/D junction depth ($X_j$) and could potentially reduce or eliminate S/D series resistance components. Several process modules including spacer...
formation and epitaxial growth must be integrated to realize this type of structure and will be detailed in sections 2 and 3 of Chapter 3.

The largest S/D series resistance component is the contact resistance between the semi-metallic silicide and the heavily doped semiconducting portion of the silicon fin. I will demonstrate later that this component constitutes > 40% of total $R_{S/D}$. From a materials perspective, modifying the properties of the silicide-silicon interface is an attractive option to reduce this contact resistance. This can be achieved either through the use of novel silicides, NiSi alloys, or by altering the silicon dopant density. Chapter 4 highlights beneficial changes to silicide resistivity and contact resistance due to modification of either silicide (alloying, surface prep) or silicon (surface prep, impurity implantation).

Once the thin silicon fins have been thickened by epitaxy, implanted, and silicided the final barrier to device fabrication is forming electrical contact to the S/D. For single fin devices it may be possible to land a single contact over the freestanding fin but circuit designers will require modulation of channel width to achieve varying degrees of current drivability. This caveat motivates the need for small pitch fin arrays that cannot be contacted with an array of standard circular vias. To overcome this limitation, I demonstrate the use of slot contacts that land over the entire fin array. The issues associated developing a contact etch that successfully lands over a 3D surface in addition to material selection to reduce contact resistance between via and silicide are detailed in Section 3.4 and Section 4.2 respectively.
The above process module and materials alterations to the standard FinFET architecture enable aggressive scaling of device dimensions, improved device area efficiency, and reduction of S/D series resistance while maintaining close adherence to existing process, tool, and material selections currently employed for mass production of cutting edge transistors for IC applications.
2. MATERIAL AND STRUCTURE CHARACTERIZATION

2.1 Electron Microscopy

The three dimensional nature of the structures in this study requires heavy use of electron microscopy to determine the need for further process parameter variation. Electron micrographs used in this work yielded information including:

- Material identity (mass/etch contrast)
- Etch rate (change in dimension, etch selectivity)
- Process failure (structural collapse, over etch, under etch)
- Critical dimensions (fin width, spacer width, hard mask thickness, recessed layers, etc...)

These observations were used to establish material selection, thickness, deposition method, and etching parameters to achieve the desired device structure.

2.1.1 SEM

A Hitachi S4800 field emission SEM with 2.1nm resolution at 1kV was used to capture the majority of the SEM images used in this dissertation. This system has been employed for etch verification, thickness measurements, and feature measurements. The samples are typically prepared with a SELA MC600 micro-cleaving tool. A PECVD tool is available to cap specimens with TEOS prior to cleave to facilitate contrast etching with phosphoric acid, potassium hydroxide, buffered oxide etch (BOE), or dilute hydrofluoric
Acid (DHF). The focused ion beam tool can also provide an area specific platinum strap when necessary. Finally, all specimens are coated with a very thin (<1nm) iridium layer just prior to imaging to prevent specimen charging.

2.1.2 TEM

A FEI Tecnai F-30 TEM with 0.2nm resolution was utilized in specific cases where SEM resolution and contrast were insufficient to determine material identity or dimensions.

2.1.3 Error Analysis

The electron microscopy utilized for this study focused primarily on image feature size and material identification. The latter was typically achieved through the use of capping layers and decorative etches to highlight one material in a structure over another. These etch contrast techniques serve to maximize the signal intensity difference at the interface between two materials to enable a more reliable measure of a specific feature. In general, the uncertainty associated with measurements based on a digital image can be expressed as a partial differential equation with three variables as shown in Equation 3.

\[
\frac{df}{dx} \, dy + \frac{df}{dy} \, dx + \frac{df}{dz} \, dz = \frac{\partial^3 f}{\partial x \partial y \partial z}
\]  

Equation 3: partial differential equation for a function of three variables

The expression for feature size in a 1-D digital image is given in Equation 4.
\[ L = p_f \frac{l_s}{p_s} \]  

(4)

Where \( L \) = 1D feature length, \( p_f \) = # of pixels in feature 1-D measurement, \( l_s \) = length of standard bar, and \( p_s \) = # of pixels in length of standard bar

Equation 4: feature size in a 1-D digital image

Therefore, the uncertainty in the image size \( dL \) is given by Equation 5.

\[
dL = \left( \frac{\partial L}{\partial p_f} \right)_{l_s, p_s} dp_f + \left( \frac{\partial L}{\partial l_s} \right)_{p_f, p_s} dl_s + \left( \frac{\partial L}{\partial p_s} \right)_{p_f, l_s} dp_s
\]

\[ \Rightarrow dL = \frac{l_s}{p_s} dp_f + \frac{p_f}{p_s} dl_s - \frac{p_f l_s}{p_s^2} dp_s \]

Equation 5: uncertainty for length in a 1-D digital image feature

The quantity \( dp_f \) is typically determined by a human or a computer algorithm and attempts to discriminate between the edge of a feature and the adjacent matrix/layer/substrate/etc. by examining changes in pixel intensity over some range of adjacent pixels. The error associated with this determination is made twice when defining two edges. Humans can distinguish ~120 gray scales but are very limited when it comes to detecting gradual changes whereas computer algorithms attempt to model a specified \( \Delta I \) associated with an edge as a mathematical function. The human based measurements shown for images in this document were aided by filtering, digital contrast enhancement, and etch contrast enhancement to minimize the pixel variation associated with a feature. Regular calibration standards are used by the SEM technicians to minimize \( dl_s \) as part of their preventative maintenance schedule. Finally, \( dp_s \) presents a
much lower contribution to the measurement error compared to $dp_f$ because the length standard utilizes sharp features displayed against a background such that contrast is maximized. In conclusion, the majority of digital image feature measurement uncertainty comes from human determination of both edges though contrast enhancement and multiple measurements can reduce the overall measurement uncertainty to a value less than the resolution of the instrument (~1nm).
2.2 Materials Analysis

2.2.1 Secondary Ion Mass Spectrometry

The SIMS profiles were acquired using a Physical Electronics ADEPT-1010 unit with a 500eV Cs\(^+\) beam at 60\(^\circ\) incidence. To avoid measurement artifacts associated with knock-on effects, the analysis was done from the wafer backside after thinning and polishing to ~150 nm silicon thickness. This technique was chosen to identify the impurity distribution in implanted silicon post silicidation. It provides a large area for analysis compared to STEM-EDXS, offers much simpler sample preparation, and much higher sensitivity. The basic premise of operation is as follows:

- **Source:** secondary ions sputtered from the sample surface
- **Detector:** a quadrupole mass analyzer utilizes electric fields to steer ions with a specific mass to charge ratio into an avalanching ion detector that multiplies the number of secondary electrons generated per incident ion; the electric fields are modulated in time to collect a range of pertinent m/q ratio ions
- **Signal:** a Faraday cup collects the secondary electrons at the last stage of the avalanching ion detector and records a relative intensity for each m/q ratio; these relative intensities are recorded in time as the material is sputtered away to yield a composition vs. depth profile

2.2.2 Grazing Incidence X-Ray Diffraction

The GIXRD scans were acquired using a Bede-D1 diffractometer. A parabolic graded multi-layer mirror is used just after the sealed Cu source to collimate the beam.
and filter all wavelengths except Cu Kα1. A 0.5 mm incident beam slit was used in conjunction with Soller slits at the detector. The incident beam angle, ω, was varied from 0.5 to 2 degrees as the 2θ scan covered from 10 to 90 degrees. The instrument setup is shown in Figure 22.

![Figure 22: GIXRD stage configuration](image)

This technique was selected to identify NiSi phases and d-spacing changes associated with prior impurity implantation of the silicon wafer. The basic premise of operation is as follows:

- **Source:** diffracted monochromatic x-rays from a crystalline material
- **Detector:** typically a lithium drifted silicon detector comprised of sandwiched p-type-intrinsic-n-type layers protected by an x-ray transparent window (Be); the diffracted x-rays penetrate the p-i-n structure and create electron hole pairs (ehps) which are immediately swept out of the semiconducting layers to signal processing electronics
• Signal: Since the energy of the x-rays from a particular anode (Cu, Mo, etc) is well known, the voltage is converted into a number of incident x-rays and is plotted against the changes in diffraction angles altered by the goniometer.

2.3 Electrical Test

2.3.1 Equipment

Electrical data was acquired using a 200mm wafer auto prober manufactured by TEL Corporation. The unit utilizes an optical stage and adaptable learning algorithm to align and probe the devices on the wafer surface. The probe card is comprised of a 2x12 array of CuBe tip needle probes ~15um in diameter. The software program Metrics ICS was employed to program the test sequence and parameters. The required spatial information from the user includes, wafer size, die size, and module location. The next level of hierarchy determines the device under test (DUT) within a module by assigning active pins through a Keithley switch matrix. Finally, the test algorithm assigns specific functions (force/sense) to the connected pins and regulates the format of data output.

2.3.2 Kelvin Contact Resistance

Determining the contact resistance between two materials requires a known potential difference across the junction, current passing through the junction, and some diversity of area for the contact to rule out size dependent effects. The test sequence is as follows: material A is held at voltage $V_A$ while material B is grounded. A current is forced between materials A and B. The potential difference is divided by the current to give resistance across the junction [44]. Finally, the polarity of the potential difference is
reversed such that current flows in the opposite direction (to check for any type of rectification behavior…not expected for metallic junctions). This test sequence is repeated for contacts of various sizes. The test structure utilized in this study is depicted below in Figure 23.

\[
R_C = \frac{V_{34}}{I_{12}} \]
\[
\rho_C = \frac{R_C}{A_C}
\]

Figure 23: cross section schematic (left) and top down view (right) for a Kelvin contact resistance structure

The single contact size ranges from 350nm down to 200nm in diameter for the devices in this test module whereas the contact array on terminals V4 and I4 are a constant 350nm in diameter.

2.3.3 Van der Pauw Sheet Resistance

Sheet resistance of a contiguous layer is determined by the Van der Pauw technique [44]. If the precise dimensions including the thickness are known then the resistivity of the material can be computed. This technique can be applied to films of any shape (clover, bar, circle, etc provided that probe placement is accurate and
complementary measurements are taken to account for non-symmetric films. The test sequence for the test structure shown in Figure 24 occurs in the following manner:

Current is sourced from probe A and collected in probe B. The other two probes, C and D are biased such that all current is collected at probe B. Because probes C and D have differing physical proximity to probe A (ratio of $\sqrt{2}$ for a square film), they will not require the same bias to ensure all current is collected at probe B. The potential difference between probes C and D is directly related to the difficulty of altering field lines in the film being measured, a property inversely proportional to the resistivity of the film. Hence, for a small potential difference we see a low sheet resistance.

This methodology is well documented and was utilized to allow the use of 4 SMUs rather than 2 SMUs + Voltmeter (an option not available on the parameter analyzer used) [45]. The Van der Pauw test structure utilized in this study is depicted below in Figure 24.

![Figure 24](image)

Figure 24: top down view of the sheet resistance test module used in this study
2.3.4 Silicide Block Kelvin Structures

Fin arrays covered partially covered with nitride were fabricated to artificially create a junction between NiSi and doped silicon. These structures essentially resemble ohmic contacts on either side of a resistor. Because the silicide makes contact to heavily doped silicon, there is no Schottky type barrier and hence no means of addressing the barrier height for carrier injection. However, these structures provide a simple means of determining the area dependence of contact resistance between silicide and doped silicon. The structures were formed and silicided with various nickel thicknesses. This should create differing interfacial area between NiSi and silicon without affecting the barrier height. The test sequence consisted of a 4 point Kelvin I-V sweep (source current, measure voltage) for fins with and without the silicide block as depicted in Figure 25.

![Figure 25: line resistance structures with (left) and without (right) a lithographically defined silicide blocking layer](image)

2.3.5 Planar Diodes

While there is not currently a test structure available for measuring the barrier height between a silicided and un-silicided fin structure, we have investigated carrier
injection for planar diodes. While these structures do not address any line width resistivity dependence or quantum mechanical confinement effects that could perturb $\Delta \phi_b$, they are easily fabricated and consist of a heavily doped and silicided region in direct contact with low doped silicon. Aluminum deposition on the backside of the wafer is used to ensure proper electrical contact to the low doped silicon. The test sequence consists of an I-V sweep that yields forward and reverse rectification characteristics over a range of temperatures [44].

2.3.6 Error Analysis

For all electrical measurements conducted in this work, up to four high resolution source monitor units (SMUs) were connected to an Agilent 5270B parameter analyzer with triaxial Kelvin cables of the same length to minimize leakage and line resistance variations. The voltage and current measurement resolution of the SMUs is $2\mu$V and 1fA respectively. In general, the measured voltages and currents for the test structures used in this study were 2-4 and 4-7 orders of magnitude above the resolution limit. All instruments including the parameter analyzer, switch matrix and auto prober station were tied to both chassis and earth ground. Direct current voltage measurement compensation was applied by the current reversal method where resistance measurements are taken at both forward and reverse bias conditions. This technique has the advantage over conventional current offset in that the white noise is reduced and stray electromotive force voltage is eliminated [70]. Wherever possible, both forward and reverse resistance calculations are included in a cumulative distribution plot to present all data points. In cases where the data was averaged, standard deviation bars are included.
3. FINFET PROCESS MODULE DEVELOPMENT

3.1 Sidewall Transfer Fins

Formation of narrow fins to enable aggressive scaling of $L_g$ for DG transistors has been widely reported. Efforts to utilize immersion lithography [47], e-beam lithography [48], and hard mask (HM) trim [49] have resulted in $W_{\text{fin}}$ as low as 10nm. However, these techniques require either costly lithography tools or suffer from process induced variation in $W_{\text{fin}}$ that can increase LER and degrade device control. Sidewall transfer or spacer transfer processes provide a means to shrink the active area CD and increase channel width per die area while bypassing costly e-beam or immersion lithography [50-54]. While impressive $W_{\text{fin}}$ via SWT (approaching 10nm) has been demonstrated for specific device layout applications, no studies covering a global integration perspective or process variability exists to date. The following section attempts to fill these needs by addressing three unique spacer transfer techniques and the process variability associated with each.

Three different approaches to achieve very thin fins via sidewall transfer (SWT) have iterated the use of silicon, silicon nitride, and silicon dioxide as shown in Table 3.

<table>
<thead>
<tr>
<th>SWT component</th>
<th>silicon</th>
<th>silicon nitride</th>
<th>silicon dioxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hard mask</td>
<td>N</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>dummy fin</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>sidewall spacer</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
</tbody>
</table>

Table 3: material options for SWT schemes
The main caveat that limits the number of potential schemes in this matrix is the use of silicon nitride as the fin HM, a choice that facilitates robust active level patterning in our facility.

3.1.1 TEOS Spacer Transfer

The process flow for SWT scheme #1 is shown in Figure 26.

A thickened nitride HM is deposited over the SOI and then capped with an amorphous silicon dummy active layer. Conventional 193nm alternating phase shift lithography is used to pattern the dummy active layer followed by RIE etch, ash, and wet clean. Next the dummy fin structures on silicon nitride are blanketed with tetraethoxysilane (TEOS) and a spacer is formed by directional RIE using a process that stops on the underlying silicon nitride layer as seen in Figure 27.
While the spacer profile is both thin and vertical, there is a significant loss (~16nm) of the silicon nitride HM during spacer etch. The subsequent dry etch removal of the amorphous silicon dummy fin utilizes CHF$_3$ that does not afford high selectivity to Si$_3$N$_4$. Further, because both materials are susceptible to F$^-$ based etching, tailoring the ratio of carbon to fluorine in the etch gas does not increase the selectivity. This scenario can lead to spacer collapse or delamination if its anchor to the silicon nitride HM is compromised by material erosion and undercut at the foot of the spacer as seen in Figure 28.
Figure 28: spacer collapse (left) and delamination (right) events after dummy fin removal due to recess of the silicon nitride during overaggressive TEOS spacer etch.

In the case of spacer collapse, it is expected that the non-vertical spacer profile (especially at the base of the dummy fin as seen in Figure 27) is to blame. After dummy fin removal, the residual stress in the TEOS film further increases the inward tilt. When combined with insufficient contact area to the nitride HM and physical bombardment of etch species during subsequent processing, the spacers are forced further toward one another and eventually break free of the underlying silicon nitride HM layer. This failure mode effectively blocks subsequent etch processing due to polymer buildup on the collapsed TEOS as seen in Figure 28 (left). Even if the dummy fin and spacer profiles are perfectly vertical, over etching the underlying silicon nitride HM during TEOS spacer formation can still undermine the cohesive force between the TEOS and silicon nitride layers. In this scenario the spacers are less likely to collapse inward but can succumb to their residual stress and delaminate as the contact area to silicon nitride is diminished as seen in Figure 28 (right). This raises serious concerns about the survivability of high aspect ratio spacers during the dummy fin removal. Once the dummy fin over etch time
was optimized to yield vertical sidewalls, increased spacer etch times were correlated with reduced final fin dimensions as shown in Figure 29.

Figure 29: effect of extending TEOS spacer etch time on final isolated (2 fin) vs. nested (20 fin) structures at both center and edge sites

The disparity between center and edge site fin width is attributed to a more aggressive etch near the center of the wafer (center fast etch) that results in thicker spacers on edge sites. Optimization of the bias conditions can help to alleviate this issue but it is a particular challenge when using SOI wafers. For a bulk silicon wafer, the source voltage is applied to the wafer chuck and accelerates the etch ions perpendicular to the wafer
surface due to uniform field lines. When the backside of an SOI wafer is biased in the same fashion, the field lines appreciably bend near the wafer edge as they traverse the BOX layer and reduce the velocity component of the etch species perpendicular to the wafer surface. This has the effect of decreasing the physical etch component near the wafer edge. An additional difference highlighted in Figure 29 is the increased thickness of nested vs. isolated fins. The reason for the thicker isolated fins is rooted in lithographic patterning of photoresist through chrome plated glass. During exposure, a significant amount of light is diffracted and/or scattered from the edge of the chrome line that is supposed to protect the underlying photoresist. For a nested structure (array of multiple fins), diffraction from adjacent chrome lines has the effect of increasing the photoresist exposure and thus reduces the ultimate feature size. For the isolated structure (any fin adjacent to a large un-patterned area or “field”), there is no chrome line on one side to provide the additional exposure and so isolated features tend to have larger CD. In any case, one can observe a tradeoff between final fin width and survivability as the etch time is increased for the same blanket TEOS deposition thickness and method. A prolonged TEOS spacer etch reduces both the spacer height and width. Therefore, a longer etch time trims the spacer width and ultimately results in a thinner SOI fin dimension. A simultaneous reduction of the spacer height helps reduce the aspect ratio and mitigates issues with spacer collapse. Unfortunately, a very short (<200Å) freestanding TEOS spacer does not effectively shield the silicon nitride HM during spacer transfer as most of this material is fully consumed during patterning of the silicon nitride. These combined observations indicate that maintaining a viable spacer height to
width (H/W) ratio (less than 3 to avoid spacer delamination) required the use of thicker spacer material (for sufficient spacer height to enable spacer transfer) and limited etch time to minimize silicon nitride undercut (to avoid spacer collapse) as indicated in Figure 30.

Figure 30: spacers formed from thicker TEOS showed a H/W ratio more amenable to higher SWT fin yield

Alleviating the issue of silicon nitride HM over etch during TEOS spacer formation required lowering the etch power, switching from timed to endpoint control over etch duration, and employing alternative etch gasses to enhance the selectivity of TEOS to silicon nitride. Lowering the etch power by more than 30% significantly reduced the physical etch component that was causing silicon nitride HM recess. This power reduction also decreased the TEOS etch rate thus increasing the amount of time required to clear TEOS from all surfaces parallel to the wafer surface leaving behind only the
vertical spacer. This increased time actually provided the additional benefit of enabling endpoint detection to control the duration of the spacer etch. Optical emission spectroscopy of the etch byproducts was continuously monitored at a wavelength of $\lambda=3865\text{Å}$, an emission line associated with the cyanide ion $\text{CN}^-$. As the TEOS is cleared and silicon nitride is exposed, the appearance of this species reaches a certain threshold (as determined by the second derivative of the intensity vs. time curve) that determines whether endpoint has been reached. For the initial work at higher power, this endpoint technique was not available because the detector dead time exceeded the total etch duration. The effectiveness of this endpoint scheme was verified by fixed wavelength reflectance spectroscopy over 9 sites across the wafer indicating TEOS spacer etch completion. Finally, because the silicon nitride HM is still susceptible to chemical etch even at lower power, I changed the etch species to a mixture of $\text{C}_4\text{F}_8 + \text{CO}$ etch gasses which inhibits nitride etch and provides better selectivity [55]. Following this optimized spacer formation process, the next dry etch is used to remove the dummy fin leaving behind freestanding TEOS spacers on silicon nitride.

A similar issue with material erosion due to the physical etch of the underlying nitride during dummy fin removal can be seen in Figure 31.
This problem was resolved by lowering the bias power (accelerates etch species) and increasing the source power (determines plasma density) to render the silicon etch more isotropic. The freestanding TEOS spacer is then used as a hard mask for RIE of the underlying silicon nitride layer. The result is shown in Figure 32.
The transfer of the TEOS spacer pattern into the underlying silicon nitride HM used for SOI fin definition tends to produce a lot of polymer residue inside the silicon nitride HM “doublets” due to the inefficiency of silicon etch and mass loading effects that result in re-deposition of etch byproducts on the walls of close pitch features. Figure 32 shows a greater amount of polymer deposition on the inner surfaces indicating that the difference in pitch of ~30nm is significant enough to locally alter mass loading effects. The subsequent clearing or breakthrough etch (Cl-based) removes this polymer buildup and eliminates the need for a conventional ash and wet clean sequence prior to SOI fin definition. In the final dry etch sequence, the silicon nitride HM is used to define the SOI fins which results in a doubling of the device width in the same die area footprint without double exposure or additional masks. This integration scheme has proven the most effective thus far in reducing the overall fin width while maintaining excellent line width roughness (LWR). There appears to be minimal impact on final fin dimension based on
the choice of low pressure chemical vapor deposited (LPCVD) or plasma enhanced chemical vapor deposited (PECVD) TEOS; a phenomenon attributed to comparable dry etch rate. This optimized scheme has produced high aspect ratio fins with an average width less than 10nm as shown in Figure 33.

Figure 33: top down (left) and cross section (right) SEM images of ultra narrow fins using TEOS spacer based SWT

Full wafer critical dimension (CD), line edge roughness, line width roughness, and sidewall angle mapping is not possible using conventional algorithms in a CD-SEM tool. Typically, the derivative of the intensity profile (or how fast contrast is changing) is measured across a known feature and modeled on either side of the feature as a Gaussian. All the typical function parameters (FWHM, skew, etc) are then extracted and used to generate the aforementioned statistical parameters. Because these features are so small
compared to the resolution of the top-down CD-SEM, the algorithm cannot distinguish Gaussian profiles for intensity change at both edges of the fin. The single Gaussian that is modeled is used to determine Fin Width (~FWHM) but even this statistic is flawed because of the residual hard mask on top of the fins that give a Q-tip type profile as seen in Figure 33.

3.1.2 Amorphous silicon Spacer Transfer

The 2\textsuperscript{nd} SWT process flow is depicted in Figure 34.

A thickened nitride HM is deposited over the SOI and then capped with a TEOS layer to form an oxide dummy active layer. Conventional 193nm alternating phase shift lithography is used to pattern the oxide followed by RIE etch, ash, and wet clean. The resist available for active level patterning has a low selectivity to oxide and therefore must be thickened to prevent loss of the resist line during RIE. Unfortunately, thicker
resist leads to larger line width for the same exposure conditions (not as much of an issue for SWT) in addition to resist pattern collapse for nested features such as fin arrays. One final issue with the oxide fin definition is an appreciable LER and sidewall angle that prevents formation of very thin contiguous spacers as shown in Figure 35.

![Figure 35: TEOS fins patterned by conventional CₓFᵧ dry etch show poor LER and sidewall angle](image)

The poor sidewall angle is due to the low power and insufficient over etch of the dummy oxide fin. Lower power is required to preserve the photoresist during fin patterning which has limited selectivity to oxide whereas the lack of over etch is required to preserve the thickness of the underlying silicon nitride layer. Tweaking these two parameters may improve the oxide fin profile but surely has a narrow process window and was not further explored in this work. The use of a metallic hard mask rather than photoresist to pattern the TEOS fins may be an attractive alternative because the HM can be removed selectively by wet etch without harming the oxide fins or the underlying silicon nitride layer. One potential issue with this approach is formation of a metallic oxide that would inhibit dry etch of the metal HM and complicate dummy TEOS fin
removal. Dummy fin structures on silicon nitride were blanketed with amorphous silicon and a spacer was formed by directional RIE of silicon. The selectivity to nitride is compromised when etching silicon with halogen (F⁻, Cl⁻) based species exacerbating the recess of the underlying nitride HM. However, the spacer structure is also much more robust exhibiting faceted edges that may contribute to its survivability. After spacer formation, the dummy fin was removed by vapor HF etch as seen in Figure 36.

Figure 36: faceted AmSi spacers after vapor HF removal of the dummy TEOS fin.

Figure 36 shows that the recess of the silicon nitride HM has increased by ~20% compared to SWT scheme #1 and that both spacer footprint and shape have been altered by the material permutation. The blurred contrast inside the dummy fin “hole” verifies the aforementioned LER issues associated with patterning of oxide structures and the trapezoidal shape that can contribute to inward spacer collapse is also evident and may be enhanced as residual stress in the polysilicon tries to “close the gap”. Nonetheless, this process scheme has shown excellent wafer uniformity in addition to a contiguous HM on even the shortest Lg modules for variety of AmSi spacer thicknesses as shown in Figure 37.
Figure 37: top down SEM images of both long and short (insets) channel SWT fins show comparable HM width for a variety of spacer thicknesses. This observation is attributed to the “hardiness” of the AmSi spacer compared to a TEOS spacer. The apparent consistency of HM thickness and survivability for different AmSi thicknesses stems from the increased spacer “shadow”. Because the silicon nitride area underneath the sloping spacer has increased there is very little chance of completely losing it during SOI patterning. Fins patterned using the most aggressive AmSi spacer thickness of 300Å are shown in Figure 38.
While this scheme shows excellent repeatability and within wafer (WIW) uniformity, there are several process optimizations that still remain before very thin fins (<10nm) can be formed including:

- Eliminate rough, tapered oxide fin sidewall (potential solutions: increased power/over etch or use HM instead of resist to pattern TEOS fins)
- Additional scaling of the spacer material (potential solution: use CVD polysilicon for thinner films)
- Improving the etch selectivity between silicon and silicon nitride (potential solution: use of an inhibitor/oxidant like O$_2$ or CO combined with etch species that attack SiO$_2$)

It should be noted that reduction of the AmSi spacer could be achieved by a very short thermal oxidation followed by HF based removal of the oxidized portion. This process tweak could be incorporated before or after the removal of the dummy TEOS fin.
3.1.3 Sidewall Oxidation and Transfer

The final SWT integration process flow is shown in Figure 39.

Figure 39: sidewall oxidation and transfer process sequence

The initial structure formation mirrors that of SWT scheme #1 but uses thinner amorphous silicon and adds an additional silicon nitride layer atop the dummy active layer. After conventional 193nm alternating phase shift lithography is used to pattern the dummy fins, they are exposed to furnace oxidation using the in-situ steam generation (ISSG) process developed by Applied Materials (AMAT) [56]. The top and bottom nitride layers prevent oxidation except at the sidewalls of the dummy fin. A calibration plot of oxidation thickness versus time for ISSG oxidation at 1050°C is shown in Figure 40.
Figure 40: ISSG calibration curves for the process used in SWT scheme #3

The initial recipe targeted a nominal oxidation of 150Å and resulted in an actual oxidation thickness of ~120Å as seen in Figure 41.

Figure 41: cross section SEM image of oxidized fins capped with platinum and etched in BOE for contrast

The lower than expected oxidation thickness is surprising because the silicon material is amorphous. With the added grain boundary volume compared to crystalline silicon on
which the recipe was developed, we would expect a much more rapid oxidation. There are several competing materials changes that may account for this observation that are discussed below.

The amorphous silicon dummy fin layer was deposited by thermal decomposition of \( \text{Si}_x\text{H}_y \) at 530°C in a horizontal tube furnace. It is expected that the film is fully amorphous and has no measurable grain size when deposited at this temperature [57]. Amorphous silicon is known to harbor a large population of point defects and point defect clusters [58]. Many of these point defects take the form of silicon interstitials whose population is increased with increasing oxidation rate [59]. The large number of silicon interstitial defect sites in AmSi enable a greater density of high oxidation states (a silicon atom bonded to 3 or 4 oxygen atoms) upon exposure to an oxygen ambient compared to crystalline silicon surfaces [60]. The formation of these high oxidation states has been identified as a prerequisite to the formation of silicon dioxide on bulk silicon [59-60]. It is well known that the volume expansion of \( \text{SiO}_2 \) results in residual oxide stress depending upon the oxidation temperature [61]. This stressed oxide tends to reduce \( \text{O}_2 \) diffusivity and is responsible for the parabolic nature of Deal-Grove oxidation rate as the oxide film thickness increases. Residual stress of oxidized AmSi and c-Si have been evaluated and indicate that the \( \text{SiO}_2 \) formed on AmSi exhibits much lower stress states [62]. The above observations all seem to imply that oxidation of an amorphous silicon film should proceed faster than of a crystalline silicon film because:

- chemisorption of \( \text{O}_2 \) is enhanced by the larger defect density of AmSi
- low stress oxides formed on AmSi permit faster diffusion of \( O_2 \) to the oxide-silicon interface

Closer examination of the concurrent oxidation and re-crystallization events within the amorphous dummy fin during the high temperature ISSG process, especially in the presence of hydrogen, can help elucidate the observed thickness limitation for oxide formation during SWT scheme #3.

Hydrogenated AmSi films exposed to a “wet” (H\(_2\) or H\(_2\)O vapor added to O\(_2\) ambient) have shown retarded oxidation and grain growth due to hydrogen passivation of dangling bonds associated with silicon defect states especially at grain boundaries [58-60]. Put simply, hydrogen can rapidly diffuse to dangling silicon bonds and terminate the site of potential Si-Si or Si-O bond formation and may also play a role in intercepting oxygen diffusing toward the oxide-silicon interface as indicated by the relative bond energies shown in Figure 42.

![Figure 42: proposed mechanism for hydrogen inhibition of grain growth and oxidation in hydrogenated amorphous silicon](image)

Figure 42: proposed mechanism for hydrogen inhibition of grain growth and oxidation in hydrogenated amorphous silicon
The inclusion of hydrogen during the oxidation of amorphous silicon also limits ability of the growing oxide or silicon to relieve stress especially for thinner films, an effect also seen for crystalline silicon oxidized in dry vs. wet ambient [57, 62]. Studies have shown that modest temperatures ~350°C or higher initiate H\textsubscript{2} out gassing from AmSi films implying that during the ISSG process, a continuous source of hydrogen is supplied to the oxide interface due to out gassing from the dummy fin structure [62-63]. If this is the case, an O\textsubscript{2} sticking coefficient one order of magnitude lower than that observed on c-Si is expected [62]. Also, any portion of the dummy fin structure that becomes depleted of hydrogen during the ISSG process results in limited O\textsubscript{2} penetration [62]. The above observations provide the building blocks for a kinetic and thermodynamic model that explains the limited oxidized volume observed for freestanding dummy fin structures used in SWT process #3. The specifics of the model are detailed below and graphically represented in Figure 43:

- The initial dummy fin consists of completely amorphous hydrogenated silicon due to the thermal decomposition of a Si\textsubscript{x}H\textsubscript{y} precursor at low temperature (530°C)
- O\textsubscript{2} chemisorption is limited due to hydrogen passivation of dangling silicon bonds and prohibits formation of high oxidation states necessary to form SiO\textsubscript{2}
- Out gassing from the dummy fin continually supplies H\textsubscript{2} near the oxide-silicon interface limiting stress relief that slows O\textsubscript{2} diffusion through the very thin growing oxide
Once the dummy fin is fully depleted of H₂ during the high temperature ISSG process, O₂ diffusion into the densifying silicon is limited further.

This scheme circumvents the need for scaled spacer deposition and etching by selectively oxidizing the fin sidewalls to form a thermal oxide HM and produces fins (in pairs) with a pitch much closer to industry expectations than the other two schemes. Moreover, the pitch of the initial dummy layer can be aggressively scaled without worrying about conformal deposition and etch of a spacer material. Subsequent dummy fin removal erodes most if not all of the silicon nitride HM yet the robust nature of the thermal oxide prevents spacer collapse. Final transfer to the SOI has resulted in thin fins of ~14nm average width (see Figure 44) with good center to edge wafer uniformity attributed to the ISSG process.

Figure 43: proposed model for ISSG oxidation of a hydrogenated amorphous silicon fin structure
Figure 44: sidewall oxidation and transfer fins with tapered profile and aggressive pitch

Unfortunately, there appears to be a narrow process window for the survivability of these SWT fins. The experimental matrix has utilized 100, 125, and 150Å nominal ISSG recipes. The shortest duration (100Å) did not produce a sufficient oxide HM for fin transfer while the remaining splits showed no appreciable difference as indicated in Figure 45.
It is interesting to note the loss of HM over the most curved portion of the fin structures (see Figure 45) and may be attributed to the action of the breakthrough step during final SOI fin definition or enhanced residual stress in the ISSG oxide over the curved portion of the fin.

3.1.4 Sidewall Transfer Summary

Evaluation of three unique approaches to reduce fin width while doubling channel per unit device area has been conducted. The first SWT scheme was optimized by
tailoring the spacer H/W ratio and silicon nitride to oxide dry etch selectivity to ensure a robust freestanding spacer. A final fin width <10nm was ultimately achieved by scaling the blanket TEOS deposition thickness within the constraints of maintaining viable spacers. Further reduction of the fin width may be possible through blanket TEOS thickness reduction and/or over etch but preliminary investigations indicate that these techniques will result in decreased fin yield. The second SWT scheme was plagued from the outset due to problems with patterning oxide fin structures with low LER and vertical sidewalls. The techniques typically utilized to achieve these parameters on silicon fins were unavailable due to the poor selectivity between the photoresist and the furnace oxide being patterned. This issue may be overcome through the use of a hard mask to pattern the oxide fins but may complicate the attractive vapor HF removal of the dummy fin due to HM residue. Nonetheless, SWT fins were reliably fabricated using this methodology (albeit of larger than desired W_fim) and reduction of spacer dimensions without aggressive dry etch are possible with this scheme to further reduce final fin dimension. Finally, SWT scheme #3 yielded narrow fins (W_fim~15nm) at a very tight pitch (<40nm) by forming an oxide on dummy silicon fins to serve the same function as a spacer for patterning SOI fins. The oxidation process showed a remarkable reduction in the expected oxidation rate that appears to be self limiting at least for the nanoscale features and processing times used in this study. This unexpected behavior is attributed to the role of hydrogen during the simultaneous oxidation and crystallization processes that occur during a rapid thermal cycle.
In conclusion, SWT scheme #1 has yielded the thinnest fins, will satisfy T_{Si} requirements for the 16nm node, and has been incorporated into additional structures used in subsequent sections. Table 4 incorporates a summary of the findings for the various SWT schemes investigated in this work.

<table>
<thead>
<tr>
<th>SWT scheme</th>
<th>#of dry etch processes</th>
<th>benefits</th>
<th>issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1: TEOS spacer</td>
<td>5</td>
<td>endpoint detection available and good selectivity to silicon nitride during spacer formation makes freestanding spacers very robust</td>
<td>scalability of conformal TEOS spacer thickness is limited</td>
</tr>
<tr>
<td>#2: AmSi spacer</td>
<td>4</td>
<td>simplified and more scalable dummy fin removal process, non-RIE spacer width reduction technique available</td>
<td>requires significant silicon dioxide fin etch development</td>
</tr>
<tr>
<td>#3: silicon dioxide sidewall spacer</td>
<td>4</td>
<td>very small pitch between individual SWT fins and fin doublets, possible self limiting oxidation step could allow for significant process variation</td>
<td>limited control over very thin oxidized sidewall width for amorphous silicon dummy layer</td>
</tr>
</tbody>
</table>

Table 4: summary of findings for three SWT schemes explored in this study
3.2 Multi-layer Spacer

FinFETs present a particular challenge during dry etch processing due to the vertical nature of the fin sidewalls. In our baseline flow, a relatively thick gate hard mask is required to allow an aggressive over etch of the gate metal at elevated temperature to clear it from the fin sidewalls. Without this aggressive etch sequence, metallic spacers would remain on the fin sidewalls and short the source and drain electrodes destroying device functionality. The thick gate HM must be cleared prior to silicidation for proper gate contact and is currently removed by a prolonged spacer etch. Unfortunately, the data presented below indicates that although the spacer etch opens the contact pads for both active and gate level, spacer residue persists on the fin sidewalls despite a significant over etch that also leads to recess into the BOX region at the gate edge. The ramifications of this un-optimized process include:

1) limited silicon surface on the fin for silicidation which impacts \( R_{CO} \) between NiSi and the fin extension

2) limited silicon surface on the fin for epitaxial growth which limits attempts to reduce S/D series resistance or alternative contact schemes on pad less fins

3) increased parasitic capacitance

4) difficulty clearing resist and BARC residue from the trenched out BOX near the gate edge after implant litho operations
3.2.1 Single Layer Spacer

The simplest FinFET spacer process forms an all silicon nitride spacer using anisotropic dry etching on ~50nm blanket silicon nitride. This scheme makes use of the height difference between the gate and fin (~3:2) to leave a smaller spacer on the fins compared to the gate. Top down SEM images are shown in Figure 46 for devices just after spacer etch.

![Figure 46: top down SEM image of single layer silicon nitride spacers for padless (left) and padded (right) active area FinFETs](image)

Clearly, a significant amount of spacer material exists on the fin sidewalls especially for structures with freestanding fins of width ~50nm. It has already been established that the pad less FinFET structure shown in Figure 46 has an insufficient capture cross section for implantation and would require selective epitaxy to thicken the S/D region of the transistor. Because the silicon nitride spacer covers more than ½ the fin height, epitaxy would almost certainly bridge the S/D and gate electrodes resulting in device failure.
Moreover, the standard spacer etch significantly etches both the BOX and fin near the gate edge as seen in Figure 47.

![Figure 47: cross section SEM image between fins and through the gate highlighting BOX and fin recess due to aggressive spacer etch](image)

Although the spacer footprint has been significantly trimmed to ~34nm by the over etch process, there are issues with both fin and BOX damage near the gate edge. Specifically, the silicon fin height has been reduced by ~19nm (more than 25% of $H_{\text{fin}}$) and will increase the device resistance in one of two ways:

1) if the fin is completely silicided then there is less contact area between silicide and HDD $\Rightarrow R_{\text{CON}}^{\text{silicide to HDD}}$ increases

2) if the fin is only partially silicided then the current must spread from a reduced silicon volume as it passes underneath the spacer $\Rightarrow R_{\text{SP}}^{\text{HDD}}$ increases
The fin recess could potentially be repaired by epitaxy as this will increase the fin volume. Yet another issue is the dramatic 50nm deep recessed areas in the BOX with no observable gate spacer that could potentially affect:

1) clearing of spin-on BARC and resist layers used in subsequent litho operations (implant, silicide block)

2) the stress transfer and topography of blanket deposition stressor films such as the CESL

3) profile of epitaxial silicon growth on the unprotected gate sidewall during HDD thickening (could bridge the S/D to the gate)

These observations motivate the need for a multilayer spacer that allows for clearing the fin sidewalls without the use of an aggressive dry etch.

3.2.2 Two Layer Spacer

To mitigate the loss of both silicon and BOX thickness near the gate during spacer etch, a two layer (silicon dioxide/silicon nitride) spacer is proposed. The goal is to aggressively dry etch the outermost oxide portion of the spacer while making use of the bottom nitride layer as an etch stop. In this manner, one can significantly extend the spacer over etch time without damaging either the BOX or the fin while leaving a minimal amount of spacer material on the fins. In order to fully remove the residual silicon dioxide and silicon nitride portions of the spacer from the fin sidewalls after dry etch, an H₃PO₄ wet etch at 160°C was utilized to etch both TEOS and silicon nitride while minimizing any attack on the underlying BOX. It should be noted that this scheme also relies upon the height ratio between gate and fin that should be increased as much as
Possible to maximize the effectiveness of any spacer module that requires leaving spacer on the taller vertical surface while removing it from the shorter one. Recall that this final wet etch must also clear any portions of remaining gate and fin hard masks that are impervious to the HF based salicide pre-clean. With this additional caveat in mind, the residual gate HM thickness should have been minimized to prevent excessive undercut of the bottommost silicon nitride spacer layer which is much thinner than the gate HM. Permutations of the initial gate HM thickness or thinner resist were not explored in this experiment though we did attempt to remove any remaining gate HM prior to spacer formation using phosphoric acid to mimic this effect. A simplified process sequence is shown in Figure 48.

Figure 48: process sequence for 2-layer spacer formation (depicting spacer near gate only for simplicity)

The two different types of TEOS films were utilized because of differing etch rates in hot phosphoric acid. The etch rates of exposed materials during the final wet etch of this scheme are listed in Table 5.
Interest in the use of NiSi during the mid 80s prompted engineers to develop a means of reducing the thermal budget associated with thermal decomposition of TEOS precursors in an O₂ environment to deposit ILD [64]. It was discovered that combining TEOS with ozone (O₃) could reduce the process temperature from ~700°C to ~400°C while maintaining excellent step coverage [65]. Unfortunately, the ozone based TEOS showed severe problems with moisture absorption, high silanol concentration, and intrinsic film stress [66]. Plasma excitation is another option for depositing TEOS at low temperatures and was first reported more than 4 decades ago. Modern PECVD tools can deliver high quality “dry” films at astounding deposition rates in excess of 1µm/min. Herein lies the problem: PETEOS is not well suited for thin film deposition and cannot rival the conformality of ozone based TEOS films[64]. The difference in etch rate of these two films in H₃PO₄ is attributed to the significantly higher silanol content and moisture absorption in TEOS:O₃ vs. PETEOS. Si₃N₄ etch byproducts consist of hydrolyzed silicon and ammonia thus rendering silanol rich TEOS films more susceptible to H₃PO₄. Also, increased water content from the TEOS tends to poison the phosphoric acid bath and increase the oxide etch rate [67].

The first attempt used 150Å of silicon nitride with 400Å of TEOS:O₃ as the dual layer spacer with SEM images post etch shown in Figures 49-51.

<table>
<thead>
<tr>
<th>material</th>
<th>etch rate (ER) in 160°C H₃PO₄ (Å/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>silicon nitride</td>
<td>84</td>
</tr>
<tr>
<td>thermal oxide (BOX)</td>
<td>1</td>
</tr>
<tr>
<td>ozone decomposed TEOS (TEOS:O₃)</td>
<td>52</td>
</tr>
<tr>
<td>plasma enhanced TEOS (PETEOS)</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 5: wet etch rates for silicon nitride and various silicon dioxides in phosphoric acid
Figure 49: top down SEM images of padless (left) and padded (right) FinFETs with 150Å silicon nitride/400Å TEOS dual layer spacer

This image shows a marked improvement in the amount of residual spacer material on the fin sidewalls though the contrast (darker = dielectric) seems to indicate the presence of some residual spacer material. In any case, the spacer footprint adjacent to the gate is larger than that next to the fin so the process is moving in the correct direction.

Figure 50: gate cross section SEM images in SE and BSE (inset) modes of padless FinFET structure with 150Å silicon nitride/400Å TEOS dual layer spacer
The recess of the silicon nitride layer is as expected for the wet etch duration although the higher magnification cross section image combined with the utility of BSE clearly indicates that there is still spacer or hard mask on top of the fin in at least a few places. Another observation from this image indicates the presence of a conductor cladding to the sides of the fin; a side effect of an un-optimized gate etch sequence that failed to remove some material (either polysilicon cap, gate metal, or both). Irrespective of the gate etch issues, the dual layer spacer appears continuous along the gate line as seen in Figure 51.

Figure 51: rotated tilt SEM image of padless FinFET structure with 150Å silicon nitride/400Å TEOS dual layer spacer

The last image for this spacer attempt shows two important improvements over the single nitride layer spacer:

- Little or no silicon fin recess
- Obvious spacer material between the fins implying less BOX recess
The next experimental split used a nitride portion of the dual layer spacer with half the thickness and both of the TEOS deposition methods to explore the potential advantage of material wet etch rate differences mentioned in Table 5. One other important change is the use of SWT fins rather than conventional litho fins because there now exists a small space between the SWT fins where mass transport during wet or dry etch processing may be compromised. For this reason, the RIE duration (over etch) was significantly increased for these splits. The top down SEM images for both spacer stacks are shown in Figure 52.

![Image: Figure 52: top down SEM images of TEOS:O3 (left) and PETEOS (right) based dual layer spacers post dry etch and 120sec H3PO4 wet etch at 160°C (horizontal white bars in the images are artifacts of the image recognition software used to target the devices in the CD-SEM tool)]
Both TEOS materials showed similar endpoint behavior during the dry etch where a 100% over etch showed clear indication of full access to the underlying nitride portion of the spacer. The differing wet etch rates of the two TEOS materials does not explain the difference in the spacer footprints as seen in Figure 52. We would expect a greater loss of the TEOS:O\textsubscript{3} spacer material during the 120 second H\textsubscript{3}PO\textsubscript{4} etch yet the spacer footprint is larger than the sample with PETEOS. Presumably this is due to the poor step coverage of the thin PETEOS layer; an assertion reinforced by the greater variability in the spacer line width as seen in Figure 52. If the thickness of PETEOS deposited on the gate sidewall was non-uniform and less than the thickness deposited on the BOX (a characteristic of films with poor conformality) then the subsequent RIE would leave a behind an irregular and thinner spacer. It is difficult to surmise from these images whether spacer material was completely removed from the sidewalls of the narrow fins because the top down image only reveals the width of the SWT fin HM. Nevertheless, this 2-layer spacer scheme shows a marked improvement compared to a single nitride layer spacer for pad less fins.
3.3 Epitaxial Growth in Source Drain Region

The above sections have already motivated the need for selective epitaxy in the S/D region of FinFET structures that make use of SWT to reduce fin width and increase channel width in the same device footprint. Figure 53 attempts to reinforce this point once more so that the reader has a clear understanding of the ramifications of scaling via SWT.

Figure 53: tilt view SEM image of a SWT active region showing the “removed” S/D pad previously used to capture dopants in the HDD region.

In addition to enabling efficient implant and increased contact area, selective epitaxy on the fins can provide an opportunity for strain engineering with SiGe(pMOS) or SiC(nMOS) to strain the channel and further enhance device performance due to mobility increases.
3.3.1 Epitaxial silicon Pre-clean

Surface preparation prior to selective epitaxial growth consists of a vapor HF clean to remove any native oxide from the silicon surfaces followed by a pre deposition anneal in HCl to terminate the silicon surface with hydrogen. This hydrogen termination results in silane (SiH₄) decomposition only at the silicon surfaces without the need for a plasma or high temperature that would blanket all surfaces (hence the selectivity of the process to surfaces that can be hydrogen terminated by exposure to HCl). The first attempt to grow epitaxial silicon on SWT fins utilized a number of timed runs to determine the process window. Because the test structure consisted of SWT fins only (no gate or spacer) there was a concern that the HF pre-clean might potentially recess the BOX under the narrow fins and lead to collapse. The pre-clean recipe was altered to minimize BOX recess and the results are shown in Figure 54.
Figure 54: top down SEM of various timed epi growth recipes on SWT fins with insufficient preclean (original fin profile is shown as colored bar for clarity, original \( W_{\text{fin}} \sim 15\text{nm} \)).

Although there appears to be a trend of increased epitaxial silicon thickness based on time, the weaker HF pre-clean did not completely remove the native oxide from the fin sidewalls as evidenced by the inhomogeneous epitaxial silicon coverage. The 200 second epitaxial silicon case was chosen as the optimal condition because it appears that the
SWT fins are just beginning to merge after ~35nm of epitaxial silicon growth on either side of the fins.

3.3.2 Hydrochloric Acid Pre-Bake Temperature

A subsequent experiment was conducted using the more aggressive pre-clean and two different HCl pre-deposition anneal temperatures in an attempt to minimize thermal budget impact on the high-k dielectric. The results for center and edge sites are shown in Figures 55 and 56.

Figure 55: cross section SEM images of SWT fins from wafer center (top) and edge (bottom) exposed to 700°C HCl pre-bake and 200 seconds epi growth at 800°C.
Figure 56: cross section SEM of SWT fins from wafer center (top) and edge (bottom) exposed to 800°C HCl pre-bake and 200 seconds epi growth at 800°C

It is important to note that the SWT fin hard mask (bulbous protrusion from the top of the fins) is composed primarily of silicon nitride and hence is not an active silane decomposition site due to the inability to hydrogen passivate this surface. The selectivity of the epitaxial growth process explains the lack of vertical silicon growth. It appears that increasing the difference between HCl bake and epitaxy temperatures (see Figure 55) result in a temperature gradient across the wafer and undermines center to edge uniformity. Because the profile for the 800°C pre-bake shows better uniformity between wafer center and edge die, it has been selected as the optimized process for selective epitaxy on SWT fins. As indicated in Figure 56, the total width of the epitaxially thickened SWT doublet is slightly less than the smallest available 193nm lithographically patterned contact diameter of 150nm and hence is quite amenable to making a single via
to single SWT pair contact that could dramatically reduce device area footprint for applications such as SRAM.

3.3.3 Silicide Profile on Epitaxially Thickened Fins

In order to evaluate the potential benefit of increased contact area between silicide and HDD, two epitaxially thickened fin structures blanketed with 150Å of nickel by PVD and processed using the standard silicidation anneal sequence (shown in Figure 57).

Figure 57: cross section SEM image in BSE mode of non-SWT fins with short (left) and long (right) duration epi growth followed by silicidation using 150Å Ni deposition for salicide (initial fin dimensions colored for clarity)

Although both short and long epitaxial silicon runs exhibit continuous silicide profiles, there are concerns for the impact on $R_{SD}$ for both cases. Specifically, the short epitaxial silicon case has larger contact area to the HDD portion of the fin but may provide a detrimental interface between the narrow body fin extension and silicide that will result in severe current crowding as detailed in Section 1.3. While the epitaxial silicon case prevents formation of a silicide-fin extension interface, the path length between silicide and fin extension through the HDD has increased as indicated graphically by the size of
the resistors drawn into Figure 57. Moreover, the contact area between silicide and individual fin appears to have decreased for the long epitaxial silicon (merged) case because the initial nickel deposition no longer has access to the thickened fin sides. One important note is that the optimized epitaxial silicon process for SWT fins will merge the individual fins that constitute a fin pair but not the fin doublets themselves as shown in Figure 56. This scenario is expected to separate the silicide and fin extension while maximizing the contact area and minimizing the HDD path length.

3.4 Slot Contacts

An additional process optimization to reduce $R_{S/D}$ for 3D transistor structures is maximization of contact area to the silicided HDD fin. Moreover, the use of SWT requires either targeted individual contacts that land over the fin doublets or a slot type contact for multiple fin arrays. Issues of concern are ability to land a standard ILD contact etch on a CESL deposited over topography rather than a planar S/D pad feature and the ability of conventional PVD contact liner and CVD W plug deposition to fully seal and fill the contact respectively. The initial investigation consisted of preparing an SEM cross section through a slot contact over fins via FIB prep to examine the profile of the Ti/TiN barrier and W plug over the HDD fins. Figure 58 shows the SE and BSE SEM images for a slot contacted transistor over litho patterned (not SWT) fins.
Figure 58: cross section SEM images in BSE (left) and SE (right) modes through a conventional fin array under the slot contact.

Though some voids are apparent in the CVD tungsten plug, the contact area to fins patterned at a pitch of 200nm is maximized for this structure. A top down view of the W slot is shown in Figure 59.

Figure 59: top down SEM images of a slot contact over conventional fins, structures were deembedded from the ILD and CESL using BOE and H₃PO₄ respectively.
The void volume fraction down the center of the W slot is expected to increase for shrinking contact dimensions though full coverage of fins at the bottom of the slot and sufficient conductive pathway to the metal level are still expected. The gate to drain distance of ~400nm is prohibitive for high performance devices as this increases the $R_S^{\text{silicide}}$ series resistance component. Process space to reduce this distance between contact and gate edge down to 100nm exists though shrinking as drawn gate dimensions below $L_g\sim20$nm will ultimately violate design rules regarding metal to contact overlay as indicated in Figure 60.

![Figure 60: 193nm metal level litho mask design rule constraints on gate length](image)

\[ \text{M1 pitch} \geq 140\text{nm} = (2\text{GtD} + L_g) - 2(\text{M1 to con overlap}) \]

\[ \rightarrow \text{for 193nm litho metal level, } L_g \geq 20\text{nm} \]

As seen in Figure 60, if the proximity of the source and drain metal edges is less than ~140nm, the reticle may harbor several defects that short source and drain at the first metal level for aggressively scaled devices. These issues could be mitigated with advanced reticle preparation but will be accompanied by an exponential increase in mask
cost. Higher magnification and atomic number contrast is required to determine the coverage of the Ti/TiN liner material deposited by PVD and is shown in Figure 61.

Figure 61: cross section TEM image of a fin under the slot contact

From the enhanced resolution and contrast afforded by TEM, we can observe the following:

- The via (slot) etch has removed the silicon fin that apparently acted as a hard mask for the resulting triangular oxide pillar
• The PVD derived Ti/TiN shows minimal deposition on the fin sidewalls and exhibits a thickened profile at the top of the fin in agreement with the density of field lines in the sheath bias.

Optimization of the slot etch and possibly ALD liner materials will be needed to correct these issues. A contact etch process was developed with lower power ILD and CESL etch steps to try and prevent the loss of the silicon fin. The results are shown in Figure 62.

![Figure 62: top down SEM images of optimized slot contacts over conventional (left) and SWT (right) fin arrays just after contact etch](image)

The reduced contact etch power resulted in survival of both fin types in addition to reducing the slot contact width. Electrical results for these structures will be treated in Chapter 4.
4. ELECTRICAL AND PHYSICAL DATA ANALYSIS OF TEST STRUCTURES

This section is comprised of electrical and physical characterization data to validate the utility of the novel slot contact methodology as well as attempts to reduce the magnitude of $R_S/D$ components via silicide engineering.

4.1 Silicide Sheet Resistance

The silicide sheet resistance was evaluated for the experimental splits detailed in Table 6.

<table>
<thead>
<tr>
<th>WFR #</th>
<th>N &amp; F Implants</th>
<th>Ni/Co/TaN/TiN deposition</th>
<th>Contact</th>
<th>W Liner</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NONE</td>
<td>100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TiN</td>
</tr>
<tr>
<td>4</td>
<td>NONE</td>
<td>100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ta/400A TaN</td>
</tr>
<tr>
<td>5</td>
<td>NONE</td>
<td>100A Ni/100A TiN</td>
<td>ODH + IPA rinse</td>
<td>250A Ta/400A TaN</td>
</tr>
<tr>
<td>9</td>
<td>NONE</td>
<td>100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TiN</td>
</tr>
<tr>
<td>10</td>
<td>NONE</td>
<td>100A Ni/100A TaN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
<tr>
<td>11</td>
<td>NONE</td>
<td>100A Ni/10A Co/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
<tr>
<td>12</td>
<td>NONE</td>
<td>10A Co/100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
<tr>
<td>13</td>
<td>NONE</td>
<td>50A Ni/10A Co/50A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
<tr>
<td>14</td>
<td>N @ 2keV, 3.5E15, 0deg</td>
<td>100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
<tr>
<td>15</td>
<td>F @ 2keV, 3.5E15, 0deg</td>
<td>100A Ni/100A TiN</td>
<td>HF</td>
<td>250A Ti/400A TaN</td>
</tr>
</tbody>
</table>

Table 6: various silicides used on padless fin structures

The silicide was formed over litho patterned fin arrays without any gate, spacer, or implant processing. Skipping the intervening process modules facilitated expeditious characterization of slot contacted fin structures and cost reduction (a savings of ~$16,000). Data were taken on three identical devices per die on 9 die per wafer. Several processing distinctions should be clarified at this point to assist in data interpretation:
• Wafers 2, 4, & 5 were deposited in a tool that allows for a degas step to volatilize any residual moisture that remains after the pre-clean whereas the PVD tool used for wafers 9-15 is not equipped with a heated chuck so no degas operation was available.

• Wafers 4 and 5 utilize a different contact liner material deposited in a tool without the conventional pre-sputter and degas capability of the PVD tool used for Ti/TiN liner on wafers 2, 9-16.

Due to the large number of splits, SEM cross sections have not been performed to determine the silicide thickness and hence data comparisons are of sheet resistance (~sheet resistivity for very thin films) as opposed to silicide resistivity (a material property) as explained by Equation 6.

\[
R_{sh} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} R = \frac{\pi}{\ln(2)} \frac{V_{34}}{I_{12}}
\]  

Equation 6: sheet resistance for a symmetric square sample with near ideal peripheral contacts such that contact size to sample side length is minimized; where \(\rho\) = resistivity, \(t\) = thickness, \(V_{34}\) = voltage differential between two adjacent contacts, and \(I_{12}\) = current sourced between two adjacent contacts as defined in section 2.2.3 [44]

Note that the term \(\rho/t\) is not the sample resistance and hence has units of \(\Omega/\square\) such that the resistance, \(R\) (measured in \(\Omega\)), of a sheet is simply \(R_{sh} \times \#\) of squares. The cumulative distribution of sheet resistance values for all wafers deposited without a degas operation are shown in Figure 63.
The following observations follow from the statistically robust data presented above:

- Low sheet resistance for NiSi is possible without a degas operation prior to PVD deposition → the HF etch prior to PVD deposition does not leave a large amount of residue on large (100) oriented active area silicon

- The use of a TaN layer as the oxidation barrier reduces the sheet resistance of the silicide layer → the TaN is not fully removed by the wet SPM etch used to remove un-reacted nickel and hence acts as a parallel conductor with the underlying NiSi; further discussions below will show how this situation also favorably impacts device reliability.
• A cobalt layer deposited between nickel and the underlying silicon in either a two-layer or three-layer structure increases the sheet resistance attributable to the higher silicidation temperature required to form low resistivity CoSi$_2$

• A cobalt layer deposited on top of nickel most likely prevents formation of any cobalt silicide attributable to the differences in silicidation for these two metals; Ni is the more rapid diffusing species and seeks out silicon to form the silicide whereas silicon must diffuse to a Co reservoir in order to react. The higher sheet resistance is most likely due to the formation of high resistivity CoSi due to the limited available silicon reactant.

• Any implantation scheme results in increased sheet resistance in the silicide N and F impurity species perturb the metallic bonding in the silicide and act as scattering sites

• Nitrogen implantation compromises the sheet resistance to a lesser extent than fluorine implantation due to less aggressive electron scavenging during bonding and a more homogeneous implant profile (SIMS data to follow in subsequent section)

These findings motivate the use of a TaN cap to prevent nickel oxidation prior to silicidation anneal. A comparison of NiSi sheet resistance with and without predeposition degas is shown in Figure 64.
This data shows ~30% reduction in the silicide sheet resistance is possible with a simple degas operation at 250°C to prepare the silicon surface for nickel deposition. It is expected that the aqueous HF based pre-clean just prior to nickel deposition leaves some water residue on the silicon surface that must be removed to prevent formation of native oxide. When nickel diffuses down into the silicon volume during and reacts during silicidation, oxygen is freed up and could simply act as an impurity thus increasing the resistivity of the material.
4.2 Silicide to Metal Contact Resistance

The silicide contact resistance was also evaluated for the experimental splits detailed in Table 6. As explained in section 4.1, the silicide was formed on the active pattern without any additional module processing. The Kelvin structures tested are discussed in section 2.2.1. Figure 65 shows the average contact resistivity as a function of contact diameter.

Figure 65: average contact resistivity from 25 die for a range of contact diameters

The striking difference in the standard deviation (not shown for clarity) of the silicide formed with the degas process compared to the other splits is not expected and may be related to the higher base pressure for the PVD tool used to fabricate the degas silicide sample that results in higher impurity content. All splits fall below the targeted contact resistance proposed in section 3.2 for contact diameters greater than 250nm. Assuming
the contact area can be maintained or increased for 3D devices, these silicide film stacks are on target to enable DG transistor scaling. The increasing contact resistivity as a function of via diameter is problematic and attributed to the following processing rather than materials issues:

- Shorter effective over etch duration in small vias due to mass transport during RIE
- Inefficiency of wet clean process in shrinking via diameter
- Greater void volume fraction in the W plug
- Poorer step coverage of liner materials

An extreme case for a 150nm contact (not electrically tested) shown in Figure 66 verifies some of these issues.

Figure 66: cross section SEM image of a 150nm contact

Figure 66 shows a prominent wineglass shaped void in down the center of the via indicative of pinch-off during W deposition and it is difficult to discern the PVD Ti/TiN liner sidewall coverage without higher resolution or mass contrast. The well defined top corners and vertical sidewall indicate a successful contact etch process even at smaller
dimensions. Finally, the W plug still makes maximum area of contact with underlying silicide though topography at the bottom of the via landing on fins may compromise the contact area. To clarify the spread in the data, Figure 67 shows the contact resistance distribution function for the 350nm contact diameter.

Figure 67: contact resistance cumulative distribution functions for the largest contact diameter used in this study

The uniformity and low value of the Ni/TaN silicide contact resistance for the 350nm contact are powerful incentives for the use of this film stack with the improved performance attributed to the reduction in barrier height due to better work function alignment as shown in Figure 68.
Later sections will address the nitrogen implanted specimen that may provide the additional benefit of low electron barrier height with a minimal penalty to sheet resistance and contact resistance. Figure 69 highlights the effectiveness of a tantalum based liner material for standard W plug contact schemes.

Figure 69: contact resistance for materials with either Ti/TiN or Ta/TaN liner materials
The data for the Ta/TaN split with clean B is quite scattered and several orders of magnitude higher than the maximum Contact resistance shown on the x-axis due to wafer wide device failure. It is expected that the wet clean process damaged the integrity of the contact hole. It should also be noted that the other Ta liner based sample got the standard clean prior to deposition but did not get a pre-sputter treatment prior to liner deposition that normally serves to remove any oxidized silicide at the bottom of the contact hole. Even with these limitations, the data suggest that a 15% reduction in contact resistance between via and silicide may be achieved through the use of degas prior to Ni/TaN deposition combined with pre-sputtering of the silicide surface prior to Ta/TaN liner material deposition.

4.3 Slot Contact Resistance

Silicided fin arrays were connected to the metal level through slot contacts and their I-V characteristics were taken. The modules tested consisted of 10 fin arrays at two different thicknesses and a single fin array (all exposed to the standard NiSi process) as shown in Figure 70.
Extrapolation of a linear fit for the data to the y axis produces a resistance value for a fin of zero effective length. This extracted value depends upon $R_{\text{CON}}$ via to silicide and to a lesser extent the metal and via resistances respectively. Therefore, this test structure is useful for electrically determining the contact area for the slot contact over the fin array with a much larger dataset than microscopy could reasonably provide. The “zero fin length” resistance of the ten fin modules is $\sim 4.5\, \Omega$. Given the contact resistivity of $\sim 5\times10^{-9}$ Ohm-cm$^2$ determined in section 4.2 for this particular silicide material, approximately 250nm wide slot contacts as seen in section 3.4, and a maximum active area of $4.25\times10^{-9}$ cm$^2$ (calculated from 10 fin array dimensions), these data imply 20-25% utilization of
available contact area between the fin structures and the slot contact, a number that can surely be increased with process optimization. Keep in mind that these numbers assume identical silicide resistance on 110 fin sidewalls, PVD liner coverage, and W coverage over a 3D structure.

4.4 Silicide Barrier Height

The silicide barrier height for nitrogen and fluorine implanted NiSi was evaluated using planar diode test structures. The blanket wafer was implanted and silicided to form a rectifying metal-semiconductor junction with aluminum deposited on the wafer for backside contact. Reverse bias I-V curves taken temperatures from 25-125°C were used to extrapolate current at V=0 and barrier height was calculated using Equation 7.

\[
\phi_b = \frac{kT}{q} \ln \left( \frac{AA^*T^2}{I_s} \right)
\]

where \( A^* = \frac{4\pi qk^2m^*}{h^3} \equiv 120 \frac{m^*}{m} \)

Equation 7: barrier for zero bias condition; \( k \) = Boltzman’s constant (J/K), \( T \) = temperature (K), \( q \) = fundamental unit of charge (C), \( A \) = diode area (cm²), \( I_s \) = extrapolated saturation current (A), \( m^* \) = carrier effective mass, \( h \) = Planck’s constant

Implant profiles as simulated with SRIM® are shown in Figure 71 [68].
The low implantation energies were chosen to contain the impurity near the surface in an attempt to enhance impurity segregation during silicidation by the snowplow effect. The electrical results indicate that a fluorine implant does not sufficiently modulate the barrier height for either electrons or holes given the issues with contact and sheet resistance discussed in sections 4.1 and 4.2. However, the nitrogen implanted specimen shows a substantial decrease in the electron barrier height (and the accompanying expected increase for hole barrier height) as seen in Figure 72.
Figure 72: barrier height modification using nitrogen and fluorine implantation prior to NiSi processing

The nitrogen and fluorine implant profiles were determined using secondary ion mass spectrometry (SIMS) and are shown in Figures 73 and 74.

Figure 73: SIMS profile for nitrogen implanted silicon post silicidation
The nitrogen profile throughout the NiSi layer appears mostly homogeneous whereas the fluorine seems to pile up at both the silicide-surface and silicide-silicon interfaces. The segregation behavior of the fluorine is attributed to its desire to seek out and passivate dangling bonds as well as diffusion driven by the concentration gradient. Barrier height modification must occur at the silicide-silicon interface where fluorine pileup may result in the formation of defect states within the silicon layer. These defect states would enjoy an abundant supply of electrons from the NiSi and would tend to populate up to and pin the Fermi level of the silicon. This Fermi level pinning would render the barrier height independent of the metal work function and explain the observed electrical results.

For the much more promising case of nitrogen implantation, GIXRD was employed to identify the possible NiSiN$_x$ phase formation and lattice constant as shown in Figure 75.
Figure 75: GIXRD at multiple omega settings to probe through the depth of the specimen.

The film was well matched to orthorhombic phase NiSi using powder diffraction card #380833 indicating that nitrogen did not appreciably participate in bonding schemes within the NiSi. Additionally, omega angle variation to probe deeper into the specimen did not reveal any appreciable changes in phase. This data combined with the SIMS profile suggests that nitrogen has populated interstitial sites within the NiSi matrix. One hypothesis that could potentially explain the observed barrier height reduction is strain at silicide-silicon interface. Biaxial type strain is known to induce splitting of the silicon conduction band into 2-fold and 4-fold degenerate $\Delta$ valleys that force a redistribution of the heavy and light effective mass carriers [69]. The reduced effective mass parameter used in Equation 2 would lead to a reduced contact resistance. This strain effect combined with an increased effective dopant density at the silicide-silicon interface ($\sim 2\text{e}^{21} \text{ N atoms/cm}^3$) are the expected reasons for electron barrier height reduction.

In summary, nitrogen dispersed throughout the NiSi decreases the material’s conductivity but its apparent 50% $\text{e}^-$ barrier height reduction attributed to strain induced conduction.
band splitting and effective donor density increase at the silicon interface could offset the increased $R_s\text{silicide}$ to reduce the overall series resistance.

4.5 Silicide to HDD Contact Resistance

Although an appropriate test structure similar to that treated in section 4.2 is not available to measure the contact resistance between silicide and doped fin, I have attempted to determine this value by measuring the total resistance of fins with and without a silicide blocking layer patterned over the middle of the fin as described in section 2.3.4. By comparing the resistance of these two structures, one can subtract out or neglect all other series resistance components in an attempt to quantify $R_{\text{CON sil to HDD}}$. Figure 76 shows the cumulative distribution of total resistance for silicided fin structures of varying width.

![Figure 76: total resistance for silicided fins of varying width; the fin array consists of 110 fins in parallel](image)

110
The trend of increasing resistance for thinner fins is expected given the larger volume of silicide formed when more silicon is available. The total resistance of these structures is given in Equation 8.

\[
R_{\text{TOTAL}} = 2R_{\text{CON}}^{\text{M1 to silicide}} + 2R_{\text{SP}}^{\text{silicide}} + \rho_{\text{silicide}}L_{\text{sil}}/(A_{\text{sil}})/\# \text{ of fins} \quad (8)
\]

Equation 8: total resistance of fully silicided fin structures

Because the length of the fins is more than 50\(\mu\)m, the silicide resistance dominates \(R_{\text{TOTAL}}\) for this structure. I have chosen to compare the resistance values of the fin arrays to increase the number of times a transition between silicide and HDD must occur. The I-V characteristics of show that that a fully silicided fin array has an average resistance of 2.25 +/- 0.28 \(\Omega/\mu\)m of length. A similar set of features with a silicide blocking layer were also measured with the results shown in Figure 77.

![Figure 77: total resistance of fins with an unsilicided middle portion](image)

Figure 77: total resistance of fins with an unsilicided middle portion
The expression for the total resistance of these structures is given in Equation 9.

\[
R_{TOTAL} = 2 * R_{CON}^{M1 to silicide} + 2 * R_{SP}^{silicide} + \rho_{silicide} * L_{sil}/(H_{fin} * W_{fin})/# of fins \\
+ \rho_{HDD} * L_{HDD}/(H_{fin} * W_{fin})/# of fins + 2 * R_{CON}^{silicide to HDD} 
\]  

(9)

Equation 9: total resistance of partially silicided fin structures

Here I assume as in the previous case that the resistance contributions other than HDD resistance, and \( R_{CON}^{sil to HDD} \) are negligible. For example, the portion of the fin structure that has been exposed to the silicide process is 1\( \mu \)m in length and therefore amounts to less than 1% of the total measured resistance for this structure (based on structures referenced in Figure 76). Equation 9 can now be simplified as follows:

\[
R_{TOTAL}^{silblk} \simeq \rho_{HDD} * L_{HDD}/(H_{fin} * W_{fin})/# of fins + 2 * R_{CON}^{silicide to HDD} 
\]  

(10)

Equation 10: simplified resistance for fin array with a silicide block

\( R_{TOTAL} \) is determined empirically while the two remaining components are not easily separated from one another because the silicon resistance can be calculated only if the doping concentration and dimensions are well known. Measuring the doped silicon line resistance is possible but would be accompanied by a changed probe contact resistance in place of the silicide. In an effort to solve for the remaining unknown and quantify \( R_{CON}^{silicide to HDD} \), implant simulations for these structures were used to estimate the doping concentration as shown in Figure 78.
It is reasonable to assume that the activation anneal will result in $1e19$ to $5e19$ activated dopant atoms/cm$^3$ though there is no simple means of determining this absolute value. Given these boundary conditions on doping concentration, the silicon resistivity can then be calculated and combined with fin dimensions based on SEM cross sections of similarly processed wafers to allow for subtraction of the HDD resistance component leaving only a value for $R_{\text{CON}}^{\text{silicide to HDD}}$. Since there are many assumptions made during this analysis, I offer a targeted range of expected behavior in Figure 79.
Figure 79: contact resistance between silicide and HDD dominates total resistance for a fin array structure.

This figure serves to illustrate the robust nature of this analysis and any the effect of any errors in my above assumptions are addressed as follows:

- Doping concentration – the convergence of the $R_{\text{CON}}/R_{\text{TOTAL}}$ percentage at higher doping concentrations is due to the asymptotic behavior of the silicon resistivity above 5e19 atoms/cm$^3$ (see Figure 80) such that even a 1-2 order of magnitude error in the doping concentration will not change the calculated fin resistance by more than $\sim$10%.
The specific fin dimensions are known to vary WIW and WTW so a range of potential fin widths are given to highlight the other source of error in my calculation of fin resistance. Put simply, if the empirical data I am using to generate this plot comes from small fins then the $R_{CO}$ impact is not as severe whereas wider fins would imply a smaller $R_{\text{silicon}}$ contribution to the total resistance making $R_{CO}$ much more severe.

Given the above stipulations, it is reasonable to conclude that $R_{\text{CON}_{\text{sil to HDD}}}$ for an arsenic implanted silicon-NiSi interface comprises 40% or more of the total resistance.
5. CONCLUSION

Several key process modules and silicide engineering techniques were examined to enable FinFET transistor scaling to the 16nm node and beyond. Three different sidewall transfer methods to decrease \( W_{\text{fin}} \) were demonstrated with processing complexity and layout advantages described for each. The use of a TEOS spacer as a HM for SOI fin definition has produced fins with an average width of less than 10nm allowing gate length scaling to 16nm or lower without suffering from severe SCE. Amorphous silicon spacer HM is also shown to be quite scalable but significant optimization of oxide fin structures is still required to fabricate thin fins with acceptable LER. Eliminating the use of spacers can decrease the pitch of the resulting SWT fins though the process window for controlling the oxidized sidewall thickness is very narrow. Elimination of conventional S/D pads during sidewall transfer requires the use of a gate spacer process that leaves little or no material on the vertical fin sidewalls while still maintaining spacer integrity at the gate edge. A two step etch was employed to pattern a TEOS/silicon nitride spacer whereby the TEOS layer is dry etched and the thin silicon nitride layer is wet etched to remove most of the spacer material from the fins. Subsequent epitaxial silicon growth was developed to augment the dopant capture cross section of the narrow SWT fins during implant in addition to increasing the contact area between silicide and the HDD portion of the fin to reduce \( R_{\text{S/D}} \). A novel contact scheme was developed to connect the first metallization level to the source and drain of a pad-less fin array by
trenching out a slot in the ILD while dealing with active area topographic variation due to the 3D nature of the device. Silicide engineering consisted of introduction of Co interlayers as well as F and N implants. Introduction of cobalt during nickel deposition results in higher sheet resistance when there is insufficient thermal budget to enable formation of CoSi$_2$ though the barrier height to silicon was not evaluated. The effects on sheet resistance and barrier height indicate that nitrogen implanted NiSi may facilitate low barrier height for nMOS devices whereas F implantation has little or no effect on barrier height due to Fermi level pinning at the silicide-silicon interface. The use of TaN as an oxidation barrier for NiSi and/or the W plug liner material alongside pre-deposition surface treatment techniques are shown to decrease the contact resistance between metal and silicide. Finally, the contact resistance between a silicided and arsenic doped fin structure is estimated to be 40% or more of the total series resistance outside the channel and further motivates the need for novel silicides to offset the device degradation that will occur for aggressively scaled 3D devices.

Future work intended to optimize certain process modules and explore additional means of reducing $R_{S/D}$ are underway. The specific issues to be addressed are listed below:

- Employing a recursive SWT process whereby spacer patterning is applied twice before final fin definition will radically reduce pitch and quadruple channel width per device area footprint. Although this is a very attractive means to increase device density, the applicability of existing SWT schemes is questionable given the additional number of RIE operations at successively smaller pitch.
• The ISSG oxidation behavior observed for SWT scheme #3 warrants further investigation. Test structures consisting of amorphous or polycrystalline silicon fins patterned with a Si$_3$N$_4$ HM and sitting on a blanket Si$_3$N$_4$ layer. Rapid thermal anneals to modify the hydrogen content prior to dry and wet oxidation runs will provide a means for testing my hypothesis that H$_2$ out-gassing limits the oxidation rate for the unique sidewall oxidation structure reported in this work.

• I intend to develop processes for selectively growing SiGe and SiC on SWT fins that will provide a means for significantly stressing the channel and increasing carrier mobility for pMOS and nMOS transistors respectively. In addition, depositing SiGe with different Ge content provides a means of tailoring the applied strain to aid in identification of stress transfer mechanisms into a 3D channel structure.

• The observed electron barrier height lowering due to nitrogen implantation may be linked to residual stress in the NiSi and hence test structures must be developed to verify N implantation scheme effectiveness on FinFETs that may have different stress transfer mechanisms and implantation cross section.
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