STUDY OF GATE ELECTRODE MATERIALS ON HIGH-K DIELECTRICS

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This problem in lieu of thesis report presents a study on gate electrode materials on high K dielectrics, including poly-SiGe and Ru.

The stability of poly-SiGe in direct contact with Hf silicon-oxynitride (HfSiON) is studied by Rapid Thermal Annealing (RTA), Rutherford Backscattering Spectrometry (RBS), X-ray photoelectron Spectroscopy (XPS) and High Resolution Transmission Electron Microscopy (HRTEM). By performing a series of RTA treatments we found that as RTA thermal budgets reach 1050°C for 30s, the poly-SiGe layer begins to intermix with the HfSiON film, as observed by TEM. The maximum annealing condition for the Hf$_{0.14}$Si$_{0.23}$O$_{0.46}$N$_{0.17}$ film to remain stable in contact with poly-SiGe is 1050°C for 20s in high purity N$_2$ (99.9%) ambient. We also found that after 1000°C annealing for 60s in a nitrogen ambient, the poly-SiGe crystal phase structure was changed from a columnar structure to a large grain structure.

For a metal gate, Ru was studied to determine N$_2$ annealing effects on sheet resistance of Ru sample electrodes and electrical characterization of Ru/HfSiO$_x$/Si stack. Results show that a pure Ru metal gate is not a good choice for high k materials since it is hard to etch off, and different annealing conditions can cause large changes in the electrical behavior.
ACKNOWLEDGMENTS

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STUDY OF GATE ELECTRODE MATERIALS ON HIGH-K DIELECTRICS

1. Introduction

As silicon complementary metal-oxide-semiconductor (CMOS) devices are scaled below 100 nm, advanced high-K gate dielectrics will be required to obtain an equivalent oxide thickness (EOT) < 1.0 nm. As EOT decreases, the poly-Si gate depletion problem becomes severe, making it necessary to consider alternative gate electrode materials, such as poly-SiGe and metals. The search for appropriate gate materials in CMOS devices presents many challenges such as (a) low resistivity (< 10^{-5} Ohm-cm), (b) compatible work function, (c) process compatibility, and (d) thermal/chemical interface stability with dielectrics.¹

The research reported here examines gate electrode materials on high-K dielectrics, including poly-SiGe and Ru metal.

For the poly-SiGe gate, the stability of poly-SiGe in direct contact with Hf silicon-oxynitride (HfSiON) is studied by Rapid Thermal Annealing (RTA), Rutherford Backscattering Spectrometry (RBS), X-ray photoelectron Spectroscopy (XPS) and High Resolution Transmission Electron Microscopy (HRTEM).

For a metal gate, Ru was studied to determine N₂ annealing effects on sheet resistance of Ru sample electrode and electrical characterization of the Ru/HfSiOₓ/Si stack.
1.1 The depletion problem in the poly-Si gate

To understand the poly-Si gate depletion problem, the different bias modes of a p⁺-doped poly-Si gate/dielectric/n-type Si substrate stack under three different bias voltages are introduced: (a) The accumulation mode, where the gate voltage \( V_G \) > the flatband voltage \( V_{FB} \); (b) The depletion mode, where the flatband voltage \( V_T < V_G < V_{FB} \); and (c) The inversion mode, \( V_G < V_T \).²

These three modes, as well as the charge distributions associated with each of them, are shown in Figure 1.

Figure 1. Charges in a p⁺-doped poly-Si gate/dielectric/n-type Si substrate structure under accumulation, depletion and inversion conditions
For a p^+-doped poly-Si gate/dielectric/n-type Si substrate stack:

Accumulation mode: the accumulation mode occurs when the positive voltage is applied on the gate. The positive charge on the gate attracts electrons (Majority carriers in n-type Si substrate) from the substrate to the oxide-semiconductor interface. This results in a higher concentration of electrons near the interface than that in the bulk for the n-type Si substrate.

Depletion mode: The depletion mode occurs when a negative voltage is applied on the stack. The negative charge on the gate pushes the electrons away from the dielectric/Si substrate. Therefore, the n-type semiconductor is depleted of majority carriers (electrons) at the interface and a positive charge, due to the ionized donor ions, is left in the space charge region. The voltage separating the accumulation and depletion regime is referred to as the flatband voltage, $V_{FB}$.

Inversion mode: The inversion mode occurs when a negative voltage beyond the threshold voltage is applied on the gate stack under consideration. In inversion, there exists a positively charged inversion layer at the oxide-semiconductor interface in addition to the depletion-layer. This inversion layer is due to minority carriers, which are attracted to the interface by the negative gate voltage.

The poly-Si gate depletion problem always occurs when a MOS capacitor is biased into depletion or inversion. Let us consider a PMOS capacitor which has p^+-doped poly-Si gate and an n-doped silicon substrate.

Figure 2 shows energy-band diagrams that depict the two situations of a PMOS capacitor (without depletion and under depletion). (“+” means “heavily doped”, doping concentration $\geq 10^{19}$/cm$^3$)
For p+-doped poly-Si gates, a negative bias applied between the gate and substrate causes either depletion or inversion in the silicon substrate. The charge induced in the silicon substrate by this biasing is positive. An equivalent negative charge must exist in the gate. For the poly-Si gate, acceptor ions in the p+-doped poly-Si constitute this negative charge, and it causes a depletion region of some finite thickness to be formed in the gate. This depletion region in the gate is the basis of poly-Si depletion. $\Psi_p$ in Figure 2(b) represents the voltage drop caused by this depletion. This voltage drop and the depletion layer cause a depletion capacitance.

The effect of this depletion on the total capacitance of an ideal MOS stack is described next. First, we consider an ideal MOS capacitor.
The capacitance, $C$, of an ideal MOS capacitor is given as

$$C = \kappa \varepsilon_0 \frac{A}{t_{\text{ox}}} = \kappa_{\text{SiO}_2} \varepsilon_0 \frac{A}{t_{\text{eq}}} ,$$

where $\kappa$ is the gate oxide dielectric constant, $\varepsilon_0$ the permittivity of vacuum, $A$ the capacitor area, and $t_{\text{ox}}$ gate oxide physical thickness. By assuming the same capacitance is achieved using $\text{SiO}_2$ as the dielectric, the equivalent oxide thickness $t_{\text{eq}}$ is given by

$$t_{\text{eq}} = t_{\text{ox}} \frac{\kappa_{\text{SiO}_2}}{\kappa} ,$$

which means a thicker gate dielectric of high permittivity can hold the same gate capacitance as a thinner $\text{SiO}_2$ dielectric. The near-term gate dielectric solution in the semiconductor industry has been chosen as ultra-thin silicon dioxide with a nitrided interface or oxynitride films, based on years of research and a thorough understanding of their materials characteristics.\(^1\)

Figure 3 provides the reader a schematic overview of the total capacitance in the gate stack. The gate dielectric insulates the gate electrode-gate from the Si substrate. Gate electrodes in modern CMOS technology are composed of polycrystalline Si (poly-Si) which can be highly doped (e.g. by ion implantation) and subsequently annealed in order to substantially increase conductivity through dopant activation (by driving dopants into electrically active substitutional sites).
In this gate stack, the total capacitance is calculated by the formula:

\[
\frac{1}{C} = \frac{1}{C_{\text{poly-dep}}} + \frac{1}{C_{\text{OX}}} + \frac{1}{C_{\text{inv}}}
\]

\(C\): The total capacitance of this gate stack

\(C_{\text{poly-dep}}\): The capacitance due to the depletion in the gate

\(C_{\text{OX}}\): The capacitance of the dielectric

\(C_{\text{inv}}\): The capacitance due to the inversion in the substrate

The depletion capacitance due to the poly-Si depletion is in series with the dielectric capacitance. Thus the smaller capacitor largely determines the total capacitance value. In this case, the capacitance of the dielectric is much smaller than the capacitance due to the depletion until the dielectric thickness gets below about 5.0nm.
When the dielectric thickness is < 5.0 nm, the capacitance of the dielectric is so large that the capacitance due to the depletion begins to impact the total capacitance.

The degree of capacitance reduction depends on the poly Si doping concentration, the higher the doping concentration, the smaller the depletion effect. The doping concentration limits are $10^{20}/\text{cm}^3$ for n-type poly-Si and $10^{19}/\text{cm}^3$ for p-type poly-Si due to solubility limits for dopant atoms in silicon.

The poly-Si depletion problem will become worse as the dielectric thickness continues to decrease.

### 1.2 Metal gate materials for the future CMOS stack

Metal gates are the best choice for replacement of poly-Si since they are free of gate depletion and boron penetration issues, and they offer low resistance in narrow gate line widths.  

Metal gates have advantages over poly-Si gate electrodes in sub-50nm CMOS applications. First, they can eliminate gate depletion, boron penetration problems, and typically have very low sheet resistance since a metal has a Fermi sea of electrons right

![Figure 4](image-url)
up to the dielectric interface. Also, metal gates eliminate the need for ion implantation (such as Boron implantation) into the gate to reduce the resistivity.\textsuperscript{6,7}

Second, some alloys have a low sheet resistance with an amorphous structure. This implies that, since we do not require a high thermal budget to fully crystallize a metal gate to obtain low resistivity, we can alleviate inter-diffusion between the gate, the gate dielectric and the substrate caused by high temperature annealing. It has been recently found that amorphous ternary films such as Ta-Si-N exhibit good interfacial stability in direct contact with HfO\textsubscript{2}.\textsuperscript{8}

Finally, due to the large electronegativity differences between metal and silicon atoms, chemical reactions are more likely to occur at poly Si/metal oxide interfaces and cause possible interfacial layers compared with metal gate/metal oxide gate stacks. Metal gates with similar properties to the metal atoms in the dielectric layer appear more promising than poly-Si to minimize the interfacial layer between the gate and the dielectric, when we use metal oxides instead of SiO\textsubscript{2} as the high-K dielectric in the future. These compatibility issues between poly-Si and ZrO\textsubscript{2} and poly-Si and HfO\textsubscript{2} dielectrics also require consideration.\textsuperscript{9}

However, unlike a poly-Si gate which controls the required work function for CMOS by the dopants’ concentration and type (donor or acceptor), it is difficult to attain pertinent metal gate electrodes having a suitable $\Phi_M$ for the surface channel CMOS devices.\textsuperscript{10}

For conventional device operation, the gradual channel approximation for a field effect transistor indicates that the drive current is given by:
\[ I_{D,\text{sat}} = \frac{W}{L} \mu C_{inv} \frac{(V_G - V_T)^2}{2}. \]

where \( W \) is the width of the transistor channel, \( L \) is the channel length, \( \mu \) is the channel carrier mobility, \( C_{inv} \) is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state, \( V_G \) and \( V_T \) are the gate voltage and threshold voltage respectively.\(^{11}\)

It can be seen that we must reduce \( V_T \) in order to get high current when the gate voltage is required to decrease as the size of the CMOSFET device decreases. \( V_T \) cannot be reduced below 0.2 V with adequate margin for the control of electron thermal emission, since \( kT \) is 0.025eV at room temperature. Therefore classical simulations, for conditions where the substrate is unbiased, indicate that the optimal work function is such that the gate Fermi level for NMOS (PMOS) devices is 0.2 eV below (above) the band edge \( E_c \) (\( E_v \)).\(^{12}\)

However, when quantum mechanical effects (such as quantum-mechanical penetration of the electron/hole wavefunction from the silicon channel into the dielectric) are included in the simulations, the oxide effectively becomes thicker and correspondingly the substrate doping to meet off-state leakage specification also becomes lower. In this case, the optimal work function for metal gates is such that the gate Fermi level has been established to be 0.35eV below (above) the conduction (valence) band edge in NMOS (PMOS) devices.\(^{13}\)

For midgap metal gates, according to Figure 4(a), the threshold voltage for any midgap metal on Si will be \(~0.55\)eV for both NMOS and PMOS. Since the drain current of a MOSFET device, \( I_{D,\text{sat}} \), is proportional to \((V_G - V_T)^2\) and voltage supplies are expected
to be $\leq 1.0\text{V}$ for sub-0.13 $\mu\text{m}$ CMOS technology, $V_T \sim 0.55\text{eV}$ will cause a reduction in the drain current. Using midgap metal gates will make it difficult to turn on the device, and therefore have been predicted not to be a good substitute for poly-Si gates in standard CMOS structures.

For two separate metals gates, one for PMOS and one for NMOS devices, as shown in Figure 4 (b), two metals could be chosen by their work functions.

In practice, it is very hard to find two metal gates with the required work function. For NMOS, the $\Phi_M$ value of Al could achieve $V_T \sim 0.35\text{eV}$ but aluminum will reduce nearly any oxide gate dielectric to form an $\text{Al}_2\text{O}_3$-containing interface layer. Similarly for PMOS, Au has a work function value of $5.1\text{eV}$ and could achieve $V_T \sim 0.35\text{eV}$, but Au is not a practical choice for the gate metal, since it is difficult to process, does not adhere well to most dielectrics, and is expensive. Other elemental metals with high $\Phi_M$ values such as Pt are also not practical, for the same reasons as for Au.  

Also, considering industrial costs and thermal/chemical interface stability issues with dielectrics, metal gates are not expected to be applied in standard-scaled CMOS fabrication in the industry until 2007.

In this report, we study some basic properties of Ru metal gates on high-K materials.

1.3 Poly-SiGe as an intermediate gate material

By the addition of Ge atoms into the poly Si gate, one can minimize the gate depletion problem, since poly-SiGe has a narrower bandgap than poly-Si and it provides a better dopant activation than in poly-Si. Hence poly-SiGe will likely serve as an
intermediate gate material, prior to the introduction of metal gates, although poly-SiGe has limited sheet resistance and depletion problems.

The annealing conditions for poly-SiGe are very important. If the thermal budget is insufficient, the poly-SiGe layer will not be completely crystallized and dopants will not be fully activated. This will result in high resistivity films. Additionally, interfacial layer formation between the poly-SiGe layer and the gate dielectric must be considered.

T.-J. King, et al. have deposited poly-Si$_{0.74}$Ge$_{0.26}$ directly onto thermally oxidized 100mm-diameter Si wafers (i.e. SiO$_2$) in a conventional low-pressure chemical-vapor deposition (LPCVD) system, at 625 °C and pressures between 0.1 torr and 0.2 torr. The electrical properties of poly-Si$_{0.74}$Ge$_{0.26}$ make it a potentially favorable alternative to poly-Si gate on SiO$_2$ dielectrics in MOSFET applications.$^{18}$

In this report, we study the effects of rapid thermal annealing (RTA) conditions on poly-SiGe in direct contact with HfSiON.
2. Experimental procedures and characterization methodologies

2.1 Materials

Table 1 lists the materials and equipment used in this work.

Table 1 Materials and equipment used in the experiments

<table>
<thead>
<tr>
<th>Materials</th>
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<tr>
<td>4294A Precision Impedance Analyzer, 40 Hz to 110 MHz</td>
<td>Agilent Technologies, Palo Alto, CA</td>
</tr>
<tr>
<td>4156B Semiconductor Parameter Analyzer</td>
<td></td>
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<tr>
<td>16048H cables (Four-terminal pair 2 m)</td>
<td></td>
</tr>
<tr>
<td>Keithley 7002 switch matrix</td>
<td>Keithley Instruments Company (Cleveland, Ohio)</td>
</tr>
<tr>
<td>MC Systems Probe Station enclosed by a MicroManipulator Shielding Box</td>
<td>The Micromanipulator company (Carson City, NV)</td>
</tr>
<tr>
<td>Phosphoric acid (85%, CMOS)</td>
<td>VWR Scientific products (Buffalo Grove, IL)</td>
</tr>
<tr>
<td>Hydrochloric acid (38%, CMOS)</td>
<td></td>
</tr>
<tr>
<td>Nitric acid (70%, CMOS)</td>
<td></td>
</tr>
<tr>
<td>Sputter targets:</td>
<td>Kurt J. Lesker Company (Livermore, CA 94551-4909)</td>
</tr>
<tr>
<td>Ru (99.95% purity) 2.0” diam x 0.125</td>
<td></td>
</tr>
<tr>
<td>Al (99.999% purity) 2.0” diam x 0.125</td>
<td></td>
</tr>
<tr>
<td>Si (99.9999% purity) 2.0” diam x 0.125</td>
<td></td>
</tr>
<tr>
<td>Sputter source: (Model number: TM02U)</td>
<td>Kurt J. Lesker Company (Livermore, CA 94551-4909)</td>
</tr>
<tr>
<td>Max. sputter power: DC 2kw and RF 0.6kw</td>
<td></td>
</tr>
<tr>
<td>Cathode voltage: 200V to 1000V</td>
<td>Kurt J. Lesker Company (Livermore, CA 94551-4909)</td>
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<tr>
<td>--------------------------------</td>
<td>--------------------------------------------------</td>
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<tr>
<td>Min. water (@ 25°C): 0.5 gpm</td>
<td></td>
</tr>
<tr>
<td>Target diameter: 2&quot;</td>
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<tr>
<td>Target thickness: 0.050&quot; - 0.25&quot;</td>
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<tr>
<td>Target fixture: Clamped</td>
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<td>Target geometry: Circular</td>
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<tr>
<td>Mounting flange: 6&quot; CF</td>
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<tr>
<td>Pyrometer control: 150°C to 1300°C</td>
<td></td>
</tr>
<tr>
<td>Hf silicate film was prepared by sputter deposition of Hf silicide (2.5 minutes deposition with Ar pressure 10 mTorr and the power 50 watts) followed by UV ozone oxidation (45 mins with O2 pressure 400 Torr)</td>
<td>The Laboratory for Electronic Materials and Devices (LEMD)</td>
</tr>
<tr>
<td>A Ru (electrode) film (~100 nm) was sputtered in metal evaporation chamber (deposition for 1 hour at 15 mTorr and RT)</td>
<td>LEMD</td>
</tr>
</tbody>
</table>

Hf silicate film was prepared by sputter deposition of Hf silicide (2.5 minutes deposition with Ar pressure 10 mTorr and the power 50 watts) followed by UV ozone oxidation (45 mins with O2 pressure 400 Torr)

A Ru (electrode) film (~100 nm) was sputtered in metal evaporation chamber (deposition for 1 hour at 15 mTorr and RT)
An Al (electrode) film (~200 nm) was sputtered in metal evaporation chamber (deposition for 1 hour at 30 mTorr and RT).

In this work, all of the pictures are taken with an ERGOLUX Microscope and a WILD MPS 05 camera using either a 50x lens, 20x lens or 5x lens (calibrated magnification: 644, 233 and 68 respectively, calibration was done by using the copper 200 mesh, ERNEST F. FULLAM Inc. 900 Aibany-Shaker Rd. Catham, NY 12110).

2.2 Experimental procedure

2.2.1 Fabrication process of poly-SiGe/HfSiON/SiOₓ/Si stack

We used sputter deposited HfSiON films, which are provided by the Silicon Technology Development group of Texas Instruments.

The film structure is as follows: HfSiON+SiO₂ (2.5nm)/Si (100).

HfSiON film composition: Hf=0.14 Si=0.23 O=0.46 N=0.17 determined by XPS results.

The SiGe layer was deposited by sputter deposition in a high vacuum chamber (10⁻⁸ mbar base pressure). A Si target (99.9% purity Si) was used with small pieces of Ge (about 0.5cm x 0.5cm) placed on the Si target surface. Before placing the Ge pieces on the Si target, we use a 49% HF etchant to clean the Ge pieces since Ge easily oxidizes in the atmosphere. By changing the number of Ge pieces on the Si sputter target, we can control the Ge composition to about 25 atomic% in the sputtered poly-SiGe layer. From RBS analysis of the sputtered samples, the Ge composition has been controlled.
successfully to ~25 atomic% in the poly-Si$_{1-x}$Ge$_x$ layer by putting 3 Ge pieces (99.999% purity Ge) on the target. (5% of the target is covered with Ge.)

The poly-SiGe layer thickness is mainly affected by sputtering power, sputtering time and Ar pressure. As required by HRTEM sample preparation, the poly-SiGe thickness should be thick enough (40nm – 80nm) to enable adequate TEM sample preparation. According to TEM images of sputtered samples, the poly-SiGe thickness is about 70nm after a 30 min deposition at 100W sputtering power and 15 mtorr Ar pressure.

Since insulating Si oxides and Ge oxides will degrade conduction in the poly-SiGe layer, we also need to minimize the amount of oxygen in the poly-SiGe film.

Rapid thermal annealing (RTA) of the poly-SiGe samples was performed in a high purity (99.9%) N$_2$ ambient with a pressure ~740 torr. A series of annealing treatments were prepared as shown in table 2:

Table 2 Annealing conditions used in this work

<table>
<thead>
<tr>
<th>Annealing temperature</th>
<th>Annealing Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unannealed (for reference)</td>
<td>—</td>
</tr>
<tr>
<td>950°C</td>
<td>30</td>
</tr>
<tr>
<td>1000°C</td>
<td>10, 30, 60</td>
</tr>
<tr>
<td>1050°C</td>
<td>10, 20, 30, 60, 80, 120</td>
</tr>
</tbody>
</table>
2.2.3 Fabrication process of Ru/HfSiOx/SiOx/Si stack

2.2.3.1 HfSiOx film fabrication process

The HfSiOx layer is deposited by Ar sputtering on the 100mm Si wafer in a high vacuum chamber (10^{-8} mbar base pressure). A HfSi2 target was used. Before loading the Si wafer into the PVD chamber, we use the complete RCA cleaning process (shown in the table 3) to clean wafer surface since Si easily oxidizes in the atmosphere.

First, the Si wafer needs to be cleaned prior to Hf silicate formation because of contamination and defects on the surface, such as particles and metal contamination, which lead to poor uniformity in sputter deposition and therefore degraded electrical
properties such as electrical breakdown, lower device lifetime and high leakage. The n-type (100) Si wafer (resistivity 0.01-0.02 Ωcm) was cleaned by the procedure listed in Table 3. The HfSi₂ film is produced by sputter deposition of Hf Silicide on a clean silicon wafer for 2.5 minutes with 10 mTorr Ar pressure and 25 watts power. The silicide was then oxidized to form a silicate by UV ozone in the UV ozone loadlock (Shown in the figure 5) for 45 mins with O₂ pressure of 400 Torr.

Table 3 Si wafer cleaning procedure (“RT” means room temperature)

<table>
<thead>
<tr>
<th>Cleaning steps</th>
<th>Time (min)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blow away particles with clean filtered N₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in acetone (b.p.56°C)</td>
<td>1</td>
<td>RT</td>
</tr>
<tr>
<td>(To remove organic contamination)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in H₂SO₄:H₂O (1200:300 V)</td>
<td>10</td>
<td>90</td>
</tr>
<tr>
<td>(To grow chemical oxide and remove organics)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in H₂O:HF:H₂O₂ (400:6:200 V)</td>
<td>1</td>
<td>RT</td>
</tr>
<tr>
<td>(To remove oxide and reduce metal contamination)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in NH₄OH:H₂O:H₂O₂ (250:1250:250 V)</td>
<td>5</td>
<td>80</td>
</tr>
<tr>
<td>(To remove organics and metal contamination)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in HCl:H₂O:H₂O₂ (250:200:1200 V)</td>
<td>10</td>
<td>80</td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Immerse wafer in H₂O:HF: (200:4 V)</td>
<td>1</td>
<td>RT</td>
</tr>
<tr>
<td>Rinse wafer with flowing DI water</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Dry wafer with clean filled N₂</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.2.3.2 Metal deposition on silicate film

An Al film (~ 410 nm) was sputtered in the metal evaporation chamber (deposition for 1 hour at 30 mTorr and RT) for backside ohmic contact. A Ru electrode film (~200nm) was deposited through a shadow mask by sputtering in the Physical Vapor Deposition (PVD) chamber (deposition for 1 hour at 15 mTorr and 100 Watts) for the top contact.

2.3 Physical and Chemical Characterization Techniques

To study the physical structure and the chemical characteristics of the gate stacks, microstructural and microanalytical analysis were performed. High-resolution transmission electron microscopy (HRTEM), X-ray photoelectron spectroscopy (XPS), and Rutherford backscattering spectrometry (RBS) were the main techniques.

2.3.1 TEM Analysis

Transmission electron microscopy (TEM) is a very powerful materials and thin-film analysis technique, which has the ability to provide structural and chemical information at very high resolution (2 Å is now common). Many books have been written regarding its configuration and theories of image contrast formation. The conventional TEM is capable of imaging a specimen and providing selected-area-diffraction patterns (SADP’s). High-resolution TEM (HRTEM) is a specialized TEM technique which uses phase contrast to generate images which reflect the periodicity of the specimen and in some cases can reveal atomic-level information. Interpretation of high-resolution images in terms of atomic position is complex. The text by Spence is an
excellent review of the theories and practical applications of HRTEM.\textsuperscript{22} For this research, HRTEM has been used to study the dielectric/Si and dielectric/electrode interfaces. Most of the gate dielectrics are amorphous films, and mass-thickness contrast is the primary source to differentiate dielectric layers in conventional TEM. The physical basis for mass-thickness contrast interpretation can be found in Reimer’s book.\textsuperscript{23}

HRTEM image analysis was performed under Dr. Moon Kim’ guidance.

2.3.2 TEM Specimen Preparation Techniques

A uniformly thinned TEM specimen with low contamination is crucial for microanalysis. For cross-sectional TEM studies, there are many ways to prepare specimens for the TEM. There are books devoted to this topic.\textsuperscript{25} For our HRTEM samples, the preparation way is described as follows: First, the sample is cut and glued together to produce several layers, rather like a club sandwich. Then the sandwich is sectioned such that we can see the layers and encase them in a 3-mm thin-walled tube. After that, the tube is polished by a semiautomatic MultiPrepTM polishing system. Finally, the sample is then thinning down to electron transparency by Ar ion beam milling. All the HRTEM samples were prepared by Jiang Huang, Donghyu Cha and Chun Yao.

2.3.3 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), uses the interaction of X-rays with core-level electrons to identify the chemical species at the sample surface. Electrons can be emitted from an orbital with photoemission occurring for X-ray energies exceeding the binding energy. XPS is a surface analysis technique and only sensitive to the upper 6~10 nm of the
sample because of the limited escape depth of the photoelectron. The major strength of XPS is that it provides not only elemental identification but chemical information as well. X-ray photoelectron spectroscopy was used in this study to determine the elemental ratios in certain films as well as their chemical states. More information about the technique can be found in the book by Briggs and Seah\textsuperscript{26}.

Figure 6 shows the X-Ray Photoelectron Spectroscopy system (monochromatic and twin anode sources) in LEMD.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{image6.png}
\caption{X-Ray Photoelectron Spectroscopy system (monochromatic and twin anode sources) including Ar ion depth profiling technique in LEMD}
\end{figure}
2.3.4 Rutherford backscattering spectrometry

Of all the analytical techniques, Rutherford backscattering spectrometry is perhaps the easiest to understand and to apply because it is based on classical scattering in a central-force field.

Figure 7 shows a conceptual layout of a backscattering spectrometry system. A collimated beam of mono-energetic He\(^+\)-ions is accelerated toward the sample by the Pelletron accelerator. A small fraction of the impinging ions will backscatter. The backscattered ions produce an energy spectrum, from which three kinds of information can be extracted: (i) the energy loss depends on the incident mass \(M_1\) (\(M_{\text{He}}=4\)) and the mass of the target scattering atom \(M_2\), consequently the mass \(M_2\) can be determined for light mass elements; (ii) information about the depth profile can be extracted, because of additional energy loss due to electronic stopping, and (iii) the concentration of the atoms in the sample can be obtained. The energy of the backscattered He\(^+\)-ions is measured with
semiconductor nuclear particle detectors which have an output voltage pulse proportional to the energy of the particles scattered from the sample into the detector.

The technique is quantitative because MeV He ions that undergo close-impact scattering collisions are governed by the Coulomb repulsion between the positively charged nuclei of the projectile and target atom.

Backscattering measurements are also insensitive to electronic configuration or chemical bonding within the target due to the independence between chemical bonding and the kinematics of the collision.27

Four basic physical concepts enter into backscattering spectrometry. Each one is at the origin of a particular capability or limitation of backscattering spectrometry and corresponds to a specific physical phenomenon.

They are:

1. Energy transfer from a projectile to a target nucleus in an elastic two-body collision. This process leads to the concept of the kinematic factor and to the capability of mass determination.

2. Likelihood of occurrence of such a two-body collision. This leads to the concept of scattering cross section and to the capability of quantitative analysis of atomic composition.

3. Average energy loss of an atom moving through a dense medium. This process leads to the concept of stopping cross section and to the capability of depth determination.

4. Statistical fluctuations in the energy loss of an atom moving through a dense medium. This process leads to the concept of energy straggling and
is a limitation in the ultimate mass and depth resolution of backscattering spectrometry.

The LEMD Rutherford backscattering system is shown in Figure 8.

This accelerator is a model 9SH Pelletron (R) accelerator built by National Electrostatics Corporation. The instrument provides ions (H, He, N, Ar) with energies from 50 keV to 3MeV for surface and thin-film analysis using ion beam characterization.

The accelerator beam lines provide a vacuum envelope for the ion beam to analytical stations which can be used for Rutherford Backscattering, ion channeling, nuclear reaction analysis, Proton Induced X-ray Emission studies of materials and elastic recoil detect ion analysis of materials.

Dr. Mohamed El Bouanani provided the accelerator parameters setup. The RBS samples were prepared, loaded and analyzed under Dr. Mohamed El Bouanani’s guidance.
2.4 Electrical measurement

A number of electrical measurements were performed to extract the electrical parameters from various gate dielectrics. These measurements included capacitance-voltage (C-V) and current-voltage (I-V) measurements. From these measurements, parameters such as equivalent oxide thickness (EOT), capacitance equivalent oxide thickness (CET), interface trap density (D_{it}), oxide charge, and the current density at a given bias voltage (J) can be extracted. In this section, a brief review of the electrical characterization techniques is given. Figure 9 shows the electrical probe station in the LEMD.

![Figure 9 Electrical characterization facility in LEMD](image-url)
2.4.1 C-V measuring models

![Small-signal equivalent circuit models of MIS capacitor](./small-signal.png)

Figure 10. Small-signal equivalent circuit models of MIS capacitor: 
(a) Accurate model (b) Series circuit model for low-leakage devices 
(c) Parallel circuit model for low series resistance devices.

The three-element circuit model of a MOS capacitor with leaky gate oxide is shown in Figure 10(a). The components of the equivalent circuit as described as follows:

- **C**: The actual frequency-independent device capacitance
- **\(R_p\)**: The effective device resistance due to leakage (tunneling) through the oxide
- **\(R_s\)**: The series resistance of the substrate and the gate.

From a single measurement of impedance phase and magnitude, however, only two of these three parameters may be ascertained.

For gate oxides thicker than 5 nm, the tunneling current is small and the device is dominated by series resistance. In this case, the device capacitance is measured by using the series circuit model in Figure 10(b).

C-V measurements of very thin oxides with large leakage currents are often performed using the parallel circuit model in Figure 10(c), which neglects series resistance. For our samples’ measurements, we use the parallel circuit model in Figure 10(c) since the dielectric layer is less than 5.0 nm.
From practical experience, we know that if the dielectric layer resistance \( R_{\text{ox}} \) and the corresponding electrode resistance \( R_{\text{elec}} \) ratio, \( R_{\text{ox}} / R_{\text{elec}} \geq 10^{-4} \), we can ignore \( R_s \) (including electrode resistance and other circuit resistance) during electrical measurements and use the parallel circuit model. Normally, the gate electrode resistivity should be \( \leq 10^{-5} \ \Omega \text{cm} \).

2.4.2 Resistivity measurement using 4-point probe method

![Figure 11. Schematic of 4-point probe configuration. Used with permission [29].](image)

The 4-point probe technique can be used to determine the resistivity of bulk samples and thin sheet samples with various formulas as described in the following section.

2.4.2.1 Bulk Sample

For bulk sample analysis, we assume that the metal tip is infinitesimal and samples are semi-infinite in lateral dimension. For bulk samples where the sample
thickness $t \gg s$, the probe spacing, we assume a spherical protrusion of current emanating from the outer probe tips. The differential resistance is:

$$\Delta R = \rho \left( \frac{dx}{A} \right)$$

We carry out the integration between the inner probe tips (where the voltage is measured):

$$\Delta R = \int_{x_i}^{x_f} \rho \frac{dx}{2\pi x^2} = \rho \left( \frac{1}{x} \right) \bigg|_{x_i}^{x_f} = \frac{1}{2s} \frac{\rho}{2\pi}$$

where the probe spacing is uniformly $s$. Due to the superposition of current at the outer two tips, $R = V/2I$. Thus, we arrive at the expression for bulk resistivity:

$$\rho = 2\pi \left( \frac{V}{I} \right)$$

2.4.2.2 Thin Sheet

For a very thin layer (thickness $t \ll s$), we get current rings instead of spheres. Therefore, the expression for the area $A$;

$$A = 2\pi xt$$

The derivation is as follows:

$$R = \int_{x_i}^{x_f} \rho \frac{dx}{2\pi xt} = \int_{s}^{2s} \rho \frac{dx}{2\pi x} = \rho \frac{\ln(x)}{2}\bigg|_{s}^{2s} = \frac{\rho}{2\pi} \ln 2$$

Consequently, for $R = V/2I$, the sheet resistivity for a thin sheet is:

$$\rho = \frac{\pi}{\ln 2} \left( \frac{V}{I} \right)$$
Note that this expression is independent of the probe spacing, $s$. Furthermore, this latter expression is frequently used for characterization of semiconductor layers, such as a diffused $n^+$ region in a p-type substrate. In general, the sheet resistivity

$$R_s = \frac{\rho}{t}$$

Can be expressed as:

$$R_s = k\frac{V}{I}$$

Where $k$ is a geometric factor. In the case of a semi-infinite thin sheet, $k = 4.53$, which is $\pi/\ln 2$ from the derivation. The factor $k$ will be different for non-ideal samples.

2.4.3 The minimum measurable capacitance of the Agilent 4294A Precision Impedance Analyzer

Figure 12 provides the measurement limits and associated errors for the Agilent 4294A Impedance analyzer.

First, we use the Four-terminal pair 2m (16048H) as the adapter. Every device is calibrated with this terminal adapter. The minimum measurable capacitance of this machine is $100\text{aF}$ ($100\times10^{-18}\text{F}$). When the frequency range is between 20MHz-110MHz, the uncertainty is larger than 10%. Table 4 lists the frequency range and errors at various capacitance values as taken from the chart in figure 12.
Table 4 Measuring Frequency range and associated errors for different capacitance values

<table>
<thead>
<tr>
<th>Capacitance value</th>
<th>Measuring Frequency</th>
<th>Partial Error possibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>1fF ($1\times10^{-15}$F)</td>
<td>2MHz – 110MHz</td>
<td>&gt;10%</td>
</tr>
<tr>
<td>10fF ($10\times10^{-15}$F)</td>
<td>200KHz – 110MHz</td>
<td>About 10% if measured at 1MHz or 10MHz, otherwise larger than 10%</td>
</tr>
<tr>
<td>100fF ($100\times10^{-15}$F)</td>
<td>20KHz – 110MHz</td>
<td>About 1%-3% if measured at 1MHz</td>
</tr>
<tr>
<td>1pF ($1\times10^{-12}$F)</td>
<td>2KHz – 110MHz</td>
<td>About 0.1%-0.3% if measured at 1MHz</td>
</tr>
</tbody>
</table>
Figure 12. Calculated impedance measurement accuracy at four-terminal pair port of the Agilent 4294A front panel (oscillator level=0.5 vrms). Used with permission.
2.4.4 Loading sample on probe station

![Probe station for sample loading](image)

Figure 13. Probe station for sample loading

2.4.4 Loading the sample on the probe station

Figure 13 shows the probe station. We load the sample on the wafer chuck of the probe station and turn on the mechanical pump which creates a vacuum between the wafer chuck and the backside of the sample to provide good physical contact. In order to eliminate vibrations, the mechanical pump is outside the room.

Once the sample is loaded, turn on the light and look through the microscope, bring the probe tip in close proximity with the capacitor electrode for which the measurement is to be taken. When the probe tip slides slightly on the electrode surface, the probe tip has contacted the electrode. At that time, stop the probe tip moving. The other probe tip is connected to the chuck. Then, switch off the light, and close the shielding box of the probe station to begin C-V and I-V measurements. Figure 14 shows the details of two probe tips connecting with the C-V and I-V instruments. (Instead of
being grounded, the chuck through the second probe tip is connected back to the measuring instrument by the triaxial cable, while the other tip touching the sample is directly connected back to the measuring instrument by the triaxial cable.)

2.4.5 C-V measurement and I-V measurement

Capacitance-voltage measurements were performed on MOS capacitors using an Agilent 4294A LCR meter. Prior to data acquisition, an open and/or short circuit correction was performed. The detailed procedures are described in Appendix A and B. The procedure for the sheet resistivity measurement is also described in Appendix C.

Figure 14. The details of two probe tips connecting with the C-V and I-V machines.
3. Results and discussion

3.1 Poly-SiGe results

Figures 15 and 16 show the XPS spectra of samples prepared for TEM. Since the SiGe layer is very thick (70nm), we cannot detect any photoelectrons generated from the bottom interface region between the HfSiON film and the Si substrate.

In the Ge 3d XPS spectrum (Figure 15), we cannot detect any Ge-O (33.2eV) peak. Features for elemental Ge 3d at 29 eV are clearly observed. This data suggest that there is no detectible Ge oxide near the sputtered SiGe layer’s surface, with a detection limit of about 1 atomic %.

![Ge 3d XPS spectrum of as-deposited SiGe film](image)

Figure 15. Ge 3d XPS spectrum of as-deposited SiGe film
In the Si 2p XPS spectrum, we cannot detect any Si-O (103.3 eV) peak. Features for elemental Si 3d at 99 eV are observed clearly. The data show no detectible Si oxide near the sputtered SiGe layer’s surface, with a detection limit of about 1 atomic %.

![Si 2p XPS spectrum of as-deposited SiGe film](image)

**Figure 16. Si 2p XPS spectrum of as-deposited SiGe film**

From RBS data (Figure 17(a)), we find that the average Ge composition in the poly-SiGe is about 25% as determined by spectra simulation with the software package SIMNRA 5.0. The very small oxygen peak also suggests that bulk oxygen in SiGe-layer is near the detection limit for RBS (a detection limit of ~0.1 atomic %), in agreement with the XPS results. Figure 17(b) indicates that the Hf energy edge is very close to the Ge energy edge for the poly-SiGe (13nm)/HfSiON+SiO₂ (2.5nm)/Si sample. So the Hf energy edge merging with the Ge energy edge is possible for the poly-SiGe (70nm)/HfSiON+SiO₂ (2.5nm)/Si sample.
Figure 17  

(a) Poly-SiGe (70nm)/HfSiON+SiO₂ (2.5nm)/Si

(b) Poly-SiGe (13nm)/HfSiON+SiO₂ (2.5nm)/Si
The TEM image (Figure 18) of an unannealed sample after SiGe sputter shows that the poly-SiGe and HfSiON films remain amorphous upon deposition.

![HRTEM image showing amorphous structures of SiGe, HfSiON, and SiO₂ films after sputter deposition](image)

Figure 18  HRTEM image shows the amorphous structures of SiGe (As deposited), HfSiON and SiO₂ films after sputter deposition

Figure 19 is a lower magnification HRTEM image of the sample shown in Figure 18. From Figure 19, we can clearly see the columnar structure associated with the sputtered SiGe layer. SiGe layer thickness is measured to be about 70nm. Also, the HfSiON film appears to be uniform over the region examined.
After rapid thermal annealing (RTA) 1050°C 120s (N₂ 740 torr), we observe that the poly-SiGe extensively intermixes with the HfSiON film (Figure 20).

![HRTEM image showing intermixing between SiGe layer and HfSiON/SiO₂ layer](image1)

Figure 19. HRTEM image shows the columnar structure of the SiGe layer after sputtering.

After rapid thermal annealing (RTA) 1050°C 120s (N₂ 740 torr), we observe that the poly-SiGe extensively intermixes with the HfSiON film (Figure 20).

![HRTEM image showing intermixing between SiGe layer and HfSiON/SiO₂ layer after 1050°C for 120s](image2)

Figure 20. HRTEM image shows intermixing between SiGe layer and HfSiON/SiO₂ layer after 1050°C for 120s
With decreasing RTA thermal budgets (1050°C 80s, 1050°C 60s, 1050°C 30s), the poly-SiGe does not penetrate uniformly into the Si substrate (Figures 21-26). It may be due to the non-uniform Ge distribution in the poly-SiGe or possibly non-uniformities in the HfSiON film developed locally during high temperature RTA thermal gudgets by reaction with poly-SiGe. In some areas, the HfSiON film and poly-SiGe also shows a stable interface (Figures 22, 24, 26). We note that as-deposited HfSiON films do not appear to exhibit non-uniformities, however.

Figure 21. HRTEM image shows SiGe layer does not uniformly penetrate into the substrate after 1050°C for 80s. Large SiGe grains caused by annealing also are visible.
Figure 22. HRTEM image shows the penetration area of the SiGe layer after 1050°C for 80s. (Higher magnification image of the sample is shown in Fig. 21) A stable SiGe area and HfSiON/SiO₂ area also are observed near the penetration area.

Figure 23. HRTEM image shows the penetration area of the SiGe layer after 1050°C for 60s. Stable SiGe area and HfSiON/SiO₂ area also are observed near the penetration area.
Figure 24. HRTEM image shows the stable SiGe and HfSiON/SiO₂ layer after 1050°C for 60s. (Figure 24 is higher magnification)

A stable HfSiON/SiO₂ film is observed clearly in this local area even though the penetration was observed in other areas (Shown in Fig. 23).

Figure 25. HRTEM image shows the penetration area between SiGe and HfSiON/SiO₂ layers after at 1050°C for 30s.
When the thermal budget is reduced to 1050°C 20s, the poly-SiGe/HfSiON/SiO₂/Si stack shows stability with no evidence of penetration with the substrate (Figures 27, 28). Combined with the TEM images of the RTA treatments discussed above, it appears that a thermal budget of 1050°C 20s is the maximum annealing condition for this HfSiON film composition. From Figure 28, we also see evidence for grain growth from the high temperature annealing, compared with as deposited sample shown in Figure 19.

Figure 26. HRTEM image shows both the stable SiGe and stable HfSiON/SiO₂ layers after 1050°C for 30s. (Figure 26 is higher magnification)
A stable HfSiON/SiO₂ film is observed clearly in this local area even though the penetration occurred in other areas (Shown in Fig. 25).
Figure 27. HRTEM image shows the stable SiGe and stable HfSiON/SiO$_2$ layers after 1050°C for 20s at a large scale (7.00 nm). No penetration is observed in the entire image. It implies that the maximum annealing condition is reached.

Figure 28. HRTEM image shows the stable SiGe and stable HfSiON/SiO$_2$ layers after 1050°C for 20s. A very large SiGe grain is observed.
With decreasing RTA thermal budgets (1050°C 10s, 1000°C 60s, 1000°C 30s, 1000°C 10s, 950°C 30s), the HfSiON film and poly-SiGe interface appears to be stable with no detectable penetration (Figs. 29-37). Comparing Figures 29 and 31, we also note that annealing the stack in high purity N₂ at 1000°C for 60s, the polycrystalline SiGe structure is changed from a columnar structure to a large grain structure. The impact of this structural change on electrical properties of the films was not investigated here.

Figure 29.  HRTEM image shows the SiGe and HfSiON/SiO₂ layers after 1050°C for 10s at a large scale (100.00 nm). Large SiGe grains are observed.
Figure 30. HRTEM image shows the stable SiGe and stable HfSiON/SiO₂ layers after 1050°C for 10s at a small scale (3.00 nm). (Figure 29 is lower magnification)

Figure 31. HRTEM image shows the SiGe and HfSiON/SiO₂ layers after 1000°C for 60s at a large scale (50.00 nm). Some large SiGe grains are observed.
Figure 32. HRTEM image shows a stable HfSiON/SiO$_2$ layer after 1000°C for 60s at a small scale (3.00 nm). (Lower magnification image of the sample shown in Fig. 31)

Figure 33. HRTEM image shows the SiGe and HfSiON/SiO$_2$ layers after 1000°C for 30s at a large scale (30.00 nm).
Figure 34. HRTEM image shows a stable HfSiON/SiO₂ layers after 1000°C for 30s at a small scale (7.00 nm). (Lower magnification image of the sample shown in Fig. 33)

Figure 35. HRTEM image shows the SiGe and HfSiON/SiO₂ layers after 1000°C for 10s.
Figure 36. HRTEM image shows the stable SiGe and stable HfSiON/SiO$_2$ layers after 1000°C for 10s. (Higher magnification image of the sample shown in Fig. 35) Some SiGe grains are observed in this figure.

Figure 37. HRTEM image shows the SiGe and HfSiON/SiO$_2$ layers after 950°C for 30s.
Based on our research results for the $\text{Hf}_{0.14}\text{Si}_{0.23}\text{O}_{0.46}\text{N}_{0.17}$ film, we found that for high thermal budgets (critical condition: RTA 1050°C 30s in high purity N₂ ambient), the poly-SiGe/HfSiON/SiO₂/Si stack is not stable and SiGe penetrates into the Si substrate. This may be due to the non-uniform Ge distribution in the poly-SiGe or possible non-uniformities in the HfSiON film.

The maximum allowable annealing condition for the HfSiON film investigated here is 1050°C 20s in high purity N₂ ambient. Results at lower thermal budgets confirm interfacial stability as detected by TEM. Lower temperature annealing (1000°C) for a longer time (60s) results in a polycrystalline SiGe structural change from a columnar structure to a large grain structure, but there is no SiGe penetration through the HfSiON/SiO₂ layer.

We note that, although localized nano-scale non-uniformities in the HfSiON layer due to the reaction with poly-SiGe at higher thermal budget may be present, the presence of large scale stable regions for annealing conditions of $T \leq 1000 \, ^\circ\text{C}$ suggests that non-uniformity is not as issue.

3.2 Ru deposition results

3.2.1 Shadow mask effects on Ru electrode dots

The Ru sample position relative to the shadow mask affects the metal dot pattern integrity. Figure 38 shows that if Ru atoms are deposited some distance (about 3 cm) from the wafer center, line of sight deposition can happen along the dot edge, resulting in a diffuse appearance and an error in the estimation of the dot area. It is important to have the edge as close to the mask as possible.
3.2.2 Optical Images of Ru dot depositions

The optical images of the deposited dots confirm this point. We prepared two Ru samples and the samples’ positions relative to a 4 inch wafer are shown in Figure 39. Sample 1 is in the center of the Si wafer and sample 2 is to the edge of the Si wafer. Figures 40 and 41 show sample 1 has a sharper edge on the dots than does sample 2.
Figure 39. Ru sample positions on the wafer

Figure 40. Ru dots (Sample1)
The image shows sharper edges of dots and no connection between different dots.

Figure 41. Ru dots (Sample2)
The image shows diffuse edges of dots and some dots are connected to each other.
3.2.3 Sheet resistance of Ru sample electrode before and after N₂ annealing

The sheet resistance of Ru samples 1 and 2 described above were measured by the 4294A Precision Impedance Analyzer (probe distance is about 2-3 mm)

The two samples were prepared by sputtering.

Before N₂ annealing

Both sample 1 and sample 2 get a Ru sheet resistance of about 10-20 ohms.

After N₂ annealing:

For sample 1:

After 450 °C 8 torr N₂ ambient annealing for 30 mins:

Sheet resistance: $10^6$ ohms or Mega ohms

The Ru surface becomes very hard and a little dark.

For sample 2:

After 450 °C 8 torr N₂ ambient annealing for 30 mins:

Ru resistance: 20-30 ohms

The sheet resistance didn’t change after annealing.

3.2.3 C-V results of sample 1 and sample 2

For sample 1:

We could not get C-V curves due to the high Ru sheet resistance.
For sample 2:

As the measurement frequency increases from 400Hz to 1MHz (Fig. 42, 43, 44, 45), the accumulation side of the C-V curve becomes flatter and closer to the ideal shape due to lower leakage current at higher frequency. It is reasonable since, when the measurement frequency becomes higher, the reaction time for the defects in the film to the applied voltage becomes shorter and less defects can be activated. A drop in the accumulation capacitance is attributed to the activated defects.

From the curves’ shape, we at least know the sputtering method for Ru as a metal gate is feasible. The N₂ annealing or temperatures used in this study may be not suitable for Ru samples from the sheet resistance measurement results.

Figure 42.  C-V curve at 400Hz
At the accumulation side, the capacitance drops due to high leakage current.

Figure 43.  C-V curve at 1kHz
At the accumulation side, the capacitance drops due to high leakage current and down degree is almost the same as 400Hz measurement.
Figure 44. C-V curve at 10KHz
At the accumulation side, the capacitance drops down a little less than curves at 400Hz and 1KHz. But the inversion side also begins to drop down.

Figure 45. C-V curve at 1MHz
At the accumulation side, the capacitance drops down a little less than curves at 400Hz 1KHz and 10 KHz. The inversion side also does not change much.
4. Conclusion

4.1 Conclusion for SiGe study

We found that for high thermal budgets (Critical condition: RTA 1050°C 30s in high purity N₂ ambient), for Hf₀.₁₄Si₀.₂₃O₀.₄₆N₀.₁₇ film, the poly-SiGe/HfSiON/ SiO₂/Si stack is not stable and SiGe penetrated into the Si substrate.

The maximum annealing condition for the HfSiON film investigated here is 1050°C 20s in high purity N₂ ambient. Results at lower thermal budgets confirm interfacial stability as detected by TEM. We also note that work by M. A. Quevedo-Lopez, et al.³² found that 1050°C, 60s RTA can cause boron penetration through similar HfSiON film from SIMS studies.

Lower temperature annealing (1000°C) for a longer time (60s) results in a polycrystalline SiGe structural change from a columnar structure to a large grain structure, but there is no SiGe penetration through the HfSiON/SiO₂ layer.

4.2 Conclusion for Ru study

Pure Ru metal does not appear to be a good choice for the gate material since it is hard to etch off, and different annealing conditions can cause large changes of electrical behavior.
5 Recommendations for future research

5.1 For poly-SiGe gate

If we want to continue to alleviate depletion problems, Si$_3$N$_4$ is another choice. Several technologies have been proposed to suppress boron penetration. Thermally nitrided oxide or reoxidized nitrided oxide in NO, N$_2$O, or NH$_3$ ambient can act as a diffusion barrier for boron.$^{33,34,35,36}$

However, a higher thermal budget is required for nitrided oxide, which is not desirable for future CMOS process. The nitridation in NH$_3$ was reported to introduce a large number of interface traps$^{37}$ and fixed oxide charges.$^{38}$ Direct nitrogen implantation into the gate material is a new technology featuring process simplicity.$^{39,40}$ However, the impact of gate nitrogen implant on the overall behavior of CMOS transistors is not quite well understood. Amorphous silicon ($\alpha$-Si) has been proposed as an alternative gate material to suppress boron penetration.$^{41,42}$ Yet no direct comparison has been made in terms of the MOS transistor performance among different gate microstructures.

5.2 For Ru gate

RuTa or RuO$_2$ look more attractive than Ru metal gates.

The use of binary alloys of Ru and Ta offers work function-tuning opportunities that can provide both NMOS and PMOS compatible work functions, no gate depletion and good MOSFET characteristics. The materials are promising candidates for sub-50nm CMOS devices.$^{43}$
Thin films of transition conducting metal oxides, such as RuO$_2$ and IrO$_2$ are attractive gate electrodes since they have large work functions (~5 eV), low resistivity and excellent thermal stability.

H. Zhong, et al.$^{44}$ have demonstrated that RuO$_2$ gates on ZrO$_2$ and Zr silicate provide good thermal stability resulting in minimal change of $V_{fb}$ and equivalent oxide thickness. The behavior of RuO$_2$ gates was attributed to its excellent oxygen diffusion barrier properties and its low Gibbs energy of formation compared to ZrO$_2$. This prevents oxygen loss from the dielectric thereby maintaining its electrical performance.
Appendix A. C-V measuring procedure

Figure 46 shows the Agilent 4294A Precision Impedance Analyzer for C-V measurement. Turn on the Agilent 4294A (Precision Impedance Analyzer), and the Keithley 7002 Switch system, and allow to warm up for 30~45 minutes.

1. Use the Keithley 7002 Switch system to direct the signal line to the 4294A:

2. Press “recall” first, and press “111” and “Enter” key On the Keithley 7002 Switch system:

3. Under INSTRUMENT STATE, press “Preset” key

4. Under MEASUREMENT, press “Meas” key and choose “Cp-D” (parallel Capacitance – dielectric loss) model

5. Under MEASUREMENT:

6. Press “Display” key and choose “Split on” to display capacitance-voltage curves and dielectric loss as two separate plots
7. If multiple frequency C-V curves need to be displayed on the same plot, then choose “Accumulate ON”

8. Under STIMULUS, press “Sweep” key and set “Parameter” as “DC bias”. Press “time”, set “sweep time” at “20 sec” and “sweep delay” time at “3 sec”.

9. Press “Bw/Avg” key under MEASUREMENT, Bandwidth: set at 2

10. For OSC voltage setup, total principle (Choose “source” menu under STIMULUS), press “level”: Choose a OSC voltage value to let the CV curve looks smoothly. For a thick film, we usually set OSC voltage at 500mv. For a thin film, we usually set OSC voltage at 50mv ~ 200mv. Enter 100 and then press k/m key under ENTRY.

11. Under STIMULUS, press “Source” key and choose “Bias menu”.

12. Measurement range: 100 mA

13. Begin to test: set “Start” and “Stop” values for voltage range; make sure the range is decent for typical CV curve.

14. Press “Source” and “Bias menu”, and set “DC bias” on.

15. Press “Source”, and type in appropriate values of frequency. Example: For 100 kHz, type in 100 after pressing “Source”, and then press the “k/m” key under ENTRY. For 1 MHz, type in 1 after pressing “Source”, and then press the “M/ ” key under ENTRY.

16. If the C-V curve is beyond the range of the Y-axis scale, then choose “Scale Ref” key under MEASUREMENT, and then press “Auto scale” to rescale the C-V curve.

17. If error message “DC Bias overload” appears, then alter “start” and “stop” values of voltage. Also check if the measurement range is set correctly (100mA), or if the value for the AC (oscillation) voltage level is correct.
18. To get hysteresis loop, press “Sweep”, and change “Direction” from “Up” to “down” or vice versa.

19. Save results to floppy disk drive. Press “Save” key and choose “Data” and “ASCII”.

   After that, type file name (maximum 8 characters) and press “Enter”.

20. Before switching to I/V measurement, switch DC bias off – press “Source” under STIMULUS, go to “Bias menu”, and change option to “off”.
Appendix B. I-V measuring procedure

Figure 47 shows the Agilent 4156B Semiconductor Parameter Analyzer for I-V measurement. Turn on 4156B, and the Keithley 7002 Switch system, and allow to warm up for ~ 45 minutes.

1. Use the Keithley 7002 Switch system to direct the signal line to the 4156B: Press “recall” first, and press “222” and “Enter” key.

2. Calibrate first. Press “system” key and choose “CALIB/DIAG” and “DIAG SELFTST ALL”. Wait for 5 mins.

3. Press “Meas” key. Press two times “PREV PAGE” and set model as “Sweep”.

4. Keep the first column unchanged, and set “MODE” as “V” and “FCTN” as “VAR1” for the second column, delete the left four columns.
Table 5 I-V measuring parameters setup

<table>
<thead>
<tr>
<th>unit</th>
<th>Vna me</th>
<th>ina me</th>
<th>mo de</th>
<th>fctn Stb</th>
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</thead>
<tbody>
<tr>
<td>SMU1: HR</td>
<td>V1</td>
<td>I1</td>
<td>I</td>
<td>CON</td>
</tr>
<tr>
<td>SMU2: HR</td>
<td>V2</td>
<td>I2</td>
<td>V</td>
<td>VAR1</td>
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<tr>
<td>SMU3: HR</td>
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<tr>
<td>SMU4: HR</td>
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<tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VMU2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5. Press “next” key 2 times, and set the same DC range with the I-V test as for the C-V measurement. Sweeping steps should be 201. Example:
Table 6 I-V measuring control parameters setup

<table>
<thead>
<tr>
<th>Var1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
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</tr>
<tr>
<td>Name</td>
<td>V2</td>
</tr>
<tr>
<td>Sweep mode</td>
<td>Single</td>
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<td>Lin/log</td>
<td>Linear</td>
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<tr>
<td>Start</td>
<td>0 V</td>
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<tr>
<td>Stop</td>
<td>2.5 V</td>
</tr>
<tr>
<td>step</td>
<td>12.5 mV</td>
</tr>
<tr>
<td>No. of step</td>
<td>201</td>
</tr>
<tr>
<td>Compliance</td>
<td>100 mA</td>
</tr>
<tr>
<td>Power comp</td>
<td>off</td>
</tr>
</tbody>
</table>

6. Set the sweep delay time as 0.001s and press “Graph/List” key

7. Begin to test: Under HIGH VOLTAGE, press “Single” key and see the first time sweep curve. If you want to save many repeat curves, press “Append” for the next sweep to verify reproducibility of the result
8. Finally, when ready to save the I-V curve, press “Single” key.

9. Press “Graph/List” and choose “SPREAD SHEET”. Make sure you have already inserted a diskette in the floppy disk driver.

10. After that, type file name and press “Enter” on the keyboard, and ‘Execute’ button on 4156B to save file in the floppy disk drive.
Appendix C. Determining the sheet resistivity by 4-point probe

Turn on the voltmeter, set the mode to DC and voltage range to 200 mV.

1. Place wafer onto the probe stage.

2. Flip the toggle switch located atop the probe station from "NEUTRAL" TO "DOWN".

3. Watch the probe casing lower until the probes stabilize on the wafer.

4. Return the toggle switch of the probe station to the "NEUTRAL" position.

5. Turn on the current source by turning the black switch "S1" to the "ON" position.

6. Set the current to the desired level, and proceed with measuring the voltage across the inner two probes. Map the wafer.

7. When measurement is finished, shut off the current source by turning the switch "S1" to the "OFF" position.

8. Flip the probe station toggle switch from "NEUTRAL" to "UP".

9. Wait until the probe casing is all the way up, then set the toggle switch back to "NEUTRAL".

10. Turn off voltmeter.
References


28 Kevin J. Yang, Capacitance Measurement and Analysis Techniques for High-Leakage Dielectrics, Report for the degree of Master of Science, Plan II., May 2000

29 James Chan, Four-Point Probe Manual, EECS at UC-Berkeley, Spring 1994

30 Agilent 4294A Precision Impedance Analyzer Data Sheet, pp.18

31 Matej Mayer, a Microsoft Windows program for the simulation of backscattering spectra for ion beam analysis with MeV ions, more details: http://www.rzg.mpg.de/~mam/


