AN OPTIMIZED CONTROL SYSTEM FOR THE INDEPENDENT CONTROL OF THE INPUTS OF DOHERTY POWER AMPLIFIER

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This thesis presents an optimized drive signal control system for a 2.5 GHz Doherty power amplifier (PA). The designed system enables independent control of the amplitudes and phases of the drive signals fed to the inputs of two parallel PAs. This control system is demonstrated here for Doherty PA architecture with a combiner network which is used as an impedance inversion between the path of two parallel connected PAs. Independent control of the inputs is achieved by incorporating a variable attenuator (VA) and a variable phase shifter (VPS) in each of the two parallel paths. Integrating VA and VPS allows driving varying power levels with an arbitrary phase difference between the individual parallel PAs. A Combiner network consists of a quarter-wave transmission line at the output of the main power amplifier, which is used to invert the impedance between the main and peaking transistor. The specific VA (Qorvo QPC6614) and VPS (Qorvo QPC2108) components that are used for the test system provide an amplitude attenuation range from 0.5 dB to 31.5 dB with a step size of 0.5 dB and a phase range from 0◦ to 360◦ for a step size of 5.6◦at the intended operating frequency of 2.5 GHz, offering the benefit of characterizing the behavior of PAs under test for an extensive range of drive signals to optimize the output performance such as power added efficiency (PAE) or adjacent channel leakage ratio (ACLR). For demonstration, the designed drive signal control system is integrated with two parallel GaN transistor-based PAs (Qorvo QPD0005) with

a P1dB of 37.7 dBm. Each PA is preceded by a drive amplifier with a gain of 17.8 dB to boost the power fed into the PA. The control system incorporates various custom-designed components such as a 20 dB directional coupler, a 3 dB Wilkinson power splitter, a quarter-wave transmission line, and a Doherty power combiner. While Qorvo QPD0005 (DUT) is used as a specific test case in this demonstration, the proposed system can characterize the behavior of a wide range of Doherty PAs.

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CHAPTER 1

INTRODUCTION

As modern wireless communication systems evolve to handle an increased data rates, the power amplifier performance is very crucial and to meet the signal's high data capacity for many different real-time applications, enhancement of the efficiency at power back-off is important. Modern wireless communication systems require power amplifiers to maintain a high efficiency over various output power levels. However, it is hard to satisfy such required maximum output power with significant gain and a high P_{1dB} compression point with just a single power amplifier. To overcome these drawbacks, a linear high-efficiency power amplifier, i.e., the Doherty power amplifier, can be designed, developed, and implemented to improve the overall power system performance [**3**]. The load modulated DPA has always been proven for its high drain efficiency for the range of back-off saturated output power, with high efficiency and good linearity for just a simple structure which makes it possible to implement in base stations, satellites, etc. DPA contains two individual amplifiers and a combiner with a quarter-wave transmission line at the input of either amplifier, which provides the impedance inversion between the two parallel-connected amplifiers. The main amplifier operates as a conventional Class AB amplifier to maintain the linearity at the output [**4**, **5**]. The peak amplifier operates as a Class C amplifier, which turns ON when the main amplifier reaches saturation [**6**]. The peak amplifier helps maximize the output power with the maintained constant drain voltage of the main amplifier. Now, to characterize and optimize the DPA in a repeatable and predictable way , a sophisticated PA control system needs to be established [**7**–**11**]. Components such as phase shifters and Variable Attenuators along with directional couplers, power splitters, drive amplifiers are utilized for developing such control system circuitry [**12**, **13**]. Implementing a Variable Attenuator and a phase shifter at the input of the amplifier gives the benefit of varying input amplitude and delay of the signal. Moreover, it helps obtain a wide range of control characterization for PAs to obtain the best performance. Prior works suggest that over a wide range of output power

levels, DPAs have achieved a remarkable efficiency. Past works used, analog and digital control system for regulating the inputs of DPA were fabricated on one single PCB, which restrict the use of control system for the other amplifiers [**14**–**16**]. Moreover, previous approaches show that either the control system was integrated before the power divider or two different RF generator were used for the inputs of parallel branch instead of using a power divider, which limits the control range or increase the chance of error for mismatch between two signals, respectively. Compared to other efficiency enhancement strategies, here our designed control system has the novelty of controlling any power amplifier using a singe RF generator to obtain optimized performance. For the Doherty implementation, a PA of exceptionally high output power of 37.7 dBm corresponds to a 1-dB gain compression point with a maximum drain efficiency of 72.9% is used. However, even though there are several control systems or input power distribution systems that are proposed in prior work to achieve linearity and enhance the PAE, the proposed architectures are complex [**14**, **17**, **18**]. Therefore, there is still a need to design an optimized drive signal control system that to simple to implement without involving complex circuitry and can be used for any parallel combination of power amplifiers.

In this thesis, simple to implement optimized drive signal control system for DPA is presented at 2.5 GHz. The control system has been designed by integrating an optimized 20 dB directional coupler [**19**,**20**], a 3 dB power splitter [**14**,**21**–**23**], quarter-wave transmission line [**24**], Doherty power Combiner, and commercially available components such as GaN power amplifier [**25**, **26**], drive amplifier [**27**, **28**], Variable Attenuator, and phase shifter [**29**–**31**].

The thesis is organized as follows: Chapter 2 presents the system architecture of the designed and implemented optimized signal control system, with detailed discussion of passive and active components used in the system. Chapter 3 presents results and discussion of the individual components used in the control system and optimized configuration. Chapter 4 consists of the concluding remarks and future works.

1.1. Thesis Organisation

This thesis is organized as follows. Chapter 1 discusses the overview of the designed control system and the contribution of this work to solve the problem statement.

Chapter 2 discusses the design architecture of the control system for the independent controls of inputs of a parallel-connected power amplifier which includes the design of the DUT, i.e., different ways of the parallel combination of power amplifiers.

Chapter 3 discusses the final results of the different approaches used and compared the simulated and measured S-parameters of the designed components and architecture.

Finally, the comparison and the conclusion are presented in Chapter 4.

CHAPTER 2

SYSTEM ARCHITECTURE

The designed system is divided into three (3) sections: a designed control system, parallel combination of power amplifiers and instrument clusters (Outputs). As mentioned above, two parallel combinations of power amplifiers are used to plot the performance using the designed control system [**32**, **33**]. First parallel combination PA is the Doherty power

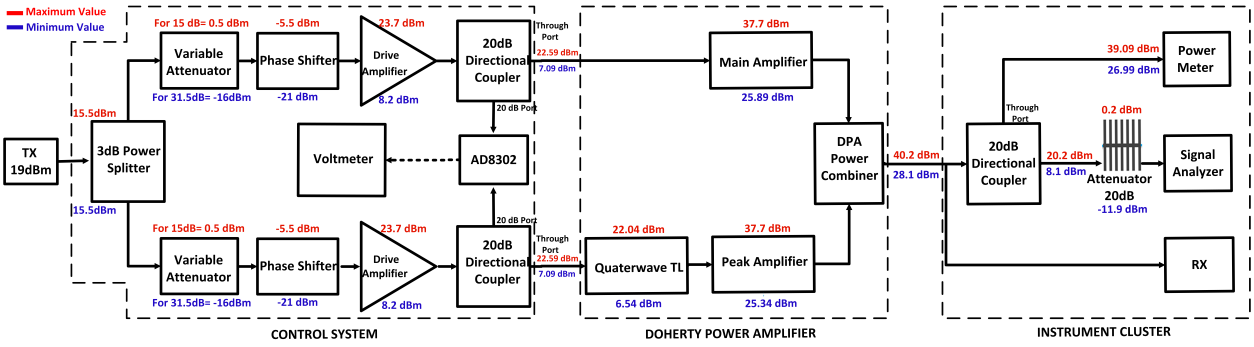

FIGURE 2.1. Block diagram of optimized drive signal control system for DPA.

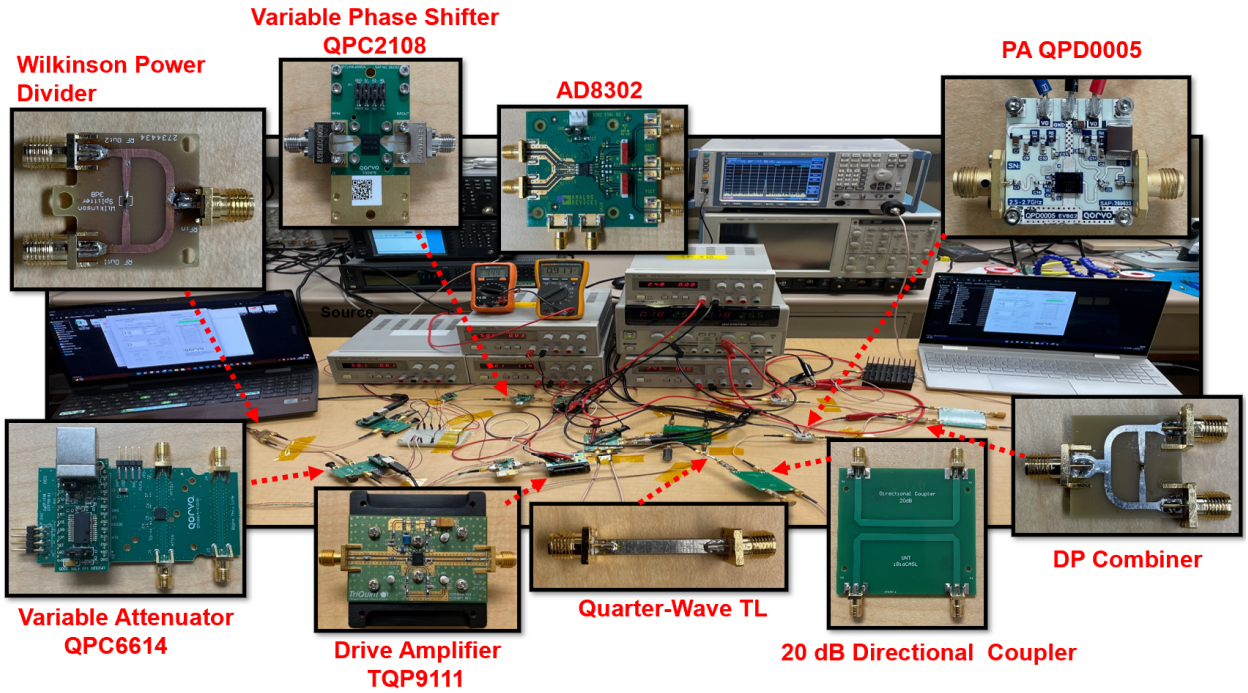

FIGURE 2.2. Control system for Doherty power amplifier.

amplifier, which consists of two parallel-connected amplifiers operating with a fixed phase difference of 90° between their inputs, and their outputs are combined using the Doherty power combiner as shown Fig. 2.1 and its corresponding test setup with component used is shown in Fig. 2.2. Moreover, second parallel combination PA is the combination of the simple parallel-connected power amplifier operating in the same phase and class of operation, with their outputs combined using a 3 dB Wilkinson power combiner. To independently control the inputs of both the amplifiers for both the DUTs, a control system is implemented which controls the amplitude and phase of each input to obtain the optimized performance to characterize the DUT. Independent amplitude control is achieved by integrating a variable attenuator in each branch and then the each outputs of VA is independently phase controlled by cascading a VPS. Now, the output section involves the measuring instruments connected to the output of the DUT to measure the important parameters to draw the characteristics. Based on the DUT, the link budget analysis is performed for the operating frequency of 2.5 GHz. After integrating the control system with DPA, obtained estimated theoretical output is 28.1 dBm for maximum attenuation of 31.5 dB and for the minimum attenuation of 15 dB, the output is 40.2 dBm. The suitable Variable attenuator, variable phase shifter, and drive amplifier were chosen based on the link budget analysis as shown in Table 2.1 and their model/manufacturer are given in Table 2.2. The power splitter, power combiner, and directional coupler were fabricated on an FR4 substrate with a dielectric constant, $\varepsilon_r = 4.3$, which are incorporated into the overall control system by performing a thorough link budget analysis. The design and fabrication of the 3 dB Wilkinson power splitter, Doherty Power combiner, and 20 dB directional coupler are described in this Section later.

The optimized drive signal control system consists of a custom-designed 3 dB Wilkinson power divider, and two of each variable attenuator (QORVO QPC6614), variable phase shifter (Qorvo QPC2108), drive amplifier (Qorvo TQP9109), custom-designed 20 dB directional coupler, as shown in Fig. 2.1. For a combined DPA architecture, nuanced differences in amplitude and phase needs to be set in order to ensure the optimal output parameter. Typically, this is achieved with manual adjustment of trace lines or with surface mount com-

ponent changes. This is a time-consuming task and may lead to degradation of the circuit board that may compromise the final performance achieved. However, this control system enables independent control of the amplitudes and phases of the drive signals fed to the inputs of the two parallel amplifiers used as a DPA architecture. Incorporating a variable attenuator (VA) and a variable phase shifter (VPS) in each of the two parallel paths allows for driving uneven power levels with an arbitrary phase difference to the individual amplifiers, offering the benefit of characterizing the behavior of DPA, which is under test for an extensive range of drive signals to optimize the output performance such as power added efficiency, P_{1dB} compression point, maximum output power, stability, gain, and adjacent channel leakage ratio (ACLR).

TABLE 2.1. Link budget analysis - Doherty power amplifier

Component	**Link budget analysis**		
	Specifications	**Minimum Output (dBm)**	***Maximum output (dBm)***
3dB Power Splitter	Insertion Loss= 0.5 dB	15.5	15.5
attenuator (QPC6614)	P0.1dB = +30 dBm	-16	0.5
Phase Shifter (QPC2108)	P1dB= 29 dBm, Insertion Loss= 5 dB	-21	-5.5
Drive Amplifier (TQP9111)	O/P P1dB= +32.5 dBm, Gain= 29.2 dB	8.2	23.7
Power Amplifier (QPD0005)	O/P P1dB= +37.7 dBm, I/P P1dB= +24 dBm, Gain= 18.8dB	25.89	37.7
DP Combiner	Insertion Loss= 0.52 dB	28.1	40.2
20 dB Directional Coupler	Insertion Loss= 0.08 dB	8.1	20.2

TABLE 2.2. Components used in the optimized drive signal control system

Component	**Model and Manufacturer**	
	Model number	***Manufacturer***
3dB Wilkinson power splitter	Custom (Designed and Fabricated)	Custom-designed
Variable Attenuator	QPC6614	Qorvo Inc.
Variable phase shifter	QPC2108	Qorvo Inc.
Drive amplifier	TQP9111	Qorvo Inc.
20 dB directional coupler	Custom (Designed and Fabricated)	Custom-designed
Power amplifier	QPD0005	Qorvo Inc.
3dB power combiner	Custom (Designed and Fabricated)	Custom-designed
Fixed attenuator	25-Watt, Product ID: PE7393-20	Pasternack
RF Gain and phase detector	MN EVAL – AD8302	Analog Devices

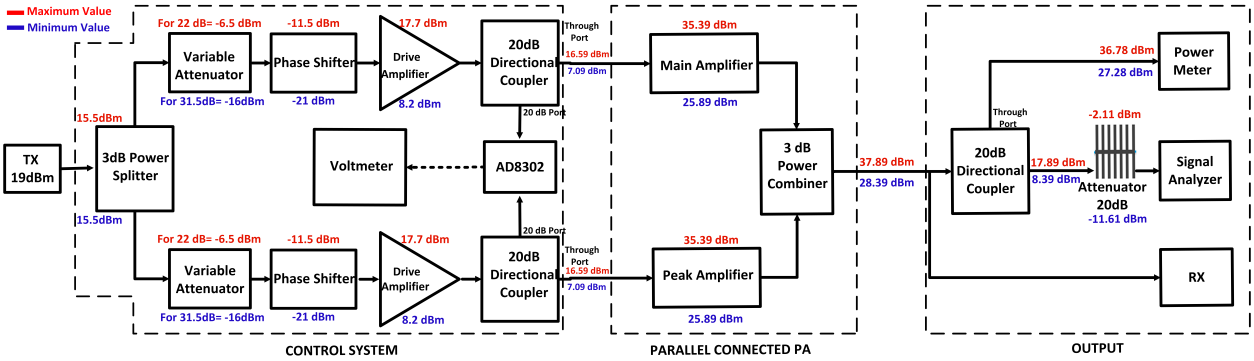

FIGURE 2.3. Block diagram of optimized drive signal control system for parallel connected PA.

The designed control system is also tested by implementing it for simple parallel-connected power amplifiers, which is presented in Fig.2.3 and corresponding, link-budget analysis is shown in Table 2.3.

TABLE 2.3. Link budget analysis - Parallel connected amplifier

Component	Link budget analysis		
	Specifications	**Minimum Output (dBm)**	***Maximum output (dBm)***
3dB Power Splitter	Insertion Loss= 0.5 dB	15.5	15.5
Variable Attenuator (QPC6614)	P0.1dB = +30 dBm	-16	-6.5
Phase Shifter (QPC2108)	P1dB= 29 dBm, Insertion Loss= 5 dB	-21	-11.5
Drive Amplifier (TQP9111)	O/P P1dB= +32.5 dBm, Gain= 29.2 dB	8.2	17.7
Power Amplifier (QPD0005)	O/P P1dB= +37.7 dBm, I/P P1dB= +24 dBm, Gain= 18.8dB	25.89	35.39
DP Combiner	Insertion Loss= 0.52 dB	28.39	37.89
20 dB Directional Coupler	Insertion Loss= 0.08 dB	8.39	17.89

2.1. Passive Devices

The optimized drive signal control system consists of a custom-designed 3 dB Wilkinson power divider, and two of each variable attenuator(QPC6614), variable phase shifter (QPC2108), drive amplifier (TQP9109), custom-designed 20 dB directional coupler, as shown in Fig. 2.1. For a combined DPA architecture, nuanced differences in amplitude and phase needs to be set to ensure the optimal parameter performance. Typically, this is done at RF frequencies with manual adjustment of trace lines or with surface mount component changes. This is a time-consuming task and may lead to degradation of the circuit board

that may compromise the final performance achieved. However, this control system enables independent control of the amplitudes and phases of the drive signals fed to the inputs of two parallel amplifiers used as a DPA architecture. Incorporating a variable attenuator(VAS) and a variable phase shifter (VPS) in each of the two parallel paths allows for driving uneven power levels with an arbitrary phase difference to the individual amplifiers, offering the benefit of characterizing the behavior of DPA is under test for an extensive range of drive signals to optimize the output performance such as power added efficiency, $P_{1\,dB}$ compression point, maximum output power, stability, gain, and adjacent channel leakage ratio.

2.1.1. 3 dB Wilkinson Power Divider[1]

The Wilkinson power divider is one of the essential building blocks for driver control circuitry. Instead of using two different RF generators for the parallel branch, this 2:1 Wilkinson power divider is used, which eliminates the chance of amplitude and phase mismatch, which may arise due to difference between signals generated by two different generators. The 3 dB power divider is designed using Keysight's Advanced Design System (ADS) design automation software. The substrate material chosen for this design is FR-4 with a thickness of 1.2 mm, and copper with a thickness of 0.08 mm is chosen as conductor material due to its high conductivity. In addition, the shunt resistor has been incorporated into the design to absorb reflective power, thus reducing the insertion loss. The power ratio design technique calculates the shunt resistance value along with the width and length of the transmission lines. The technique for calculating the line impedance and shunt resistance for the Wilkinson power splitter is as follows: As the 3 dB Wilkinson power divider splits the power into two halves, so, the value of $K = \sqrt{2}$, and the power division ratio of $1{:}K^2$ is as follows:

$$Z_{01} = Z_0 \times \sqrt{K \times (1 + K^2)} \tag{2.1}$$

[1]Section 2.1.1 is reproduced from Pallav Sah, Karthik Kakaraparty, Matthew Poulton, Hung Luyen, and Ifana Mahbub, "Prototype for an Optimized Drive Signal Control System for a 2.5 GHz Doherty Power Amplifier," 2022 IEEE Texas Symposium on Wireless Microwave Circuits and Systems (TSWMCS), pp. 1-4, with permission from IEEE.

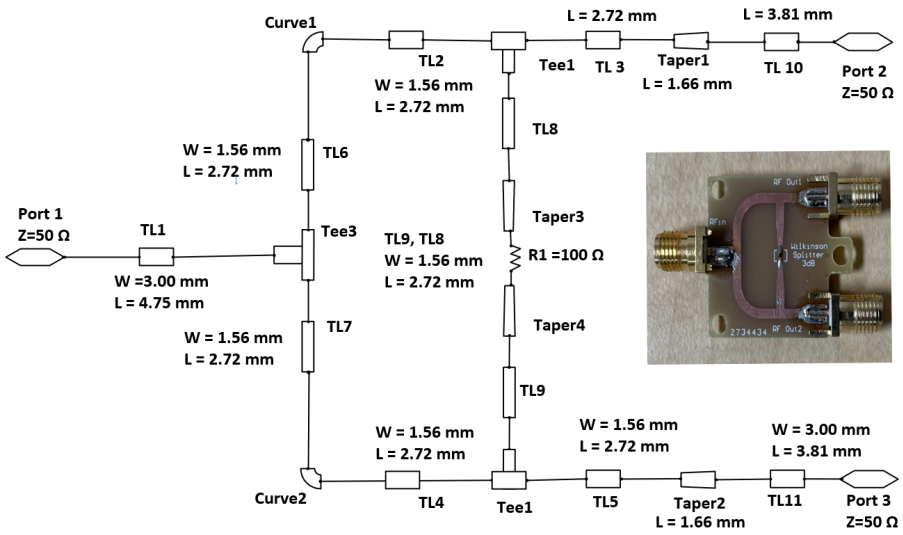

FIGURE 2.4. Schematic and fabricated design of Wilkinson power splitter.

$$Z_{02} = Z_0 \times \sqrt{(\frac{1+K^2}{K^3})} \tag{2.2}$$

$$Z_{02} = Z_0 \times \sqrt{K} \tag{2.3}$$

$$Z_{04} = \frac{Z_0}{\sqrt{K}} \tag{2.4}$$

Using the above formulas, values of line impedance and shunt resistance are obtained. The final optimized values of impedance and shunt resistance are as follows: $Z_0 = 50\Omega$, 70.71 Ω value for Z_{01}, Z_{02}, Z_{03} and Z_{04} and $R_1 = 100\Omega$. The optimized length for each microstrip line is selected by tuning and making the electrical length equal to 25°. The microstrip line–based circuit (Schematic) is shown in Fig. 2.4. The circuit is simulated for the obtained impedances with their corresponding width and length at 2.5 GHz are given in Table 2.4.

2.1.2. Variable Attenuator

To achieve a wide range of inputs for the parallel-connected power amplifiers, a variable attenuator is employed in each branch of the inputs of the amplifiers. Variable attenuators are used to achieve a wide range of outputs for a given input signal, which is accomplished by attenuating the input signal. The considered VA is a commercially available component (QPC6614) by Qorvo Inc., shown in Fig 2.5.

TABLE 2.4. Design parameters

Microstrip Type	Parameters		
	Impedance (Ω)	**Width (mm)**	**Length/ Radius (mm)**
TL1	50	3.00	4.75
TL10, TL11	50	3.00	3.81
TL2, TL3, TL4, TL5	70.71	1.56	2.72
TL6, TL7, TL8, TL9	70.71	1.56	2.72
Taper1, Taper2	-	-	1.66
Taper3, Taper4	-	-	5.03
Curve1, Curve2	-	3.00	4.57

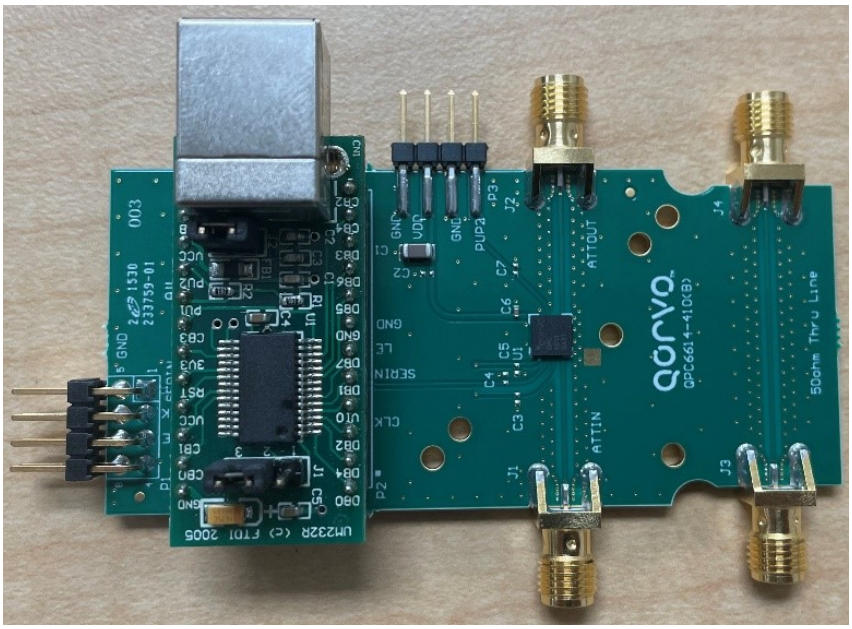

FIGURE 2.5. Variable attenuator.

Used VA is a 6-bit digital step variable attenuator that can provide a maximum attenuation of 31.5 dB, which enables a wide range of inputs with a high linearity. Moreover, the VA is easy to control, as it can be either controlled by programming it for different attenuation using a computer connected through USB type-B, or it can also be controlled by an external bus according to the attenuation word truth table as shown in Table 2.5.

Different attenuation ranges are selected based on the link-budget analysis for both the DUTs of the parallel combination of amplifiers. For the DUT - Doherty power amplifier,

TABLE 2.5. Attenuation word truth table

Attenuation Word						
D5 (MSB)	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**	**Attenuation State**
H	H	H	H	H	H	0 dB Ref. Insertion Loss
H	H	H	H	H	L	0.5 dB
H	H	H	H	L	H	1 dB
H	H	H	L	H	H	2 dB
H	H	L	H	H	H	4 dB
H	L	H	H	H	H	8 dB
L	H	H	H	H	H	16 dB
L	L	L	L	L	L	31.5 dB

the theoretical attenuation range is from 15 dB to 31.5 dB, whereas for DUT - parallel-connected amplifiers, the obtained range is from 22 dB to 31.5 dB. Long range of attenuation for DPA is because of the introduction of quarter-wave transmission at the input of peak amplifier, which introduce a insertion loss. Using this attenuation range, a wide range of inputs of amplifiers are obtained with the step size of 0.5 dB. The variable attenuator has tolerance of a 1.4 dB with an input $P_{0.1dB}$ of +30 dBm.

2.1.3. Variable Phase Shifter

Maintaining the purity of the phase and amplitude is a very challenging task, even when the outputs of the two parallel-connected amplifiers must be combined. To obtain a higher efficiency for the linear output, both output signals of the amplifiers should be combined with the correct phase. Thus, to control the delays of the output signal, the control system is equipped with two-phase shifters in both of the parallel branches following the VA. The variable phase shifter enables the control of the delays of each amplifier input signal generated by VA, which in turn helps to combine the outputs with the correct phase for achieving a higher efficiency. The phase shifters (Qorvo QPC2108), used in the control system is shown in Fig. 2.6. The phase shifter has a 360° degree coverage and offers an exceptional RMS phase error of $< 2.8°$ and an amplitude error of <0.4 dB over the entire operating frequency range of 2.5 to 4 GHz.

FIGURE 2.6. Variable phase shifter.

It is a 6 – bit variable digital phase shifter that can provide the maximum phase shifting of 360° with an LSB of 5.625° for an input P_{1dB} of 23 dBm. VPS is controlled by the binary switching, for different phase shifts by applying 0/+5V at control switch, following the bias truth table as shown in Table 2.6.

TABLE 2.6. Bias Truth Table

Bit Control							
Phase Shifter	5°	11°	22°	45°	90°	180°	**REF**
0° **(REF)**	0	0	0	0	0	0	1
5°	1	0	0	0	0	0	1
11°	0	1	0	0	0	0	1
22°	0	0	1	0	0	0	1
45°	0	0	0	1	0	0	1
90°	0	0	0	0	1	0	1
180°	0	0	0	0	0	1	1
180°	1	1	1	1	1	1	1

2.1.4. 20 dB Directional Coupler[2]

In the realization of the parallel combination of the amplifiers, the power signal measurements is the biggest challenge. Moreover, to characterize the parallel combination of amplifiers, the inputs and outputs power levels need to be determined using a signal analyzer and power meter. Since, the system operates at a high power level, to analyze the signals of high-power strength, expensive instruments with high-power handling capability are required. To avoid the expenditure, as shown in Fig. 2.7 a directional coupler with a coupling factor, $C = 20$ is designed, which allows for maintaining a thorough connection in the circuit using Port 1 and Port 2, where the measuring instruments can be connected through Port 4, which 20 dB coupled port.

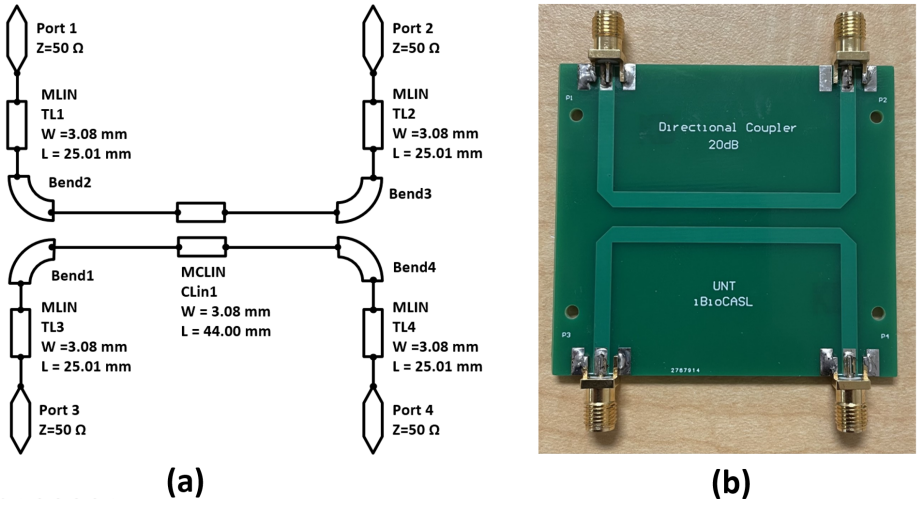

FIGURE 2.7. 20 dB directional coupler (a) Schematic (b) Fabricated design.

The designed 20 dB Directional coupler has four ports, where all four ports are approximately matched to 50Ω and show a minimum return loss. The directional coupler's Port 1 is used as the input, Port 2 as through/direct port, Port 3 as the isolation port, and Port 4 as the coupled port. Ideally, signal goes into Port 1, appears as is at the Port 2, which is the through port, and is received at Port 4 with a coupling of 20dB, and there is no signal

[2]Section 2.1.1 is reproduced from Pallav Sah, Karthik Kakaraparty, Matthew Poulton, Hung Luyen, and Ifana Mahbub, "Prototype for an Optimized Drive Signal Control System for a 2.5 GHz Doherty Power Amplifier," 2022 IEEE Texas Symposium on Wireless Microwave Circuits and Systems (TSWMCS), pp. 1-4, with permission from IEEE.

at Port 3. The coupler is realized using microstrip coupled line and microstrip lines, with the coupling factor of $C = 20$. To obtain the dimensions of microstrip coupled lines, its even and odd impedances need to be calculated for a specified coupling factor. The even impedance (Z_{oe}) and odd impedance (Z_{oo}) values are calculated using the following formulas:

$$Z_{oe} = Z_0 \times \sqrt{\frac{C+1}{C-1}} \tag{2.5}$$

$$Z_{oo} = Z_0 \times \sqrt{\frac{C-1}{C+1}} \tag{2.6}$$

To calculate the width and length of the microstrip coupled line, we used the Keysight's Advanced Design System (ADS)-Linecalc tool at 2.5 GHz for the calculated Z_{oe} and Z_{oo} equals to 52.56Ω and 47.56Ω and obtained $W = 3.08mm$, $S = 3.67mm$, and $L = 44.00mm$ for microstrip coupled line and the terminal impedance of Z_o equal to 50Ω.

2.1.5. Quarter-wave Transmission Line ($\lambda/4$)

In the DPA, the main amplifier operates in Class AB mode, and the peaking amplifier operates in Class C mode. At high input power, the main amplifier reaches the state of saturation, and at that time, both the amplifiers become active to deliver power to the load. The quarter-wavelength transmission ($\lambda/4$) line of characteristic impedance Z_0= 50Ω are chosen that both the amplifiers provide the maximum power and efficiency by maintaining their optimum load impedance. The quarter-wavelength ($\lambda/4$) transmission line at the input of the peaking amplifier provides a delay of the 90° to ensure the proper combination of outputs of the two parallel-connected amplifiers at the combining node. This quarter-wavelength ($\lambda/4$) transmission line with a characteristic impedance Z_0= 50 Ω is designed and implemented using FR4 of thickness 2.2 mm, which is shown in Fig. 2.8.

At the output of the main amplifier, a quarter-wavelength transformer recombines the output signal of the main and the peaking amplifier. From this combining node of both the PAs, the impedance is approximately half of that 50 Ω system impedance. Thus,

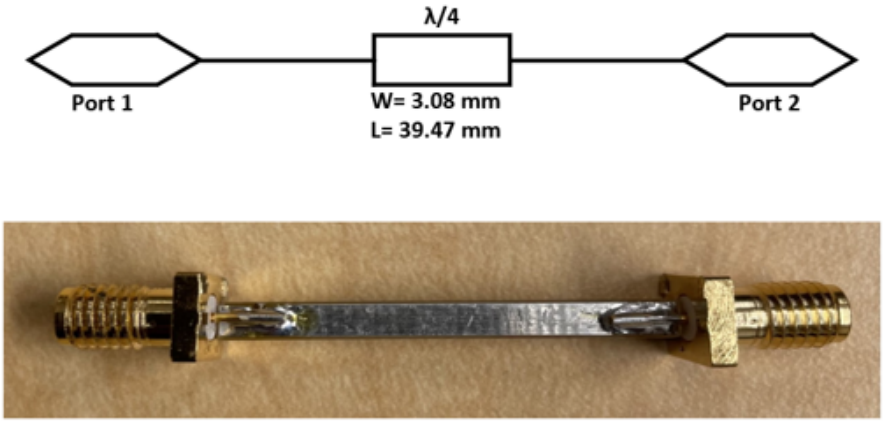

FIGURE 2.8. Quarter-wave transmission line.

a quarter-wavelength transformer is employed to convert the modulated impedance to the system impedance, ensuring the maximum power transfer to the load is satisfied.

2.1.6. Doherty Power Combiner

For the Doherty power amplifier, the outputs of the main amplifier biased in Class AB operation and peak amplifier biased in Class C operation have to be combined. So, an output combining network called Doherty Power Combiner is designed using transmission lines in ADS. This designed combiner combines the outputs of the two parallel amplifiers operating in two different classes of operation. The combining network consists of a tuning circuit to bias the peak amplifier in Class C operation. At the output of the main amplifier, a quarter-wave transmission line is employed to make the phase of both the outputs equal at the recombination node, as shown in Fig. 2.9. The impedance of the transmission lines is obtained using the load matching formula (given below) for a different case.

$$Z_0 = \sqrt{Z_{in} \times Z_l} \tag{2.7}$$

Fig. 2.9(a) presents the initial case in which only the main amplifier is operating in Class-AB operation and peak amplifier act as a open circuit with infinite impedance, whereas Fig. 2.9(b) presents the impedances when the main amplifier saturates and the peak amplifier starts conducting at high input power and sharing equal loads.

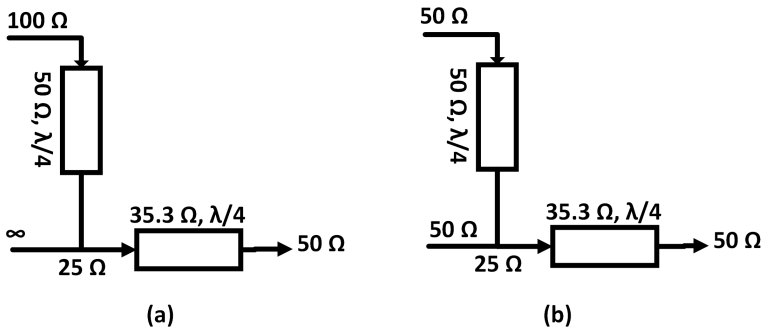

FIGURE 2.9. Combining node.

The Doherty power combiner is designed and simulated using Keysight's Advanced Design System (ADS). The substrate material considered is FR-4 with a thickness of 1.2 mm, and copper with a thickness of 0.2 mm is chosen as the conductor material due to its high conductivity. The microstrip line-based circuit (Schematic) is shown in Fig. 2.10.

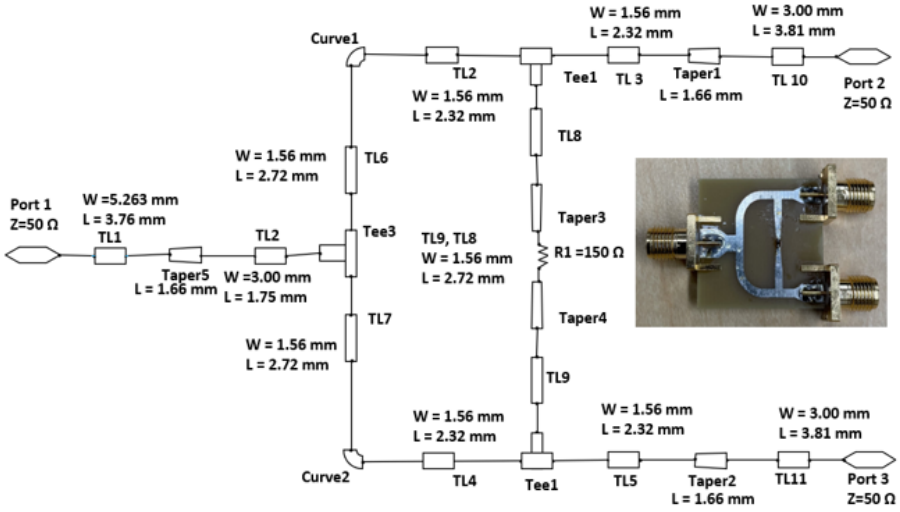

FIGURE 2.10. Schematic and fabricated design of Doherty power combiner.

2.2. Active Devices

2.2.1. Drive Amplifier

Before feeding power to the amplifiers directly through the RF signal generator, the signal is passed via a control system which includes a power divider and then a VA and VPS for each branch. The presence of a power divider, VA, and VPS, which all are connected

through RF cables, causes attenuation and insertion loss and reduces the input signal's power amplitude for power amplifiers. To compensate this loss, the input to the amplifier is boosted by implementing a drive amplifier before the main and the peak amplifier. The drive amplifier (Qorvo TQP9111), as shown in Fig. 2.11 is used as it is designed to boost its input signal with a high gain of 29.2 dB at 2.5 GHz with a P_{1dB} compression point of 32.5 dBm, which enables high linearity to drive and provide the maximum input to the power amplifier.

FIGURE 2.11. Drive amplifier.

2.2.2. Power Amplifier (QPD0005)

The power amplifier used to implement Doherty and parallel connected amplifier structure is a commercial component, Qorvo QPD0005 as shown in Fig. 2.12. It is a Gallium Nitride (GaN) based power amplifier which is used for its increased power density, reliability and gain in reduced size. Due to its reduced size and increased efficiency, this technology is employed in defense, aerospace and much more complex applications like phased arrays, radar, base transceivers for 5G [**34**–**36**]. The QPD0005 operates in the frequency range from 2.5 to 5 GHz with a drain voltage equal to 48 V. It provides the gain of 18.8 dB for the input and output 1 dB compression point of 24 dBm and 37.7 dBm, respectively.

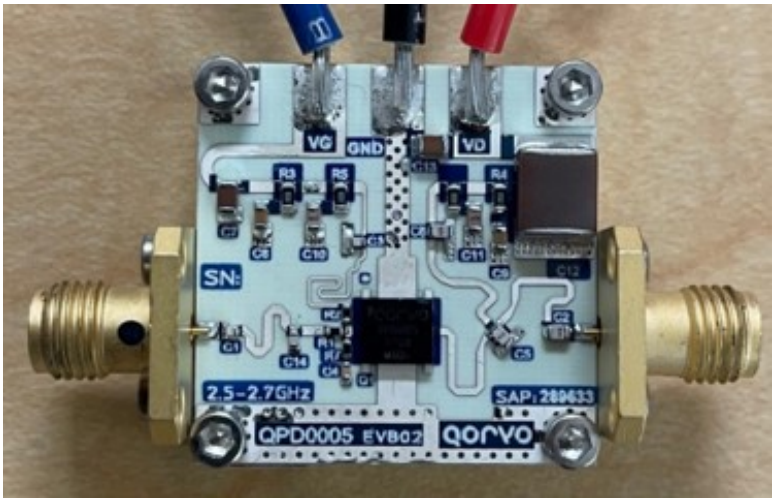

FIGURE 2.12. Power amplifier - QPD0005.

2.3. Class of Operation

Efficiency is defined as the ratio of the Radio Frequency (RF) power to the Direct Current (DC) power. Power is the capability of delivering a voltage or current to the amplifier's load at the frequency of interest. The conduction angle is considered 100 percent when the device is always on, and the waveforms are not distorted. To a lesser degree, the biasing and matching networks provided to the amplifier also help define the operation class the amplifier performs [**1**]. Here the class of operations for amplifier are summarized in Table 2.7 and discussed below:

TABLE 2.7. Summary of amplifier class of operations

Class of Operations				
Class	**Efficiency**	**Power**	**Linearity**	**Conduction Angle**
A	25 % Max.	High	Best	100 %
AB	$<$ 68 %	High	Some Distortion	$<$ 100 %
B	78.5 % Max.	High	More Distortion	50 %
C	$>$ 78.5 %	Low	Poor	$<$ 50 %

2.3.1. Class A

Amplifiers are biased in Class A operation conduct for the whole waveform period, even when there is minimal or no signal. This means the class A amplifier always operates at

full power whether there is an input signal present or not. This reduces the efficiency of the amplifiers operating class A to 25 %. Because when there is no input, the amplifier is ON and converts all the power into heat, which is not only a waste of energy but also increases the operating costs. Class A amplifiers are inherently the most linear form of amplifier.

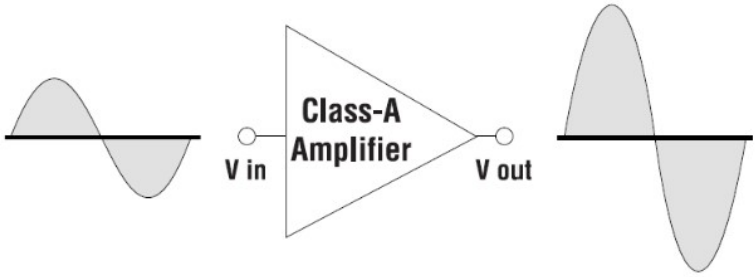

FIGURE 2.13. Linear operation of class A amplifier [**1**].

2.3.2. Class B

When an amplifier is biased for Class B operation, the conduction angle for the drain or source current becomes equal to 50 %. This can be seen in Fig. 2.14 where the amplifier is conducting only for half, and the other half is OFF. That means the DC supply is reduced to half or $2/\Pi$ compared to the Class A operation, increasing the efficiency to 78.5 %. To achieve the class B operation, the amplifier is biased so that only signal current is used to ON the amplifier keeping the DC bias current almost equal to zero. So, when the signal voltage falls below a definite level, the collector current becomes equal to zero, and the amplifier is turned-off. This will also introduce more amplified signal distortion than the Class A operation.

2.3.3. Class AB

Class AB biased amplifiers operate in between Class A and Class B operation of the region. An amplifier like class B operates for only half a period in class AB operation, but it conducts for the other half with a small amount of current. To bias the amplifier in Class AB operation, non-zero DC is applied, whose magnitude is decided according to achieving linearity, efficiency, and power. This biasing voltage determines the conduction angle of the

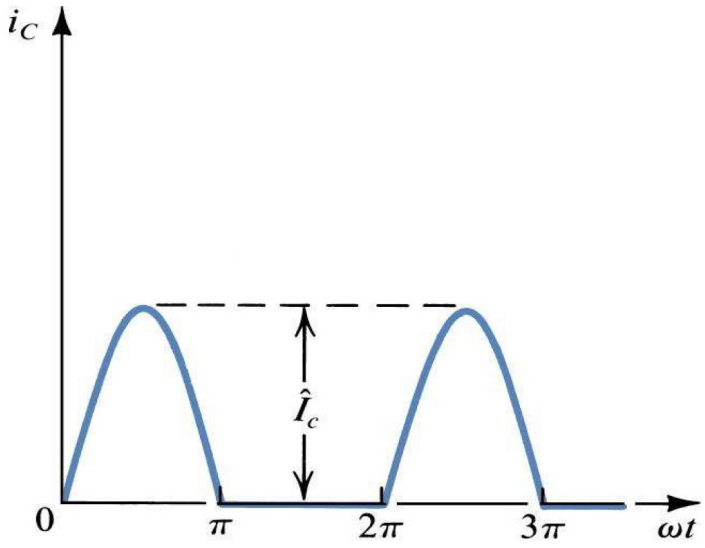

FIGURE 2.14. Collector Current Waveform for Class-B Operation [**1**].

amplifier, as shown in Fig. 2.15. Because of the reduction in total current over the period increases the efficiency to 68 %.

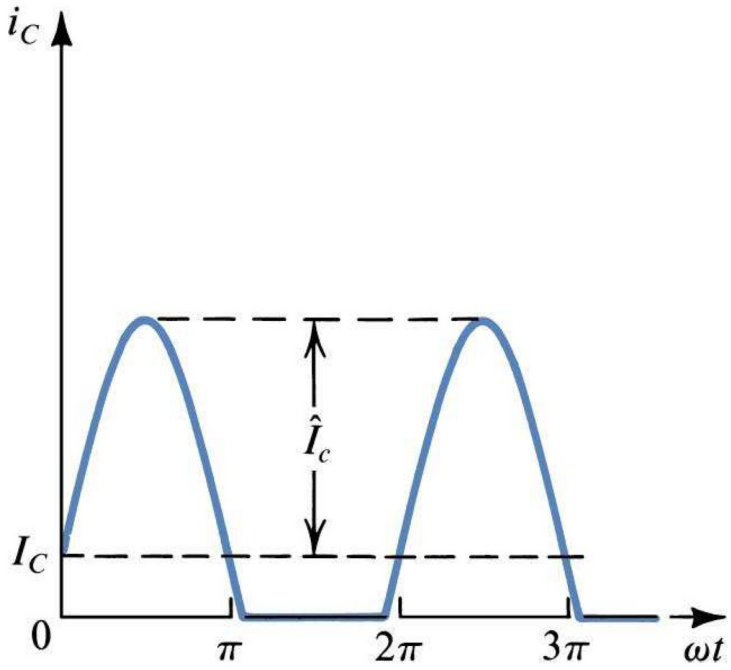

FIGURE 2.15. Collector current waveform for class-AB operation [**1**].

2.3.4. Class C

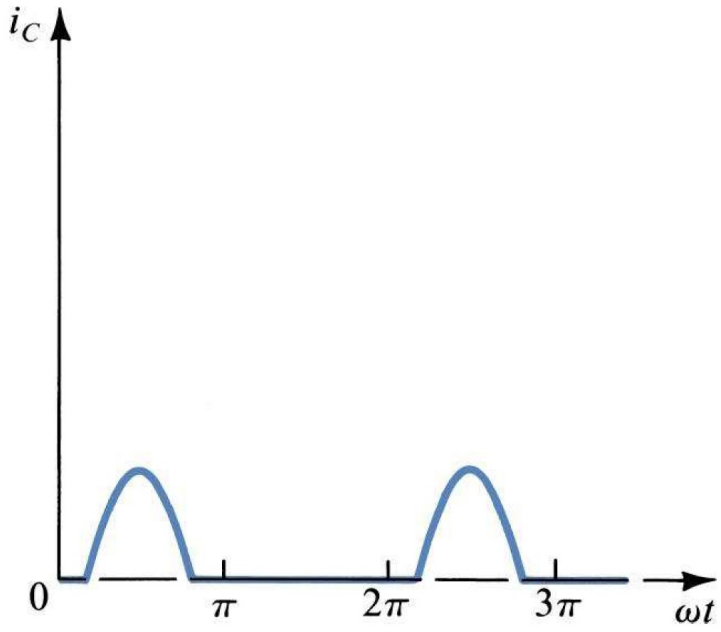

FIGURE 2.16. Collector current waveform for class-C operation [**1**].

To bias the amplifier in Class C operation, a tuned circuit as a load is used for the intended frequency, which causes high distortion. So, a Class C biased amplifier conducts less than half a cycle, enabling high efficiency. For Class C operation, the amplifier is biased in the OFF region. Therefore, when the signal is applied, the signal's peak makes the amplifier conduct only for a short period. Generally, the conduction angle for the amplifier is less than 180°, as shown in Fig. 2.16.

2.4. Characteristic Parameters

2.4.1. Power Added Efficiency (PAE)

Power Added Efficiency is the amplifier's efficiency in converting the lower RF power signal to a high power level using the DC power at a given frequency. The formula for PAE is given below:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{dc}} \tag{2.8}$$

While comparing the efficiency of the amplifiers, the PAE is a most compared figure of merit. Where drain efficiency of the power amplifier is the measure of DC power converted to RF power during amplification. The drawback of the drain efficiency is that it does not consider the input RF power.

2.4.2. Maximum Output Power

When the amplifier reaches the state of saturation for a specific input, the corresponding determined output power is the maximum output power. At this stage, the amplifier's efficiency is highest, and the output voltage is severely clipped, as shown in Fig. 2.17. The shown graph will show how the waveform may look compared to the saturated condition.

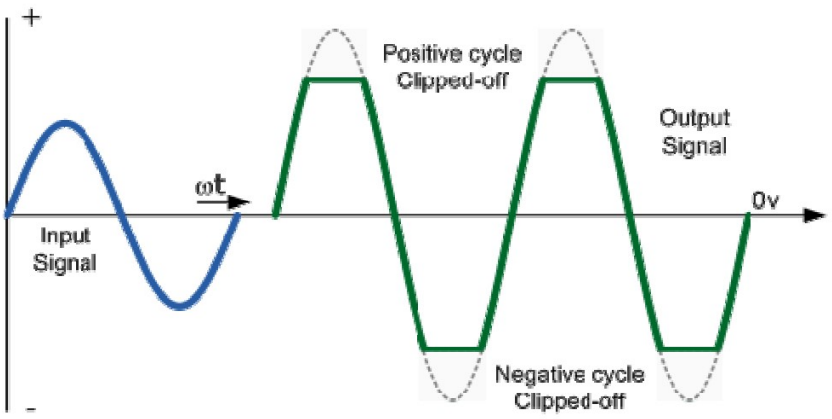

FIGURE 2.17. Ideal waveform compared to compressed amplifier output [**1**].

2.4.3. Input Amplitude and Phase Difference

The input and output must be determined to characterize the power amplifier to obtain the optimized performance. As discussed, this is an RF circuit; the measuring instruments cannot be connected directly to the circuit. To connect the measuring instruments, the 20 dB directional couplers are used. The main aim of the performed test is to identify the input amplitude and phase difference for which the maximum output and higher efficiency are achieved. A gain and phase detector (Adapter AD8302) shown in Fig. 2.18 is connected

at the input of the power amplifier via a 20 dB directional coupler as shown in the block diagram.

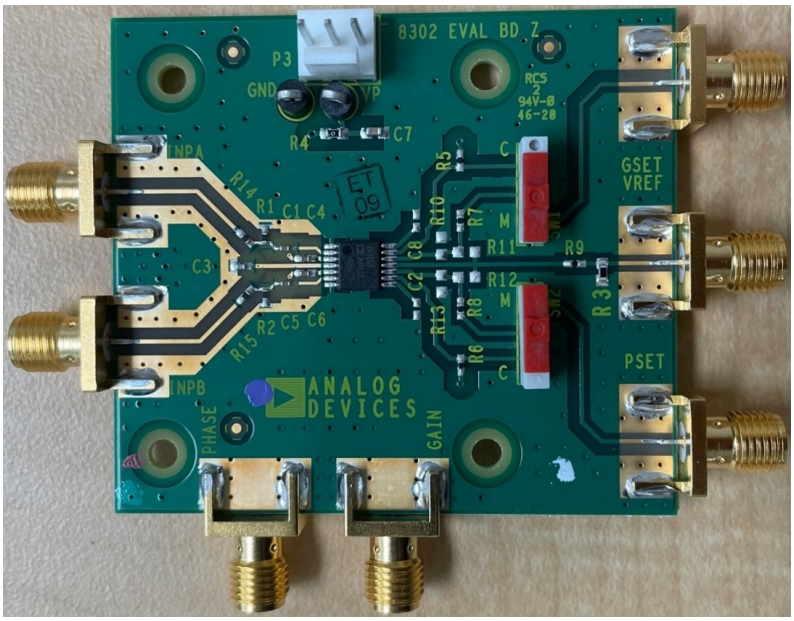

FIGURE 2.18. Gain and Phase Detector - AD8302.

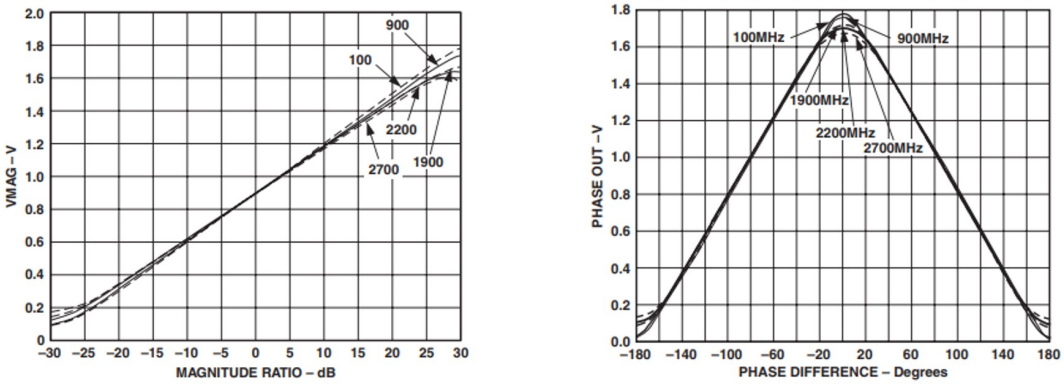

FIGURE 2.19. (a) DC voltage vs. Gain ratio and (b) DC voltage vs. Phase difference [**2**].

The used adapter AD8302 processes the main and peak amplifier RF input into DC voltage, then using the determined DC voltage, the corresponding input gain ratio, and phase differences are obtained with the help of the graph shown in Fig. 2.19 provided by the manufacturer.

CHAPTER 3

MEASUREMENTS RESULTS

The research aims to design an optimized control system for the independent control of the inputs of the parallel combined power amplifiers to determine the optimum input gain power ratio and phase difference for achieving the highest efficiency. The Wilkinson power divider, VA, VPS, and drive amplifier; all these instruments play a vital role in controlling the amplifier's input signal to achieve the highest efficiency at the maximum output power. The designed control system is used for two different case scenarios, first for the Doherty power amplifier and second for the simple parallel-connected power amplifiers operating in the Class AB operation. The results for all the designed and fabricated components for the control system, including the power amplifiers, are presented in this section.

3.1. Wilkinson Power Divider

A Wilkinson power divider is designed to divide the total input power into two parallel branches. This Wilkinson power divider divided the total input power for the control system into two equal half to feed the main and peak amplifier via other control instruments. Instead of using a power divider, two different RF generators can also be used, but the error of mismatch between two signals may arise.

S-parameters of the designed and fabricated Wilkinson power divider using FR4 dielectric substrate of constant 4.3 and thickness 1.2 mm are shown in Fig. 3.1 and Fig. 3.2.

It can be seen in Fig. 3.1 that the measured return losses for all the ports are improved, but the measured insertion loss at Port 2 and Port 3 is increased by 7.14 % in Fig. 3.2. The comparison for the simulated and measured s-parameters is shown in table 3.1 for 2.5 GHz. The difference in the simulated and measured values may be because of the real constraints during fabrication and testing.

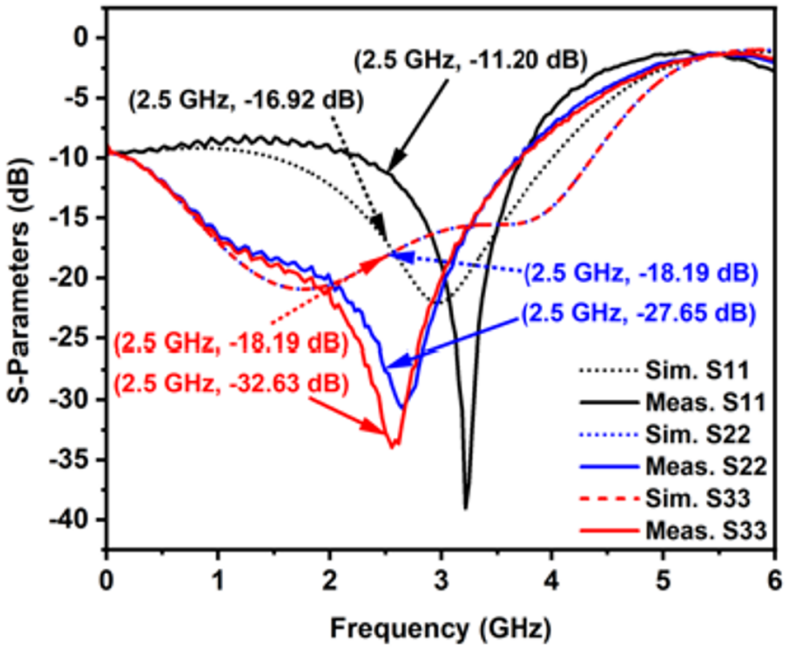

FIGURE 3.1. Wilkinson power divider - Return loss.

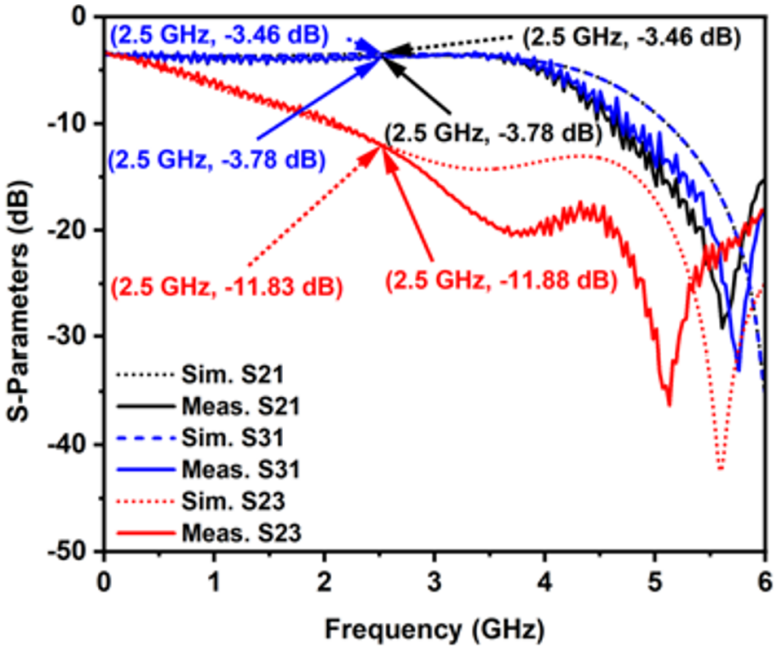

FIGURE 3.2. Wilkinson power divider - Insertion loss.

3.2. Variable Phase Shifter

Variable phase shifter plays a vital role in the control system, which is employed in each branch to control the delay of the input signals of the amplifier. By controlling the

TABLE 3.1. S-parameters for Wilkinson power divider

Comparison		
S-parameters	**Simulated (dB)**	**Measured (dB)**
S(1,1)	-16.92	-11.20
S(2,2)	-18.19	-27.65
S(3,3)	-18.19	-32.63
S(2,1)	-3.457	-3.78
S(3,1)	-3.457	-3.78
S(2,3)	-11.83	-11.88

delays of the input signals, inturns controlling the output signal helps combining the output with the correct phase for higher efficiency. Used VPS is a 6-bit variable digital phase shifter that gives the coverage from 5° to 360°. The different phase shifts achieved and errors at 2.5 GHz are shown in Table 3.2 and Fig. 3.3. The S-parameters are also obtained for the used VPS; the insertion loss is 4.4 dB at 2.5 GHz as shown in Fig. 3.4.

TABLE 3.2. VPS - Phase shift and errors

Given Phase Shift (Degrees)	**Achieved Phase Shift (Degrees)**	**Phase Shift To Be Achieved (Degrees)**	**Error (%)**
0	70.22 (Reference)	70.22 (Reference)	0
5	76.44	75.22	1.62
11	80.96	81.22	0.32
22	91.10	92.22	1.21
45	114.22	115.22	0.86
90	157.61	160.22	1.62
180	-110.49	-109.78	0.64
355	67.32	65.22	3.21

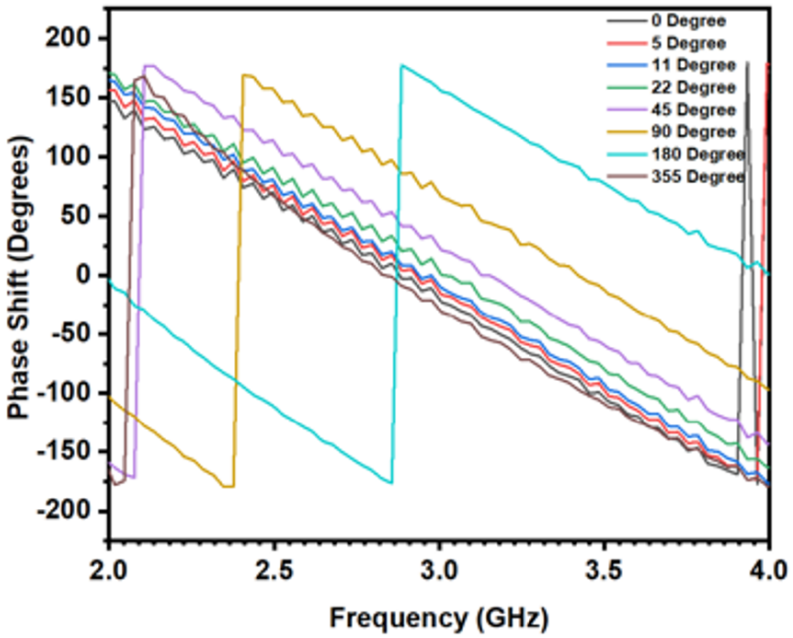

FIGURE 3.3. Variable phase shifter - Phase shift achieved.

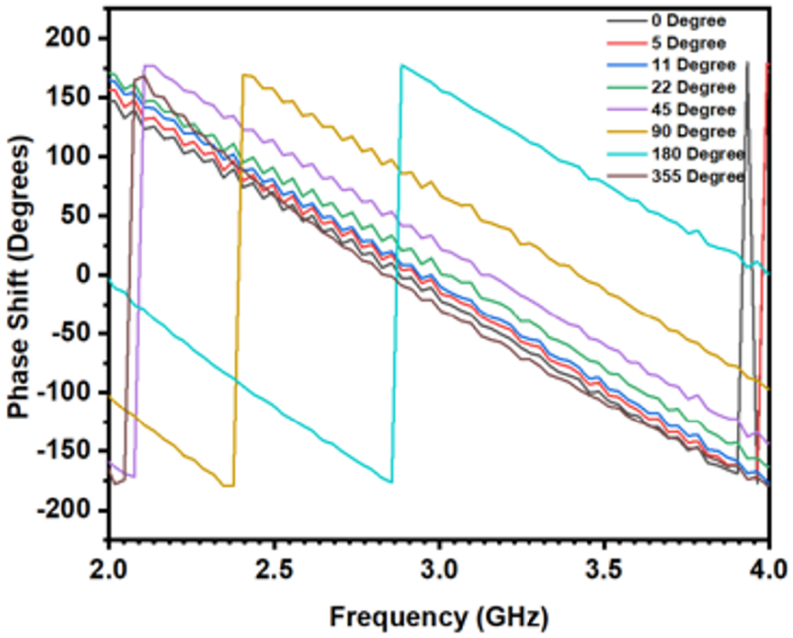

FIGURE 3.4. Variable phase shifter - S-parameters.

3.3. Drive Amplifier

As discussed above, the input signals must be boosted after passing through the power divider, VA, VPS, and RF cables as the input signal is attenuated due to their insertion loss.

The drive amplifier (Qorvo TQP9111) used in this work, which boosts the signal by 25.32 dB (S21) at 2.5 GHz to the input of the power amplifiers, as s-parameters are shown in Fig. 3.5. Obtained return loss for S11 and S22 are -14.6 dB and -10.02 dB, respectively. The highest PAE achieved for the drive amplifier during the test is 23.2% at a maximum output of 30.55 dBm for an input of 10 dBm, is calculated using Eqn.3.1 as shown in Fig. 3.6. The actual gain, which is 28.8 dB is 13.74% greater than the measured value, which is compared in Table 3.3.

$$PAE = 100 \times \frac{RF_{Pout} - RF_{Pin}}{P_{dc}} \tag{3.1}$$

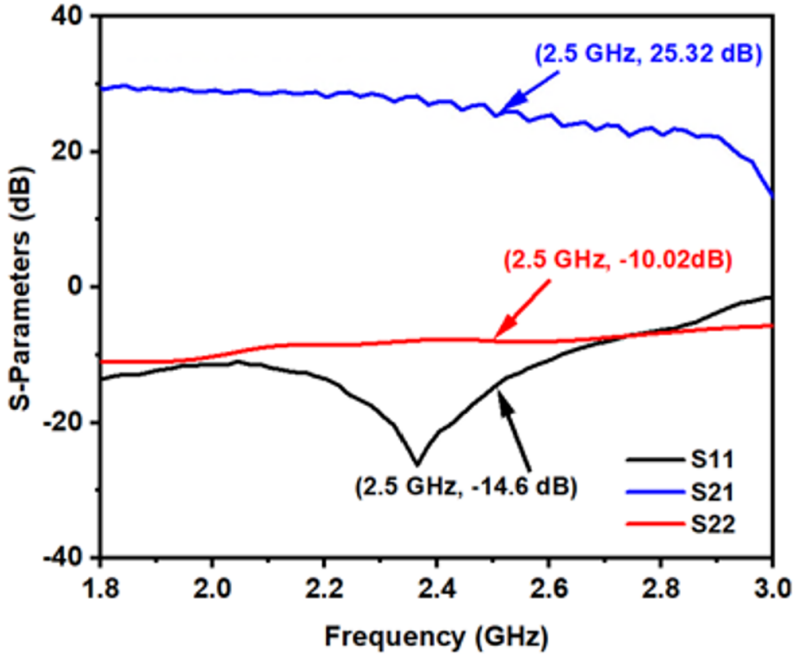

FIGURE 3.5. Drive amplifier - S-Parameters.

TABLE 3.3. Drive amplifier - Comparison

	S11 (dB)	**S21 (dB)**	**S22 (dB)**	**PAE (%)**
Provided	-13	28.8	-10	-
Measured	-14.6	25.32	-10.02	23.2

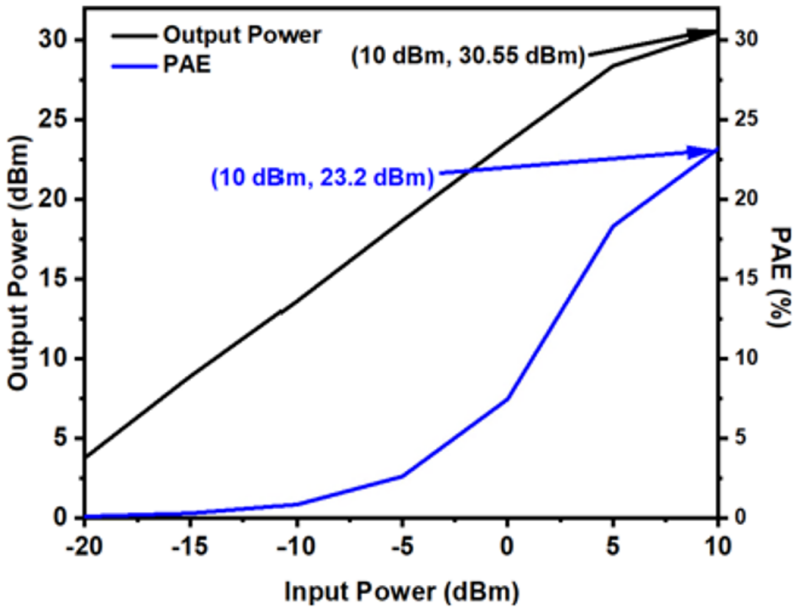

FIGURE 3.6. Drive amplifier - PAE and maximum output.

3.4. Power Amplifier (QPD0005)

Gallium Nitride transistor-Qorvo QPD0005, PA is used to design the DUTs, first Doherty power amplifier, and secondly parallel-connected amplifiers. Gallium Nitride transistor is selected because it provides higher efficiency with minimal size, making it useful for most applications like satellites, communication, robotics, etc. All the calculations, link-budget analysis as shown in Table 2.1 and Table 2.3 is performed based on the selected PA's gain, input and output P1dB, compression point, and supply voltage. S-parameters for PA are shown in Fig. 3.7. Obtained input return loss is -13.61 dB, output return loss is -5.5 dB, where the obtained gain is 17.43 dB at 2.5 GHz, which is 33.92 % lower than the actual gain. Achieved higher efficiency is 36.54 % at maximum output of 34 dBm for 20 dBm input. Plot for PAE is shown in the Fig. 3.8 and comparison between provided data and measured data for s-parameters and PAE are given in Table 3.4.

3.5. Quarter-wave Transmission Line

To provide the input phase difference of 90° between the two parallel-connected amplifiers in Doherty form, a designed quarter-wavelength transmission line is used with charac-

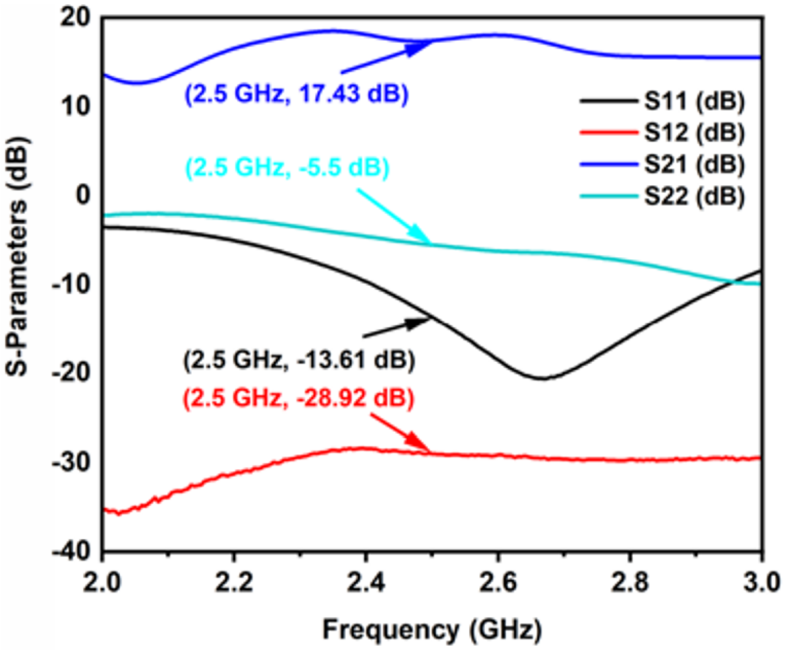

FIGURE 3.7. QPD0005 - S-Parameters.

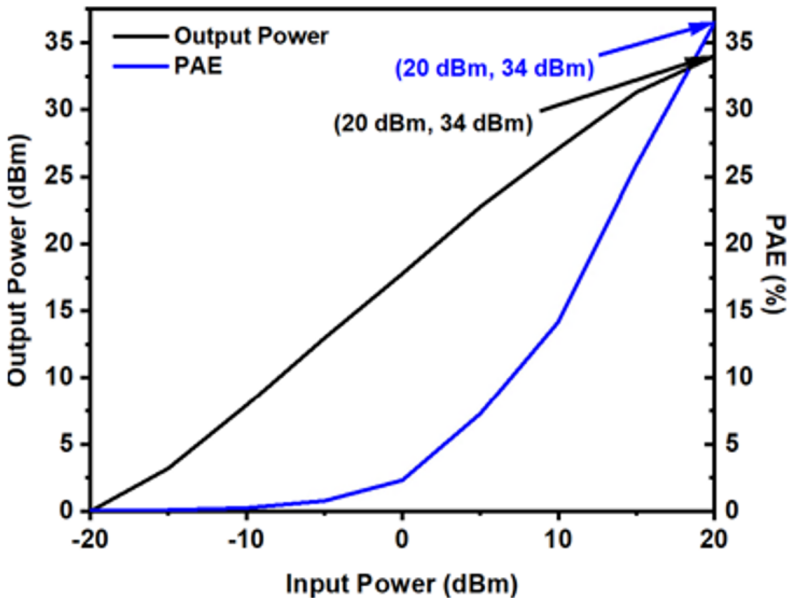

FIGURE 3.8. QPD0005 - PAE and maximum output.

teristic impedance, $Z_0 = 50\Omega$. The measured insertion loss is 1.44 dB, where as the simulated insertion loss is 0.55 dB, as shown in Fig. 3.9. This employed quarter-wave transmission line is supposed to provide a 90° phase shift, but during the test, it is noticed that it is providing a phase shift $-110°$. As of the received phase shift of $-110°$, the whole experiment for DPA

TABLE 3.4. QPD0005 - Comparison

	S11 (dB)	S12 (dB)	S21 (dB)	S22 (dB)	PAE (%)
Provided	-	-32	18.8	-	<32
Measured	-13.61	-32.25	17.43	-5.5	36.54

is done accordingly maintaining the phase gap.

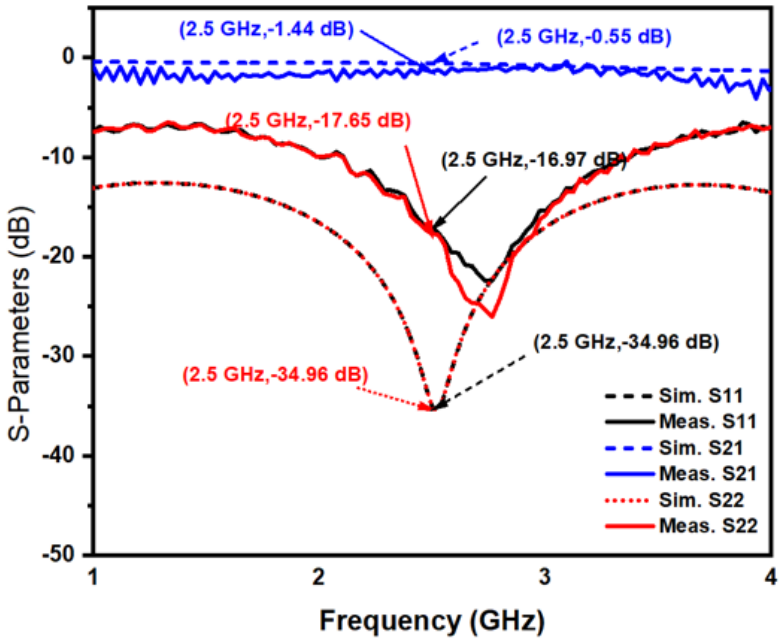

FIGURE 3.9. Return and insertion loss for quarter-wave TL.

3.6. Doherty Power Combiner

For the Doherty power amplifier, the main and peak amplifier inputs are 90° out of phase. Before combining the output of the amplifier, the phase shift needs to be eliminated. Therefore, a quarter-wave transmission line of 50 is employed at the output of the main amplifier, compensates the input phase difference of PAs.

Return losses S11, S22 & S33 and Insertion loss S21 & S31 of the designed and fabricated Doherty power combiner using FR4 dielectric substrate of constant 4.3 and thickness 1.2 mm are shown in Fig. 3.10 and Fig. 3.11, respectively. It can be observed from in Fig. 3.10 that the measured return losses S11, S22 & S33 are -18.12 dB, -19.22 dB & -19.61 dB,

respectively are reduced from the simulated value which are 16.91, -13.92 & -13.91, whereas the measured and simulated insertion loss S21 and S31 are approximately similar, equals to 0.5 dB as shown in Fig. 3.11. The comparison for the simulated and measured s-parameters is shown in table 3.5 for 2.5 GHz. The difference in the simulated and measured values may be because of the real constraints during fabrication and testing.

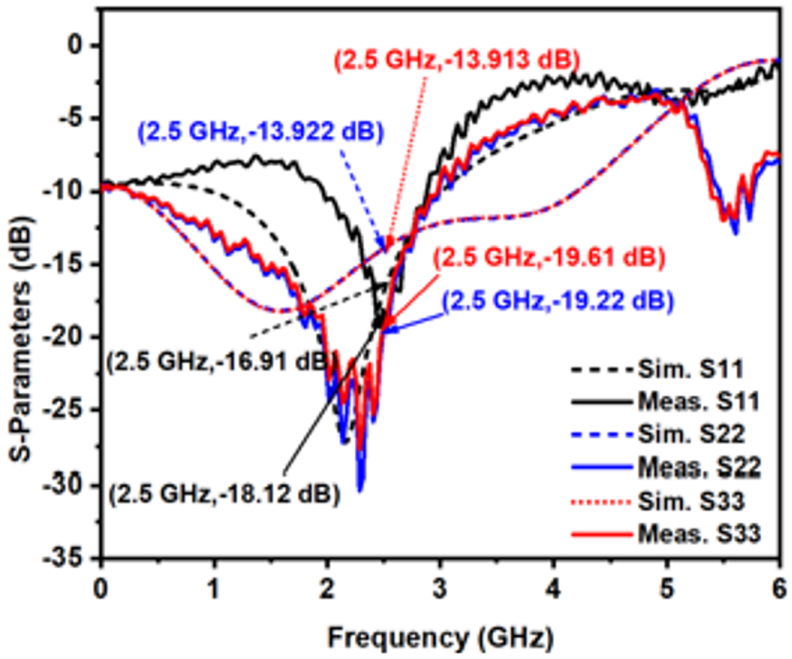

FIGURE 3.10. Doherty power combiner - Return loss.

TABLE 3.5. S-parameters for Doherty power combiner

S-parameters	Simulated (dB)	Measured (dB)
S(1,1)	-16.91	-18.12
S(2,2)	-13.92	-19.22
S(3,3)	-13.91	-19.61
S(2,1)	-3.527	-3.56
S(3,1)	-3.525	-3.5
S(2,3)	-18.05	-20.56

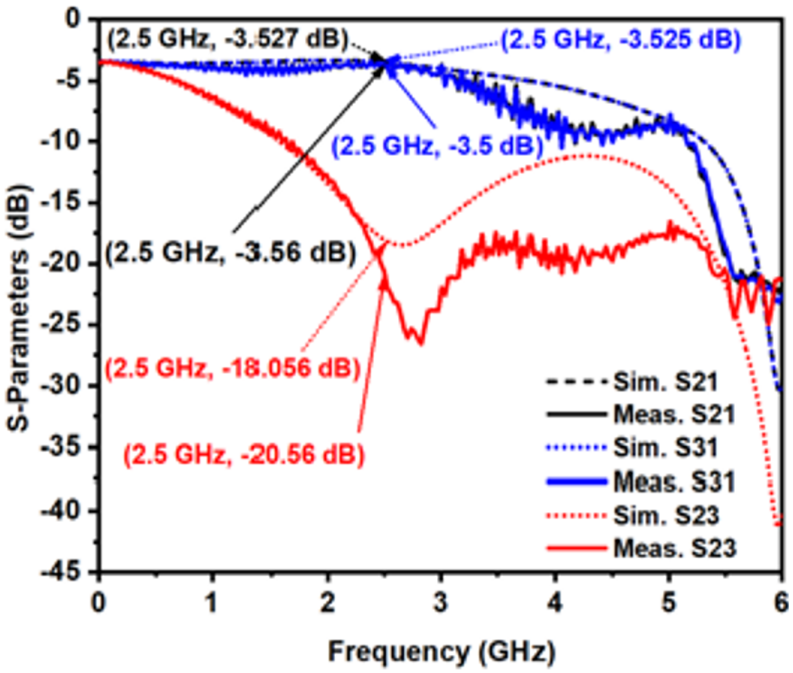

FIGURE 3.11. Doherty power combiner - Insertion and isolation loss.

3.7. 20 dB Directional Coupler

To characterize the DUTs, the inputs, outputs, gain, phase, and power need to be determined. Moreover, to connect the measuring instruments in the RF circuit, a 20 dB directional coupler is designed and fabricated on FR4. The measuring instruments are connected using Port 4, a 20 dB coupled port. Measured insertion loss, S41 is 0.08 dB, which is improved by 3.92% compared to the simulated loss, where the insertion loss, S21 i.e., a through the port, remains the same equals to 1.11 dB, shown in Fig. 3.14. However, the return loss S11, S33, S44 is improved compared to the simulated values Fig. 3.12 and Fig. 3.13.

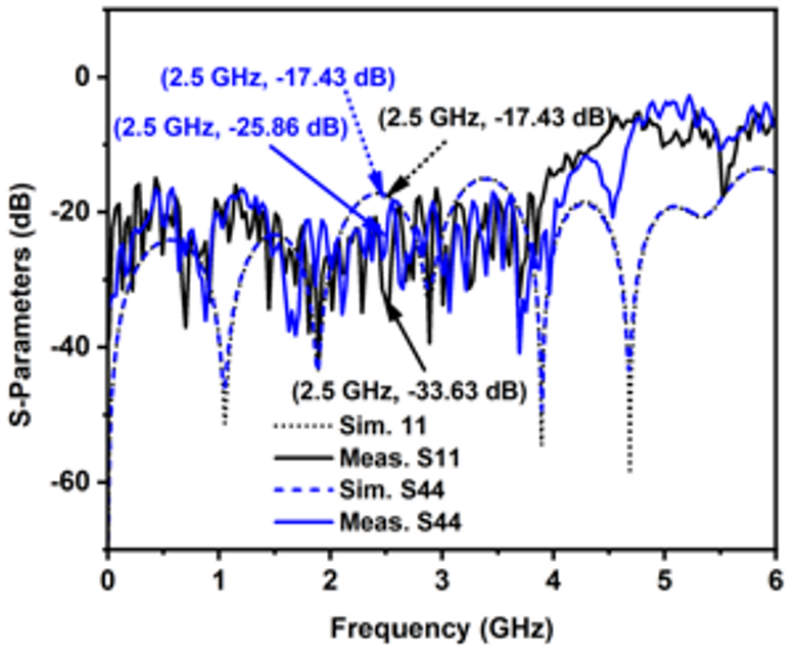

FIGURE 3.12. 20 dB Directional coupler - (a) Return loss for S11 and S44.

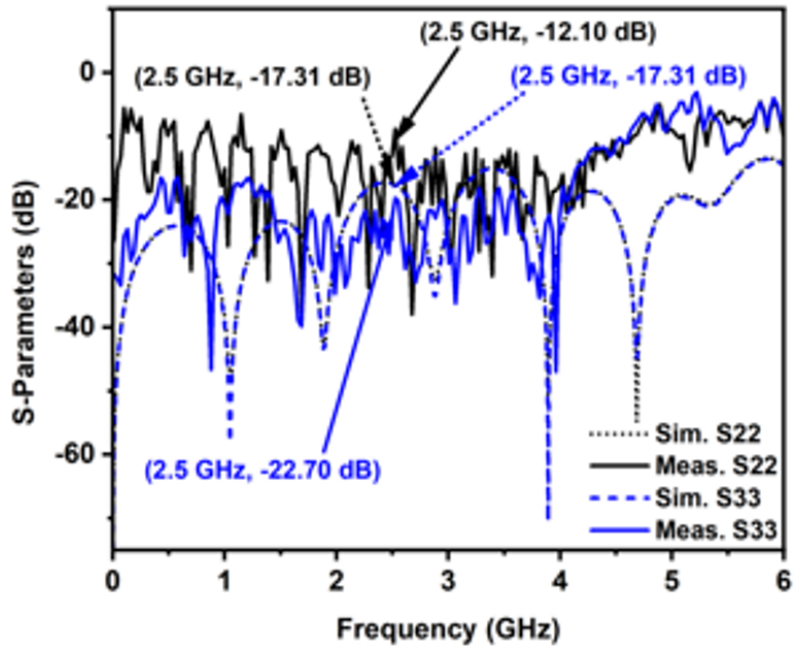

FIGURE 3.13. 20 dB Directional coupler - (b) Return loss for S22 and S33.

3.8. Optimized Outputs of the Designed System

Research is done to determine the input gain ratio, and phase difference for the parallel combined power amplifiers at higher efficiency considering two different DUTs. The

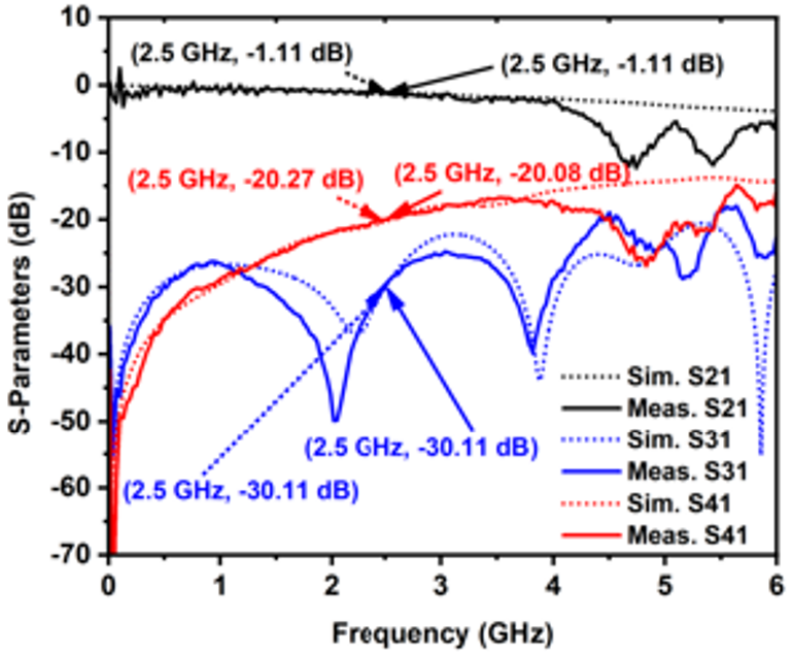

FIGURE 3.14. 20 dB Directional coupler - Insertion losses.

TABLE 3.6. S-parameters for 20 dB Directional coupler

S-parameters	Simulated (dB)	Measured (dB)
S(1,1)	-17.43	-33.63
S(2,2)	-17.43	-25.86
S(3,3)	-17.43	-25.86
S(4,4)	-17.43	-25.86
S(2,1)	-1.11	-1.11
S(3,1)	-30.11	-30.11
S(4,1)	-20.27	-20.08

measurements for both the DUTs show that a parallel combination of amplifiers enables to achieve a higher efficiency when the input gain ratio is zero, and the phase difference between both the inputs is zero as shown in Fig. 3.15 & Fig. 3.15 and Fig. 3.16 & Fig. 3.18. It implies that higher efficiency can be achieved when outputs of the amplifiers are combined in the same phase.

For the first DUT, in the Doherty power amplifier, a quarter-wavelength transmission line is employed at the input of the peak amplifier and another one at the output of the main

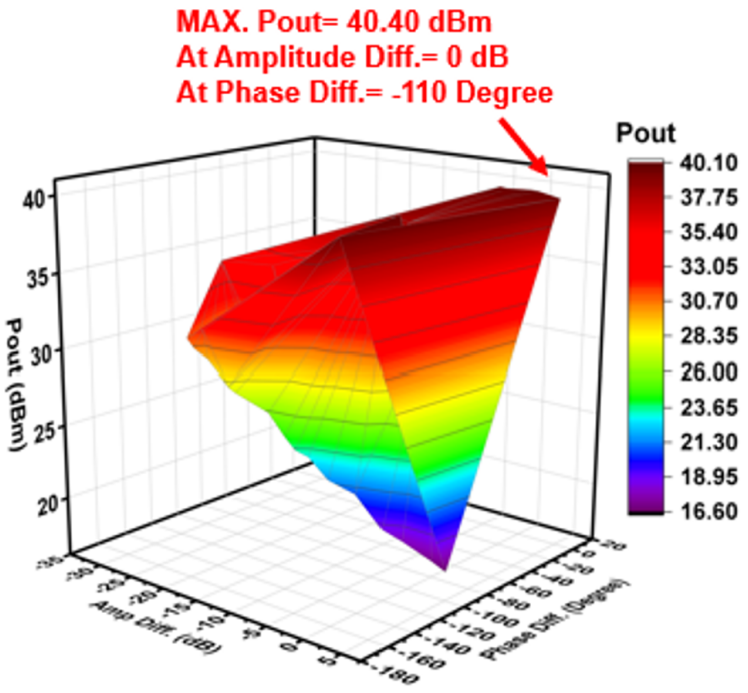

FIGURE 3.15. Doherty power amplifier - Max. Pout.

amplifier to maintain the same phase while combining the outputs. This employed quarter-wave transmission line gives the measured phase shift of $-110°$ as discussed earlier. As a result, the highest efficiency obtained is 40.67% at a maximum output power of 40.40 dBm for input amplitude difference equals to 0 dB and input phase difference of $-110°$ as shown in Fig. 3.15 and Fig. 3.15.

Maximum efficiency and output are obtained at an input phase difference of $-110°$ because of the quarter-wavelength transmission line employed at the input of the peak amplifier.

Similarly, in the case of parallel-connected PAs, the maximum efficiency achieved is 32.70% at the maximum output power of 38.30 dBm for an input gain ratio of 0 dB and a phase difference of $0°$, shown in Fig. 3.16 and Fig. 3.18.

A comparison with the prior work is shown in Table 3.7 with the results obtained from this work. In both of the prior works [**37**, **38**], the system is designed for a fixed PA, which does not give the flexibility of characterizing the other amplifiers. Furthermore,

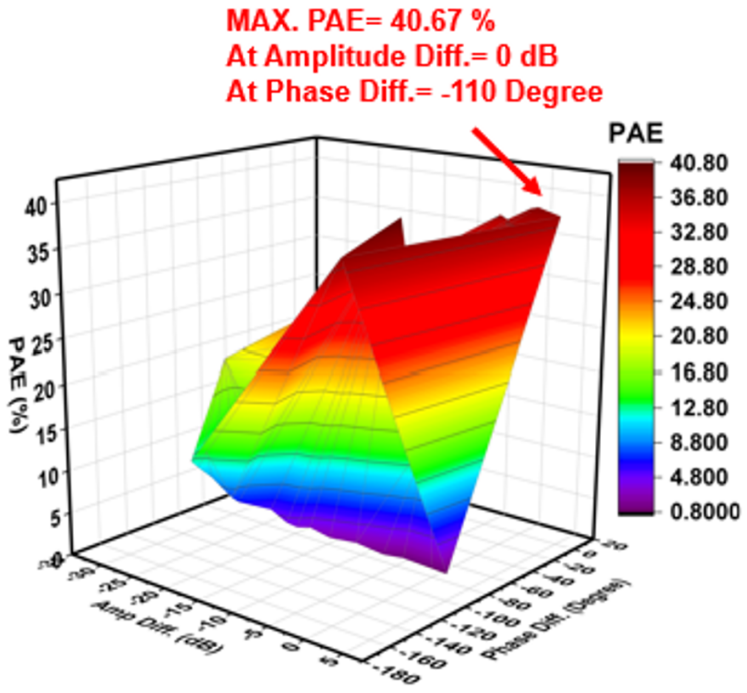

FIGURE 3.16. Doherty power amplifier - Max. PAE.

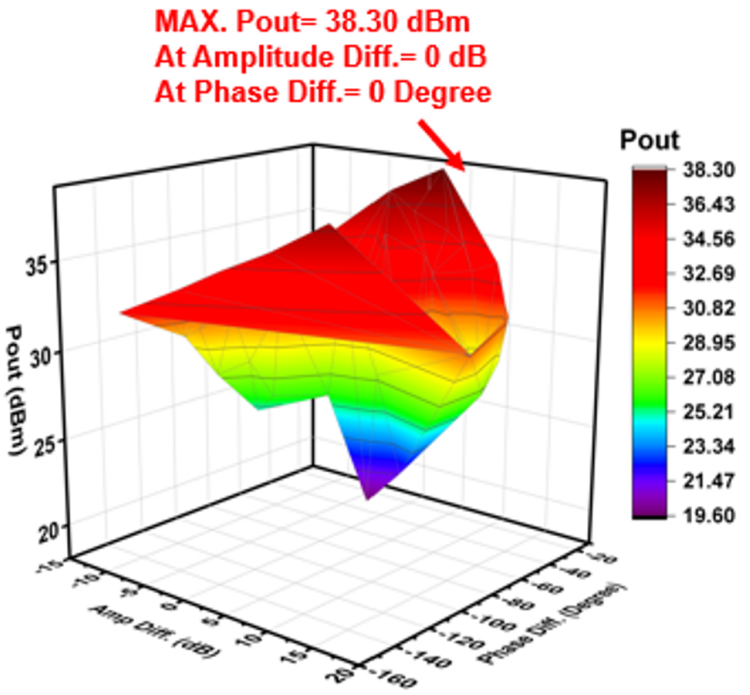

FIGURE 3.17. Parallel connected power amplifier - Max. Pout.

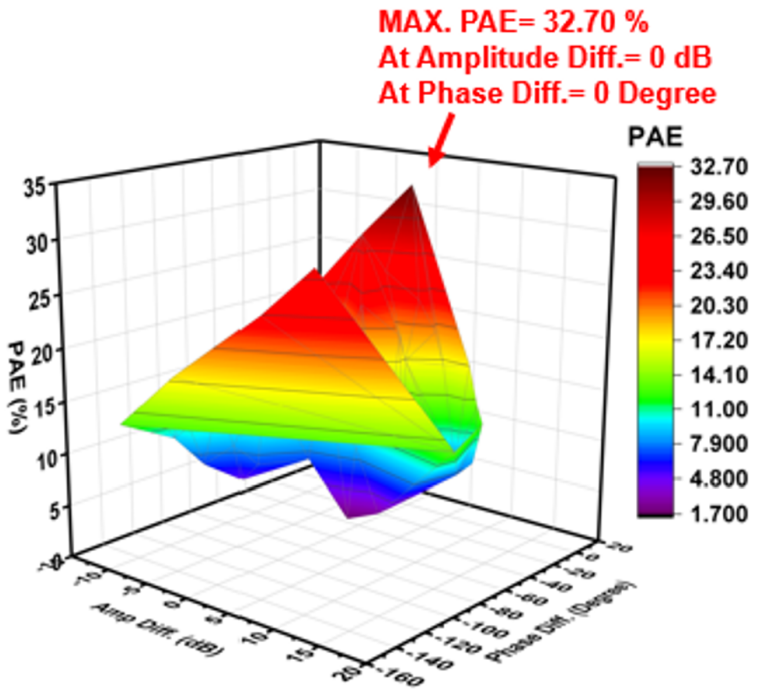

FIGURE 3.18. Parallel connected power amplifier - Max. PAE.

TABLE 3.7. Comparison with other Works

	Frequency (GHz)	**Methods**	**PAE (%)**	**Type**
[**36**]	3.1	Analog	35.0	DPA
[**37**]	3.1	Digital	38.0	DPA
This Work	2.5	Digital	36.62	Parallel Connected PA
This Work	2.5	Digital	40.69	DPA

previous work will not give the flexibility to identify the actual input gain ratio, and phase difference of two parallel amplifiers as the whole system is integrated on the same chip. To compensate this limitation, this work used a gain and phase detector (AD8302), connected just at the input of the PAs. In the second approach [**38**], two different RF generators are used to control the input amplitude and phase of amplifiers, which increases the chance of mismatch error between two signals. This test also proves that the Doherty power amplifier has better efficiency than other parallel combinations of power amplifiers, as shown in Fig. 3.19.

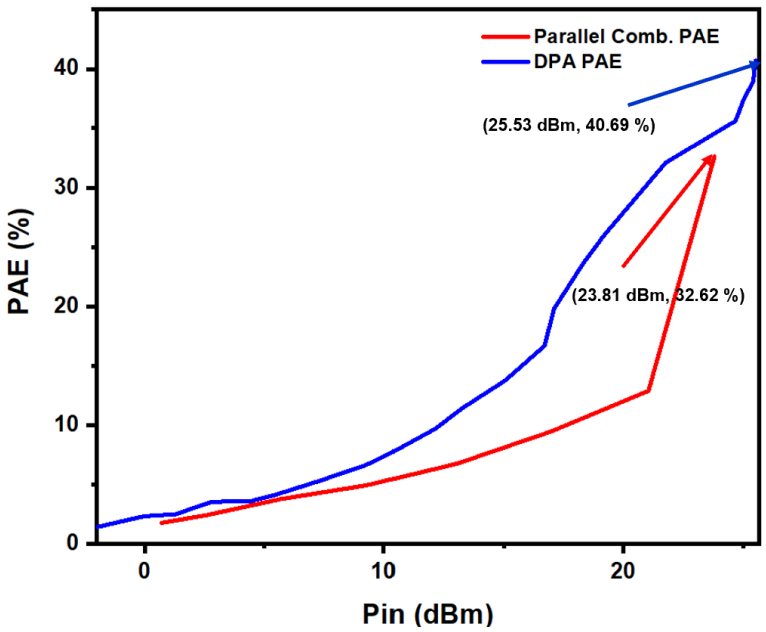

FIGURE 3.19. DPA and Parallel PA comparison.

CHAPTER 4

CONCLUSION

This thesis presents an optimized drive signal control system for a parallel combination of power amplifiers at 2.5 GHz. The designed system includes the selection of appropriate components based on the link-budget analysis, with the fabrication of Wilkinson power splitter, Doherty power combiner, quarter-wave transmission line, and 20dB Directional Coupler. The work presents the design of the effective control system, which is designed for the independent controls of the parallel-connected power amplifiers. The designed control system controls the amplitude and phase of the input signal of amplifiers. Then link-budget analysis is performed on the whole system to select the specification of the components to be used in the tests, i.e., for parallel-connected power amplifier and Doherty power amplifier.

The tests helped obtain the input amplitude difference and phase difference for the higher efficiency of parallel combined power amplifiers, which are 0 dB and 0°, respectively. Similarly, the input amplitude and phase differences for the Doherty power amplifier are 0 dB and -110 degrees, respectively. Therefore, it has been concluded that higher efficiency can be achieved only when there is a zero phase difference between signals of the parallel branches.

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