HYBRID NANOCOMPOSITES FOR BOLOMETER APPLICATIONS

Andrew Cook
Honors Capstone Thesis
Dr. Usha Philipose
1 May 2013

Hybrid Nanocomposites for Bolometer Applications

Andrew Cook; Usha Philipose, Ph.D

Abstract

This work is a study on the properties of amorphous silicon (α-Si) and crystalline silicon nanowires (c-Si NWs), focusing on the requirements placed on thin films by bolometers. Efficient bolometer performance requires that thin films have low resistivity, high temperature coefficient of resistance (TCR), and negligible low frequency noise. However, α-Si thin films are typically characterized by high resistivity and low signal-to-noise ratios. Reducing resistivity through doping is not practical. A possible solution lies in the fabrication of a hybrid nanocomposite, comprising of crystalline Si nanowires sandwiched between α-Si thin films. To test this, we must analyze the electrical properties of both α-Si and c-Si NWs. Thus, we must run 2-terminal, 4-terminal, and temperature dependent tests, in addition to Deep Level Transient Spectroscopy, on α-Si. On c-Si NWs, we must run 2-terminal and 3-terminal tests, as well as Raman Spectroscopy. These tests will enable us to determine whether my hypothesis is supported. If this is so, we will have developed the potential to make bolometers more sensitive and potentially more efficient.

Introduction

A bolometer is an instrument that measures infrared radiation by means of heating a thin film material with a temperature dependent resistance. As such, the thin film material needs to have a high temperature coefficient of resistance (TCR), as well as low resistivity and a low signal-to-noise ratio. Amorphous silicon (α-Si), is the current favorite thin film for bolometer technology, but can be improved upon. α-Si has several positives, including nontoxicity, high TCR, and the ability to control resistivity through doping. Limitations of α-Si include a high

resistivity[1] and a low signal-to-noise ratio. Though doping can control resistivity, it also reduces the TCR in α-Si.[2] One possible method of improving upon α-Si is forming a hybrid nanocomposite material with α-Si as the host and crystalline silicon nanowires (c-Si NWs) as the inclusions. c-Si NWs have several desirable characteristics which make them a natural inclusion option. Firstly, nanowire defects are much more easily controlled than those of bulk materials, which makes them more efficient than their bulk counterparts. They can also be doped more effectively than bulk materials. In addition, c-Si NWs represent "an approximately 100-fold improvement over bulk Si [which] can be achieved over a wide [temperature] range" in terms of thermal conductivity.[3] This means that c-Si NWs have a high TCR. When two materials such as these are combined, the resulting composite tends to mirror the traits of both materials. Thus, we theorize that a hybrid structure will be an improvement over α-Si for bolometer applications. It must be noted that in forming the nanocomposite material, the arrangement of the nanowires is not important. They don't have to be arrayed in parallel as Figure 1 indicates.

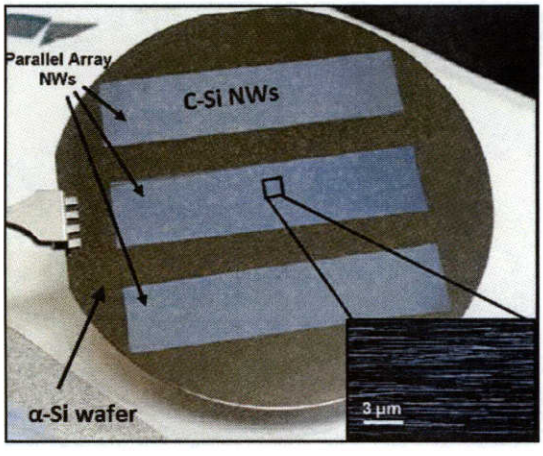

Figure 1: Amorphous silicon wafer with contacted c-Si NW arrays

[1] Hanson, Charles. 2011. "Amorphous-silicon bolometers could surpass IR focal-plane technologies." *Laser Focus World* 47, no. 4: 67-71. *Academic Search Complete*, EBSCO*host* (accessed October 29, 2011).

[2] Torres, A., A. Kosarev, M.L. García Cruz, and R. Ambrosio. 2003. "Uncooled micro-bolometer based on amorphous germanium film." *Journal of Non-Crystalline Solids* 329, no. 1-3: 179. *Academic Search Complete*, EBSCO*host* (accessed October 29, 2011).

[3] Kazan, M., G. Guisbiers, S. Pereira, M. R. Correia, P. Masri, A. Bruyant, S. Volz, and P. Royer. 2010. "Thermal conductivity of silicon bulk and nanowires: Effects of isotopic composition, phonon confinement, and surface roughness." *Journal Of Applied Physics* 107, no. 8: 083503-083517.*Academic Search Complete*, EBSCO*host* (accessed December 3, 2011).

In order to properly analyze a hybrid nanocomposite material, we must first understand the properties of the host and inclusions. Thus, the objective of this thesis was to characterize α-Si and c-Si NWs separately. On α-Si, a 2-terminal test can be used to find resistance information across the material. A 4-terminal test, also called the Van der Pauw test, is used to find sheet resistance and resistivity. We can run 2-terminal tests over a range of temperatures to determine Mott or Arrhenius behavior. Finally, DLTS is useful for finding information on deep level traps within the material, such as the activation energy of the deep level, the trap concentration, and capture cross section at the deep level. On c-Si NWs, we can again use a 2-terminal test to find resistance. We can use Raman spectroscopy to determine the composition of our sample. Lastly, we can use a 3-terminal test on a gated sample to determine field effect mobility and carrier concentration. All of these tests help us characterize α-Si and c-Si NWs so that a proper study of a hybrid nanocomposite structure can be done.

Tests on Amorphous Silicon

Our α-Si sample is mounted with four terminals, as illustrated in Figure 2. To run a 2-terminal test, we simply run a voltage through one terminal and measure the current through a second terminal, using this to calculate resistance. We also use this test in a cryostat to examine the effect of changing temperature on α-Si. From this information, we can determine at what range of temperature the sample exhibits Arrhenius behavior, which follows the equation

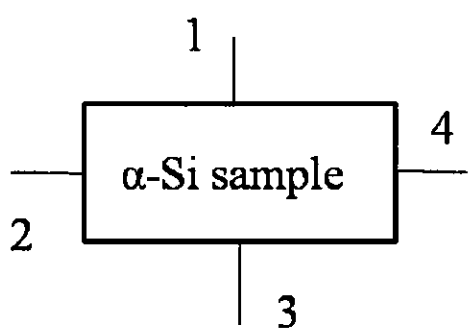

Figure 2: A sketch of a sample used for 4-terminal tests, with contacts 1, 2, 3, & 4.

$$\sigma(T)_A = \sigma_{0A} e^{\frac{E_A}{kT}}$$

or Mott behavior, which follows the equation

$$\sigma(T)_M = \sigma_{0M} e^{\left(\frac{T_0}{T}\right)^{1/4}}$$

Where T is the temperature, E_A is the activation energy, and k is the Boltzmann constant. In both cases, we have to solve for the constants.

The Van der Pauw test is a bit more complicated. We put a current through two contacts, such as 1 and 2 in Figure 2, which we call I_{12}, and measure the voltage between the other two contacts, which in this case would be 3 and 4, to obtain the voltage we call V_{34}. From this voltage and current we can calculate a resistance, as follows:

$$R_{12,34} = \frac{V_{34}}{I_{12}}$$

Then we change the contacts to get $R_{34,12}$. Also, by reversing the direction of the current, we can get more values for each resistance, reducing the effects of contact resistance. Thus, we will have resistances $R_{12,34}$, $R_{34,12}$, $R_{21,43}$, and $R_{43,21}$. Lastly, we switch contacts and get four more resistances that follow the same numbering format: $R_{23,41}$, $R_{41,23}$, $R_{32,14}$, and $R_{14,32}$. We take the average of each set and name first set's average R_a and the second R_b. To find the sheet resistance R_s, we use this equation:

$$e^{-\frac{\pi R_a}{R_s}} + e^{-\frac{\pi R_b}{R_s}} = 1$$

It must be noted that this equation cannot be solved analytically, but rather numerically. For our purposes, the Van der Pauw test program on the Agilent B1500A machine in our lab calculates R_s. Once we know R_s, we can calculate resistivity through the equation $\rho = \frac{R_s A}{l}$ where A is the

cross-sectional area of the material and *l* is the thickness of the material. Our sample's cross-sectional area is 2.5 μm^2 and its thickness is 50.5 nm.

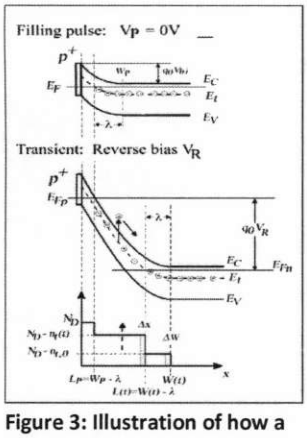

Figure 3: Illustration of how a filling pulse is used to fill traps with carriers

Mott behavior indicates the presence of deep level traps, so we use DLTS to obtain the trap signature, which includes trap density, capture cross-section, and energy level of the traps. Deep level traps interfere with the capacitance across the material in question by changing the width of the space-charge region of the material. To analyze these traps, we must fill the traps with carriers. To do this, we apply a filling pulse bias, as shown in Figure 3, which can be either optical or electrical. While the pulse is applied, the capacitance increases due to the bias. After the filling pulse, we apply an emptying pulse, which is intended to relax the trap. This results in a negative spike in the capacitance before it gradually relaxes back to normal, as shown in Figure 4. We measure the change in capacitance (ΔC) over a range in time, after a predetermined delay. This ΔC helps us determine trap concentration. We can take these measurements as a function of increasing temperature and thereby show where on the energy spectrum the deep level exists, as shown in Figure 5. We do this for different time delays to get a series of peaks like the one in Figure 5. We can take these peaks and plot them with a best-fit line to determine the capture cross-section and the trap density.

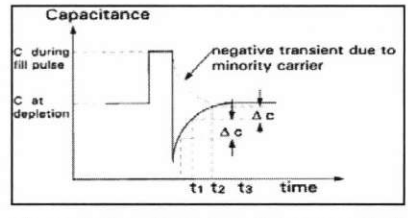

Figure 4: Capacitance vs. time grave that shows the effects of the filling and emptying pulses and the relaxation of the traps

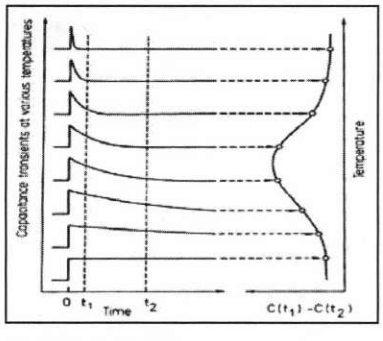

Figure 5: Relaxation measurements taken over a range of temperatures help us determine the energy levels of traps

The α-Si sample we use for DLTS is a dielectric, which in our case is Si_3N_4, sandwiched

between a α-Si layer and a metal contact. Before running DLTS on an α-Si sample, We have to run a capacitance-voltage (C-V) test on it to try to determine the threshold voltage (V_{th}) of the sample. If V_{th} is reasonable, then we can run DLTS on the sample. In order to calculate V_{th}, we must be able to find the flatband voltage (V_{fb}) and the capacitance across the dielectric (C_{de}) according to the equation

$$V_{th} = \left[\pm\frac{A}{C_{de}}\sqrt{4\varepsilon_s q|N_b||\Phi_b|} + 2|\Phi_b|\right] + V_{fb}$$

where A is the gate area, ε_r is the permittivity of α-Si, q is electron charge, and N_b & Φ_b are bulk doping and bulk potential respectively. All of these are constants for our applications. C_{ox} depends on the oxide thickness according the equation

$$C_{de} = \frac{A\varepsilon_{de}}{(1\times10^{-19})t_{de}}$$

Where ε_{de} is the dielectric constant. V_{fb} is the result of the disappearance of band bending and can be identified from the C-V graph using the value for the flatband capacitance, which can be calculated using the equation

$$C_{fb} = \frac{\frac{C_{de}\varepsilon_S A}{(1\times10^{-4})\lambda_D}}{(1\times10^{-12})C_{de} + \frac{\varepsilon_S A}{(1\times10^{-4})\lambda_D}}$$

where λ_D is the extrinsic Debye length, which is calculated by the equation

$$\lambda_D = \left(\frac{\varepsilon_s kT}{q^2 N_x}\right)^{1/2}$$

where kT is the thermal energy at room temperature and N_x is either the donor or acceptor concentration.[4]

Tests on Silicon Nanowires

Our c-Si NW samples consist of NWs connecting two Au contacts on a Si substrate with a SiO_2 layer between the NWs and the substrate. To create the gate, we scratch away the oxide layer at one corner of the sample and attach a Au contact there. The 2-terminal test works the same way here as it did on the α-Si. For the 3-terminal test, we apply a gate voltage and then run a voltage between the source and the drain, measuring the resultant current. This information can be used to calculate field effect mobility and majority carrier concentration.

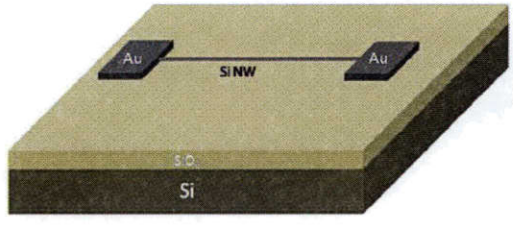

Figure 6: Conceptual rendition of a 3-terminal NW sample

To obtain field effect mobility, we must model the sample as a nanowire field effect transistor (NWFET). In this model, represented by Figure 6, the nanowire is the channel, the Au contacts are our source and drain, and the Si substrate serves as a back gate. Given this, we must start with the equation for current between the source and drain:

$$I_{DS} = \int qnv_d dA$$

Here, q is the charge of a carrier, v_d is drift velocity, A is the cross-sectional area of the nanowire, and n is the number of carriers per unit volume $\left(n = \frac{N}{V}\right)$.We know $v_d = \mu_{FE}E$. The only electric field we have to worry about here is that caused by the potential difference between the source

[4] Keithley. "Gate Dielectric Capacitance-Voltage Characterization Using the Model 4200 Semiconductor Characterization System." 2006

and the drain, so we can define $E = \frac{V_{DS}}{L}$ where V_{DS} is the potential difference from drain to source and L is the length of the gate. Now, our equation looks like this:

$$I_{DS} = \int \frac{qn\mu_{FE}V_{DS}}{L} dA$$

μ_{FE} and V_{DS} are not affected by the integral, but qn is affected. By defining Q_{acc} to be the accumulation charge of our system, we can make the following transformation:

$$\int qndA = \frac{Q_{acc}}{L}$$

Thus, we have:

$$I_{DS} = \frac{\mu_{FE}Q_{acc}V_{DS}}{L^2}$$

We can, according to S. Dayeh et. al. make $Q_{acc} = C(V_{GS} - V_t)$ where C is the capacitance between the gate and the wire, V_{GS} is the potential difference between the gate, and the source and V_t is the threshold voltage.[5] Thus,

$$I_{DS} = \frac{\mu_{FE}C(V_{GS} - V_t)V_{DS}}{L^2}$$

This can be rearranged to give:

$$\mu_{FE} = \frac{I_{DS}L^2}{C(V_{GS} - V_t)V_{DS}}$$

If we move I_{DS} to the denominator, we get this:

$$\mu_{FE} = \frac{L^2}{CV_{DS}\left(\frac{V_{GS}}{I_{DS}} - \frac{V_t}{I_{DS}}\right)}$$

Now, the transductance is defined as $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, so if we assume the relationship between I_{DS} and V_{GS} is linear, then $\frac{V_{GS}}{I_{DS}} = \frac{1}{g_m}$. Also, $\frac{V_t}{I_{DS}}$ becomes one of the contact resistances. If we take the

[5] Dayeh, Shadi A., Aplin, D. P. R., Zhou, X., Yu, P. K. L., Yu, Edward T. and Wang, D., Small, **2007,** 3: 326–332. doi: 10.1002/smll.200600379

contact resistance to be negligible, then this term goes away and our equation resolves itself thusly:

$$\mu_{FE} = \frac{g_m L^2}{C V_{DS}}$$

In order to arrive at this equation, a few assumptions had to be made. Firstly, we had to assume that the relationship between I_{DS} and V_{GS} is linear. In our experimentation, we see that this assumption is reasonable. Second, we have to make the assumption that the contact resistances are negligible. Gold is highly conductive compared to a c-Si NW, so this assumption is reasonable. Lastly, we must assume that all interface states can effectually be neglected. If we do not assume this, then extra terms must be incorporated, as is seen in S. Dayeh's analysis of mobility in InAs wires.[6] In Si wires, however, interface states can be neglected, so our equation holds.

To calculate carrier concentration, we must first start with the equation $Q_{tot} = Nq$ where Q_{tot} is the total charge, N is the number of carriers, and q is the charge per carrier. Rearranging this gives us $N = \frac{Q_{tot}}{q}$. We know carrier concentration by definition:

$$n = \frac{N}{V}$$

where V is volume of channel, so we can substitute for N and get this:

$$n = \frac{Q_{tot}}{qV}$$

We are dealing with a gated nanowire, so we can take $V = \pi R^2 L$, refining our equation as so:

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[6] Dayeh, Shadi A., Aplin, D. P. R., Zhou, X., Yu, P. K. L., Yu, Edward T. and Wang, D., Small, **2007**, 3: 326–332. doi: 10.1002/smll.200600379

$$n = \frac{Q_{tot}}{q\pi R^2 L}$$

If we take $Q_{tot} = Q_{acc} = C(V_{GS} - V_t)$, then:

$$n = \frac{C(V_{GS} - V_t)}{q\pi R^2 L}$$

Lastly, we must account for the fact that we do not know whether the charge is carried primarily by electrons or holes. To account for this, our equation must be changed thusly:

$$n = \frac{C|V_{GS} - V_t|}{q\pi R^2 L}$$

In this equation, as in the field-effect mobility equation, C is the capacitance between the NW and the α-Si. Thus, we must derive an equation for C. To do this, we must start with the definition of capacitance between two electrodes:

$$C = \frac{Q}{\phi_a - \phi_b}$$

Here, Q is total charge on each electrode and $\phi_a - \phi_b$ is the potential difference between the two electrodes. In order to obtain the capacitance between the nanowire and the gate, we must model it as a cylinder-plane capacitor, as shown in Figure 7. For our purposes, we will make C equal capacitance per unit length. Thus, our equation will be changed to:

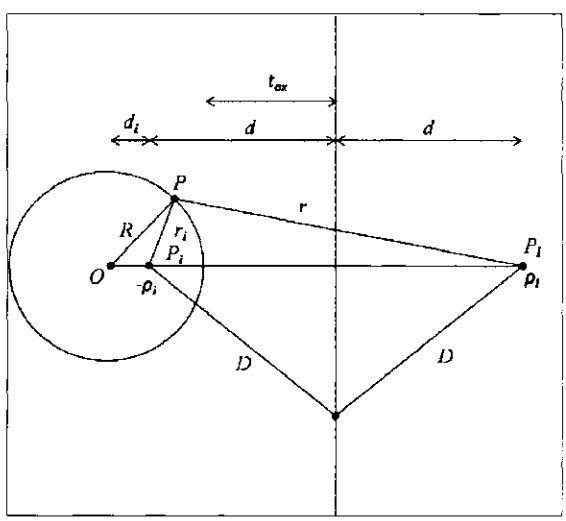

Figure 7 Cross-sectional view of the plane-and-cylinder model for nanowires on a sample with an oxide layer acting as a dielectric. tox is the oxide thickness, R is the radius of the NW.

$$C = \frac{\rho_l L}{\phi_{cyl} - \phi_{pln}}$$

Here, ρ_l is charge per unit length and $\phi_{cyl} - \phi_{pln}$ is the potential difference between a nanowire, modeled as a conductive cylinder of radius R, and a plane conductor. First, we will discuss the potential for the cylinder, which requires that we use the method of images. The potential at a distance r from a line charge can be taken as $\phi = \int_{r_0}^{r} E dr$ where E is the magnitude of the electric field due to the line charge. Since $E = \frac{\rho_l}{2\pi\varepsilon r}$,

$$\phi = \frac{\rho_l}{2\pi\varepsilon} ln\left(\frac{r_0}{r}\right)$$

If this is true and we take $\rho_i = -\rho_l$,

$$\phi_{cyl} = -\frac{\rho_l}{2\pi\varepsilon} ln\left(\frac{r_i}{r}\right)$$

Due to the nature of the method of images, triangles OPP_i and OP_iP are similar. Thus, $\frac{r_i}{r} = \frac{R}{2d+d_i}$. Also, d_i will get smaller as $\frac{t_{ox}}{R}$ gets larger. Thus, if $\frac{t_{ox}}{R} \gg 1$, $d \approx t_{ox} + R$ and $\frac{R}{2d+d_i} \approx \frac{R}{2d}$. We know that $\phi_{pln} = 0$ because for a point charge near a conducting plane, the potential on the surface of the plane is zero. Therefore,

$$C = \frac{\rho_l L}{-\frac{\rho_l}{2\pi\varepsilon} ln\left(\frac{R}{2d+d_i}\right)} \approx \frac{2\pi\varepsilon L}{ln\left(\frac{2d}{R}\right)}$$

We know that :

$$ln\left(x + \sqrt{x^2+1}\right) = cosh^{-1}(x)$$

Since we are assuming $\frac{t_{ox}}{R} \gg 1$, then:

$$ln\left(\frac{2d}{R}\right) \approx ln\left[\frac{d}{R} + \sqrt{\left(\frac{d}{R}\right)^2 + 1}\right]$$

$$ln\left(\frac{2d}{R}\right) \approx cosh^{-1}\left(\frac{d}{R}\right)$$

$$ln\left(\frac{2d}{R}\right) \approx cosh^{-1}\left(\frac{t_{ox}+R}{R}\right)$$

Thus,

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{cosh^{-1}\left(\frac{t_{ox}+R}{R}\right)}$$

Here it must be noted that ε_r is the effective dielectric constant for SiO_2.

In order to arrive at this equation, a couple of assumptions had to be made. Firstly, we had to assume that the nanowire would act as a conductor. This assumption must be made in order to treat the nanowire and the substrate as a capacitor. In practice, Si nanowires often do behave conductively, so this is a reasonable assumption. We also had to assume that the thickness of the oxide dielectric far exceeds the radius of the nanowire in question. This also is a reasonable assumption since $\frac{t_{ox}}{R} > 6$ for our samples.

Raman spectroscopy makes use of the Raman effect to, among other applications, identify the elements present in a material. The Raman effect occurs when light interacts with the electrons within a molecule. When the photons of the incident light encounter the molecule, the molecule will sometimes take energy from or impart energy to the photons, so that some of the scattered light has a different energy than the incident light. The magnitude of change in energy depends on the rotational and vibrational states of the molecule in question, so different elements and compounds will affect the energy of the incident light differently, thus making it very good for determining the composition of the sample in question.[7] We use Raman spectroscopy to determine the composition of our nanowires. This is necessary to be confident in our results.

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[7] *Encyclopædia Britannica Online*, s. v. "Raman effect," accessed March 26, 2013, http://www.britannica.com/EBchecked/topic/490453/Raman-effect

Results

On both α-Si and c-Si NW samples, we ran our 2-terminal tests from -1 V to 1 V. In α-Si, the relationship between the voltage and current is linear, as can be seen in Figure 8(a). The relationship between voltage and current in c-Si NWs should be linear, but is slightly curved, as shown in Figure 8(b), because the silver we used to apply the gold contacts to the sample creates a diode effect. We got for α-Si a resistance of 64.85 MΩ and for our c-Si NW sample, we got a resistance of 1.315 MΩ.

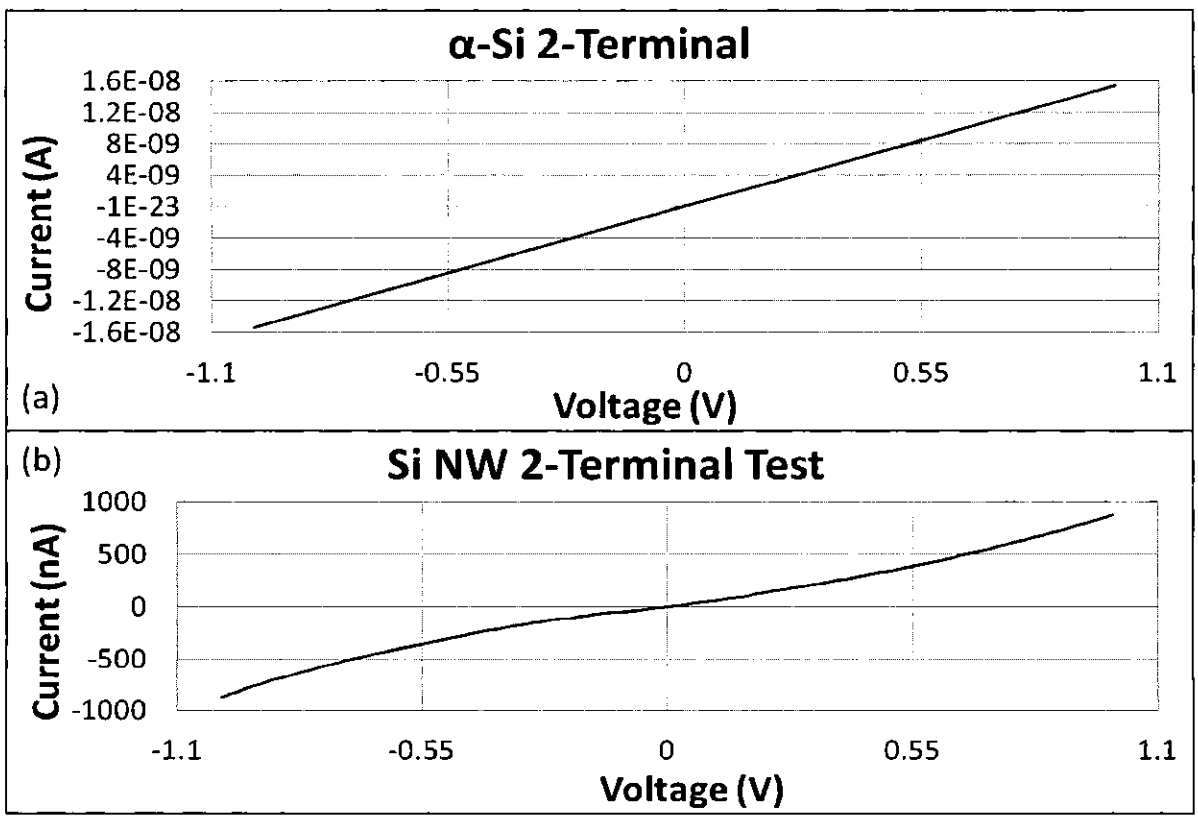

Figure 8: (a) 2-terminal test results for amorphous silicon; (b) 2-terminal test results for silicon nanowires

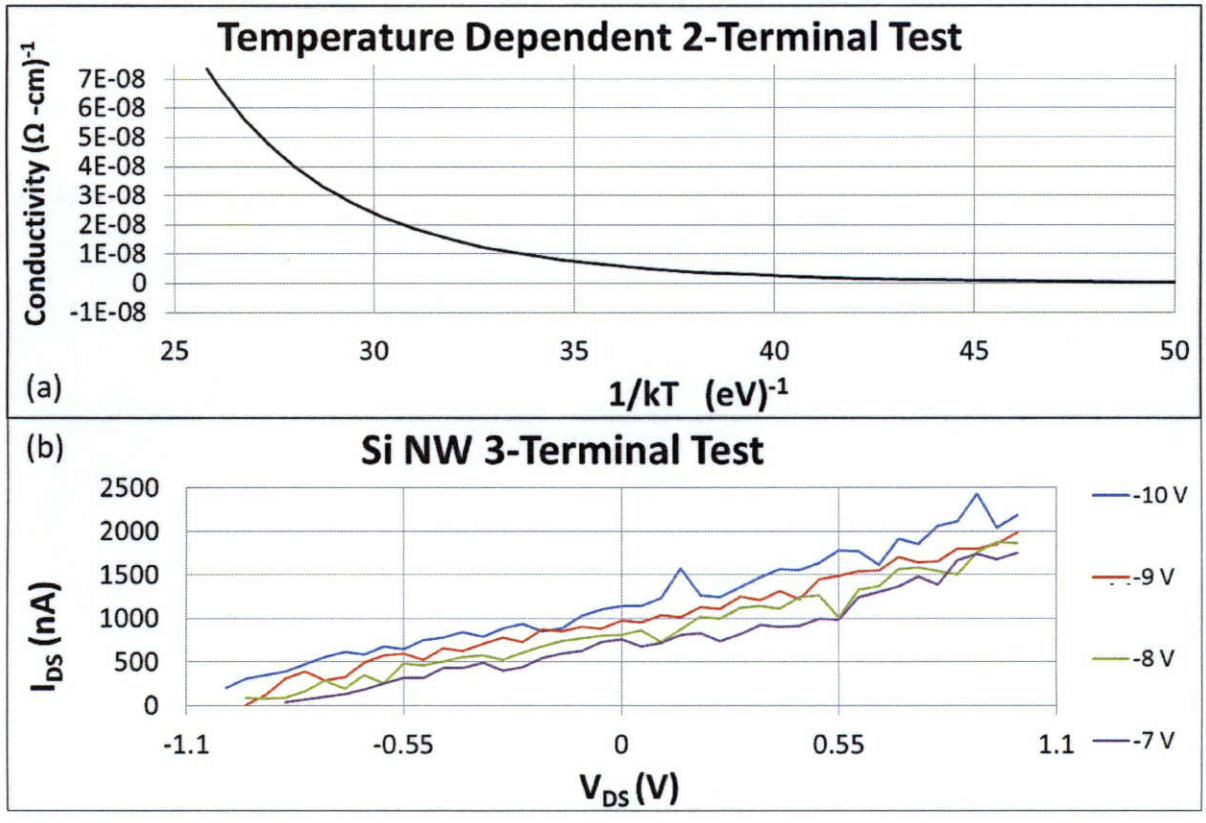

Figure 9: (a) conductivity vs. T^{-1} graph, showing the results of the temperature dependent 2-terminal test on amorphous silicon; (b)3-terminal test results for silicon nanowires with gate voltages at -7, -8, -9, and -10 V

We ran the temperature dependent 2-terminal test over a range of 85 K to 450 K, but the readings below 105 K were too noisy to be useful. From this information, we plotted conductivity as a function of 1/kT, as shown in Figure 9(a). As shown, the relationship is exponential in nature. We took the range of 105 K to 275 K and assumed Mott behavior in order to calculate σ_{0M} and T_0. F-or these constants, we got values of $3*10^{43}$ Ω-cm and $8.55*10^8$ K respectively. These values are rather abnormal, but I did not have an opportunity to rerun this test. We then took the temperature range of 285 K to 450 K and assumed Arrhenius behavior to calculate σ_{0A} and E_A, for which we got $3*10^{-5}$ Ω-cm and 0.234 eV respectively.

We ran a 4-terminal test on α-Si over a range of -1 V to 1 V and got a sheet resistance R_s = 42.37 Ω and a resistivity of 2.09 Ω-m. As illustrated in Figure 9(b), we ran 3-terminal tests at

gate voltages ranging from -10 V to 10 V through a V_{DS} (V) range of -1 V to 1 V. From this we got a field effect mobility μ_{FE} dependent on V_{DS}, as shown in Figure 10(a). We also got a carrier concentration dependent on V_{GS} as shown in Figure 10(b).

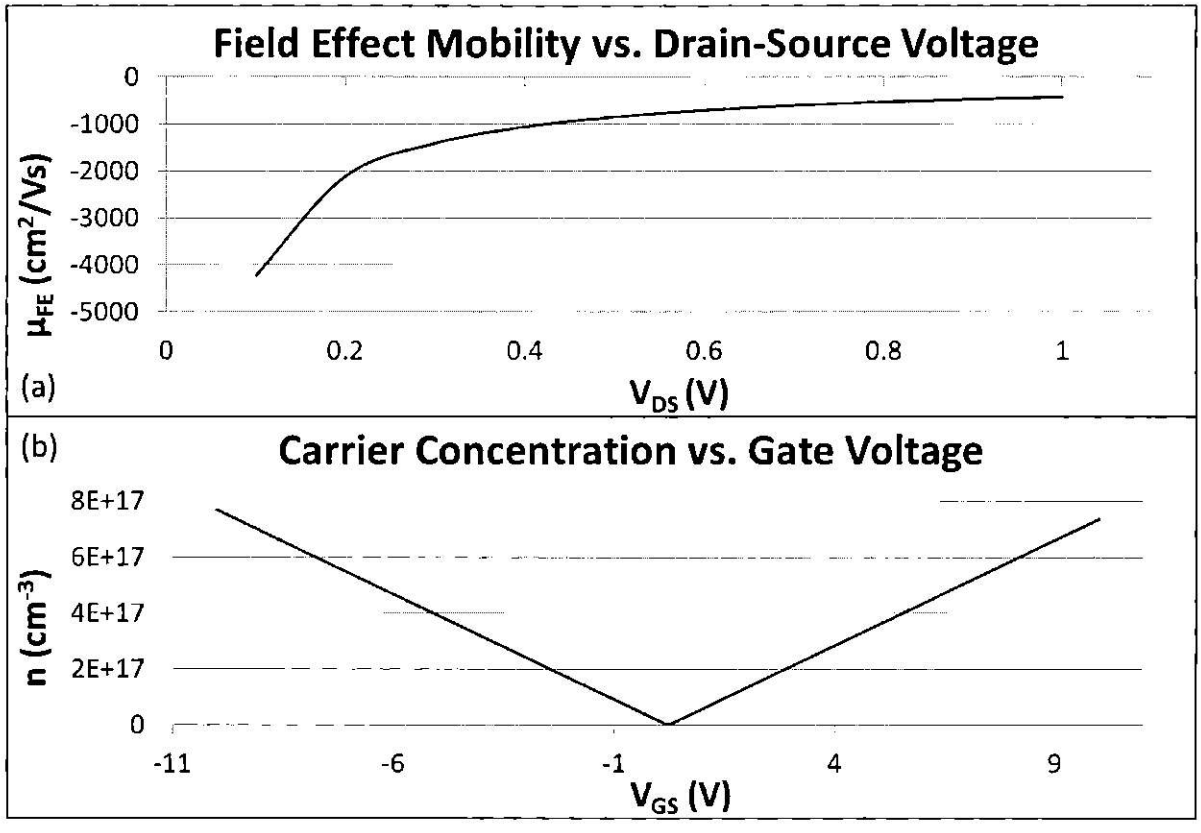

Figure 10: (a) Field effect mobility versus drain-source voltage; (b) carrier concentration versus gate voltage

We ran a C-V test on an α-Si sample at high and low frequency, which resulted in the graph in Figure 11. We could not calculate C_{fb}, so we couldn't arrive at a value for V_{fb}. Thus, we couldn't find a value for V_{th}, preventing us from running DLTS on this sample. It seems that this failure is due to the fact that the dielectric thickness is too small, preventing us from arriving at a value for our threshold voltage. A new α-Si sample with a thicker dielectric layer was being prepared, but at the time of this writing, it wasn't ready for testing.

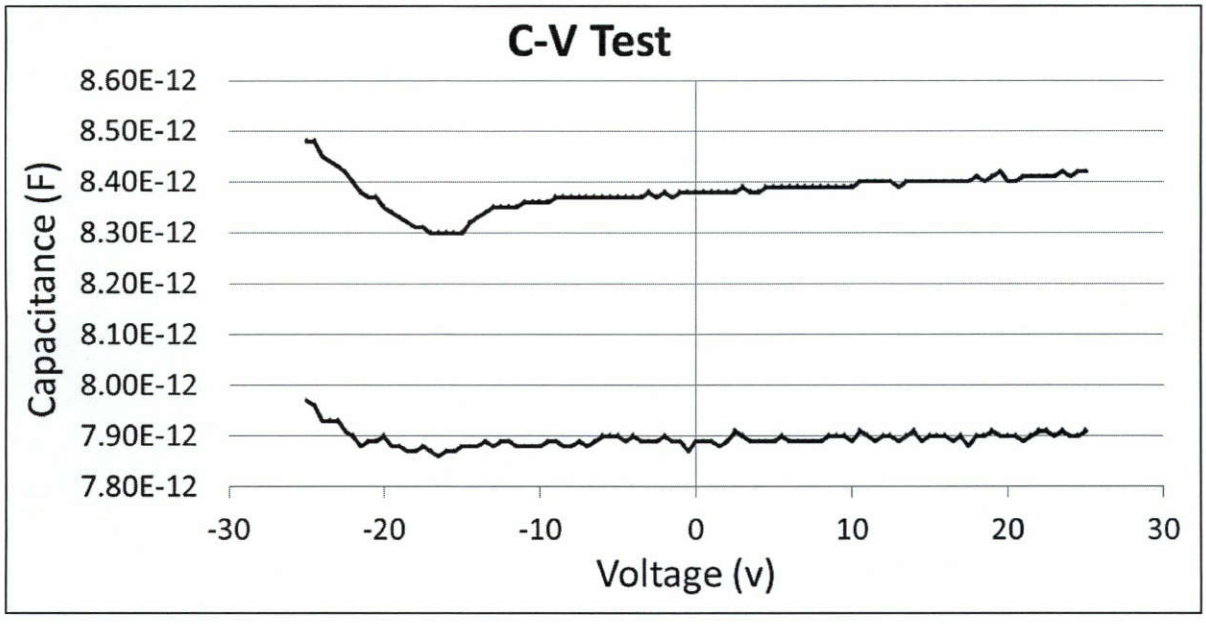

Figure 11: C-V test on amorphous silicon

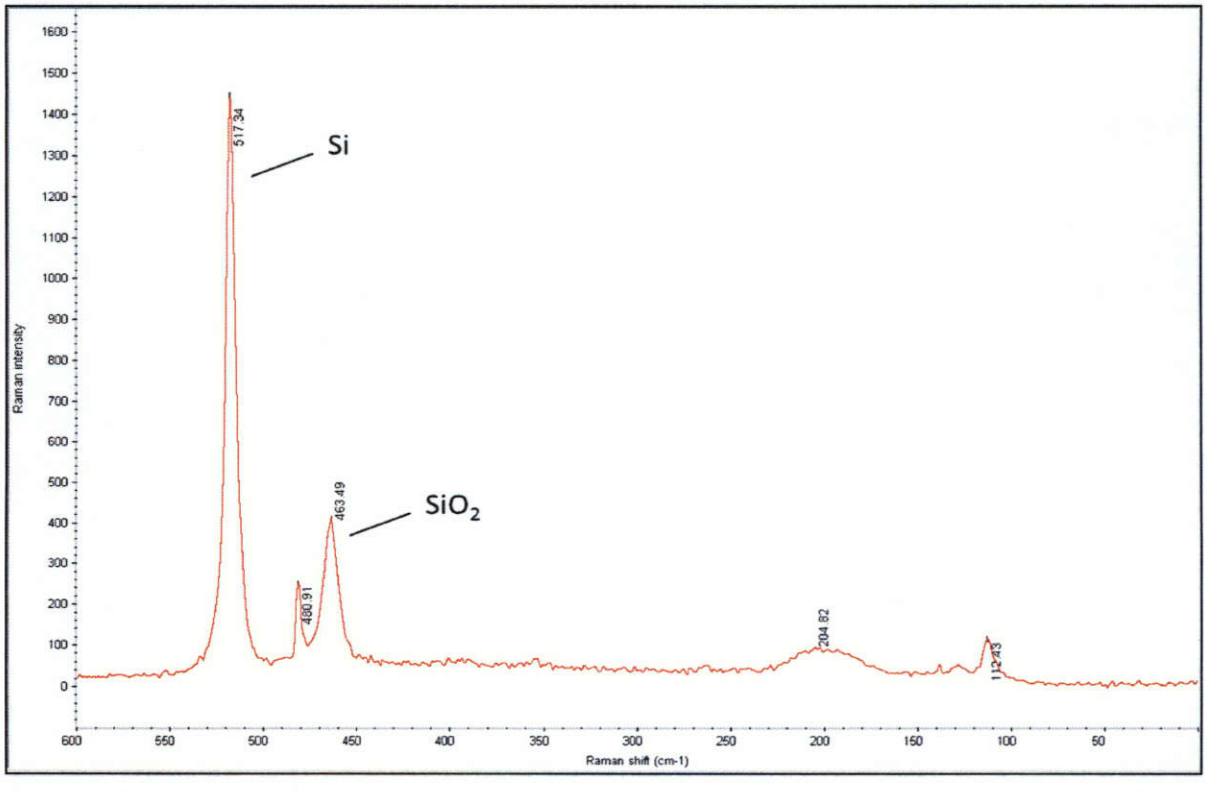

Figure 3: Raman spectroscopy results for silicon nanowire sample

Lastly, we performed Raman spectroscopy on our c-Si NW sample to determine the elements present in the sample and got the graph in Figure 12. The larger spike indicates a presence of silicon, which is to be expected. The smaller spike indicates the presence of SiO_2, which is the oxide layer.

Discussion

Though α-Si is currently one of the most useful thin film materials currently available for bolometer applications, it has limitations. α-Si has a high resistivity, which reduces its sensitivity. Also, it has a significant low frequency noise problem. Though experiments with doping have reduced this issue, they have created other issues, reducing the effectiveness α-Si. By mapping out the electrical and mechanical transport properties of α-Si, in addition to those of c-Si NWs, we have set the stage for testing the proposed hybrid nanocomposite structure. The results presented in this paper will enable future researchers to determine whether a hybrid nanocomposite structure would indeed be a viable improvement over α-Si for bolometer applications.

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