SINGLE PASS COLLIDER MEMO CN-375

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TITLE: LINAC BPM MODIFICATION PROGRAM STATUS*

In the fall of 1988 the BPM Task Force recommended (see "BPM Task Force Progress Report", 28 Oct. 1988) that linac BPM processors be pulled out of the linac, modified, adjusted for offsets, recalibrated, and reinstalled. As of the end of 1989 this process had been completed on all linac type BPM processors.

Modifications and tests included:

1. Attenuation of a factor of 2 has been inserted into the Sum channel to allow higher intensities and improved precision. The attenuation is in front of the point where the sum channel signal is split for calibration of the ratio of gains of the difference channels to the sum channel. The modified processors calibrate as before, but a factor of one-half must be inserted into the calculation of beam position from the ratio of difference to sum channel counts to compensate for the extra attenuation in the sum channel. A modification was made to BPM software to apply the proper scale correction based on processor module type. Modified processors respond to a CAMAC F3 A1 with module type 1 (bit 10 set) for model 605 BPM processors and with module type 5 (bits 10 and 12 set) for model 972 BPM processors. As the upgrade program is now complete all linac BPM processors should be of either type 1 or 5; any other value in the module type field means the module is broken and must be replaced.
2. The track and hold sampling capacitor has been changed from 100pF to 50 pF to reduce saturation effects for large sampled voltages. Saturation had been visible at the high end in some modules.
3. Input rf filters were trimmed to give less than 30 micron offsets when tested on the lab bench.
4. The measured residual offsets averaged over beam polarity and intensity were entered in the offset registers of the processors. The range of measured offsets of a module for both polarities for equivalent beam intensities in the range 0.5×10^{10} to 2.5×10^{10} was less than 100 microns.

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A post-installation test of a sample of processors was done to check the effectiveness of the modification procedures. The cables from the striplines were disconnected from the processor and replaced by the output of a four-way splitter whose input comes from a single stripline. This gives a set of inputs to the BPM processor which correspond to a centered beam of one half the beam intensity. The splitter was checked for precise amplitude balance to better than 0.1%. The BPM is then recalibrated for the appropriate beam intensity and is read out through the normal SCP. We measured electronic offsets in this manner for 28 BPM processors in linac sectors 22, 25, 26, and 27. The resulting distribution are independent of beam charge. Averaged over both beam charges they show rms widths of 65 microns in both X and Y. Therefore the rms displacement error (in two dimensions) is approximately 90 microns about the mean measured position.

The mean offset is significantly different from zero implying a systematic difference between the offsets measured on the bench and that measured in the linac. There is a bias in either the bench calibration procedure or the operating configuration in the linac which results in a systematic mean offset of -90 microns in X and +95 microns in Y. When the beam is centered in the linac the average BPM indicates that the beam is south of and below the linac centerline. This systematic shift dominates the residual random electronics errors. This bias has been removed by entering the average BPM processor offset into the database for all BPM's. The systematic offset is added to the (currently zero) values in the secondary BPMS OFFS.

Conclusions

The modification program is complete. Average offset errors can be reduced to 90 microns (rms). The system (barely) meets the goal of 100 micron rms position measurement.

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