DIP COATING PROCESS

Quarterly Report No. 3, March 19, 1976--June 18, 1976

J. D. Heaps
R. B. Maciolek
M. W. Scott
H. A. Wolner
L. D. Nelson

June 28, 1976

Work Performed Under NASA Contract NAS7-100

Honeywell Corporate Research Center
Bloomington, Minnesota

MASTER

ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Energy Research and Development Administration, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161

Price: Paper Copy \$4.00 (domestic)
\$6.50 (foreign)
Microfiche \$2.25 (domestic)
\$3.75 (foreign)

DIP COATING PROCESS

Silicon Sheet Growth Development
for the Large-Area Silicon Sheet
Task of the Low-Cost Silicon Solar
Array Project

Quarterly Report No. 3

by

J. D. Heaps, R. R. Maciolek, M. W. Scott, H. A. Wolner,
and L. D. Nelson

Period Covered: 3/19/76 - 6/18/76

Published June 28, 1976

Honeywell Corporate Research Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

NOTICE
This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Energy Research and Development Administration, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

This work was performed for the Jet Propulsion Laboratory, California Institute of Tecmology, under NASA Contract NAS7-100 for the U. S. Energy Research and Development Administration, Division of Solar Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

MASTER

JPL CONTRACT NO. 954356
DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

Per

ABSTRACT

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell quality sheet silicon by dip-coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon.

Of the various substrate materials dip-coated this reporting period, mullite appears, at this time, to best satisfy the requirements of this research program.

Dip-coating experiments continue to demonstrate that layer thickness and grain size are dependent on and can be controlled by pulling rate and melt temperature. Crystalline grains as large as 1 mm wide and 2 cm or more long can consistently be grown in layers 35 to 50 μ meters thick. The silicon-ceramic bond between the substrate and the silicon layer is apparently mechanical in nature. Its intimate contact is achieved over less than 10% of the surface, but is sufficient to provide excellent adherence. Twin and grain boundaries usually run from the substrate to the surface of the layer indicating that the coating mainly consists of single layers of crystals. This characteristic reduces the chances of recombination centers above and below the junction.

Hall measurements indicate the carrier concentration of the dip-coated layers to be an order of magnitude larger than doping levels predicted and the mobility of the layers to be about one-half that of single crystal silicon.

Problems were encountered with junction diffusion, but the cause is believed to be understood, thus providing an immediate solution.

A superior method for making electrical contact to the base layer of future solar cells has been conceived. By experimentally demonstrating that silicon will seep through narrow cracks in the substrate to its back surface when dip-coated, it is possible to utilize this principal to contact the base layer.

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
SUMMARY	1
INTRODUCTION	3
TECHNICAL DISCUSSION	5
Experimental Dip-Coating Facility	5
Dip Coating Results	6
Silicon Layer Electrical Properties	17
Junction Diffusion	26
Base Layer Electrodes	29
Substrate Development	29
CONCLUSIONS	32
RECOMMENDATIONS	34
NEW TECHNOLOGY	35
PROJECTED FOURTH QUARTER ACTIVITIES	36
PROGRAM STATUS UPDATE	38

LIST OF FIGURES

	<u>Page</u>
Fig. No. 1 Silicon Melt Thermocouple Configuration	7
Fig. No. 2 Silicon-Ceramic Interface (Unetched) of Substrate MR-8	15
Fig. No. 3 Etched Cross Section of Substrate MR-9	16
Fig. No. 4 EDAX analysis of Samples from Substrates MR-1 and MR-7	18
Fig. No. 5 Carrier Concentration and Resistivity vs. $1000/T(^{\circ}K)$	22
Fig. No. 6 Mobility vs. Temperature ($^{\circ}K$) for Sample MR-7-x and a Single Crystal	23
Fig. No. 7 Solar Cell Characteristics Typical of Past Solar Cell Work	27
Fig. No. 8 Solar Cell Characteristics of Control Cell A-19	28
Fig. No. 9 Initially Proposed Solar Cell Electroding Method	30
Fig. No. 10 Recent Proposed Base Layer Electroding Method	31
Fig. No. 11 Updated Program Plan	39
Fig. No. 12 Updated Program Labor Summary	40
Fig. No. 13 Updated Program Cost Summary	41

LIST OF TABLES

	Page
Table No. I Summary of Dip-Coated Growth Data	9
Table No. II Evaluated Dip-Coated Growth Data	13
Table No. III Summary of 300°K Electrical Properties	20
Table No. IV Summary of Techniques for Evaluating Dip-Coated Silicon	24
Table No. V. Summary of Techniques for Evaluating Dip-Coated Silicon (continued)	25

SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon.

During this reporting period 26 ea. additional substrates have been dip-coated with varying degrees of success on the following types of substrate material:

- Mullite
- 96% alumina
- 85% alumina
- Zirconia silicate
- Calcium aluminate bound alumina
- Hot-pressed "Fiberfrax"
- High density carbon
- Graphoil (Carborundum 5 mil graphite foil)

Of the ceramic substrates coated, mullite appears to best satisfy the economic and physical properties standards of the program. The possibility of its chemical contaminating effect is being investigated. The other ceramic materials appear to have thermal expansion coefficients somewhat incompatible with silicon. Carbon substrates when left in the silicon melt too long, either dissolve or totally convert to SiC and break away from the undipped portion of the substrate.

Dip-coating facility thermocouple problems have prevented a systematic evaluation of the effect of pulling rate and melt temperature on layer thickness and grain size. Those substrates dipped, however, where temperatures were measured, continue to demonstrate the dependency of layer thickness and grain size on pulling rate and melt temperature. Crystalline grains as large as 1 mm wide and 2 cm or more long can consistently be grown in layers 35 to 50 μ meter thick.

A metallographic analysis of angle-lapped layers reveal that the silicon-ceramic bond is apparently mechanical in nature, formed when molten silicon penetrates the porous substrate. This intimate contact is achieved over less than 10% of the surface but is sufficient to provide excellent adherence of the coating to the substrate. Examination of cross sections of other layers show that twin and grain boundaries usually run from the substrate to the surface indicating that the coating mainly consists of single layers of crystals.

An EDAX analysis made on two silicon coated mullite substrates revealed that within the sensitivity limits of EDAX, only silicon was observed.

Preliminary Hall measurements on samples prepared from coated layers show they in general behave as expected, but that samples doped to produce impurity levels of $5.65 \times 10^{15}/\text{cm}^3$ do, in fact, have impurity levels of about an order of magnitude higher. The mobility of these layers is about one-half that of single crystal silicon, thus resistivity measurements will indicate a higher impurity concentration than actually exists.

Problems occurred in the junction diffusion work. Low surface concentrations were measured on the top phosphorus diffused layer of single crystal wafers. The problem is believed to have resulted from the oxygen gas flow not being sufficiently dry, thereby forming phosphoric acid on the surface of the phosphorus pentoxide diffusant.

It was recently demonstrated that if a small slit is built into the ceramic substrate, that silicon will seep through to the back side of the substrate when dip-coated. This provides a superior method for contacting the base layer of future solar cells.

INTRODUCTION

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The dip-coating methods to be developed are to be directed toward a minimum-cost process with the objective of producing solar cells with a terrestrial conversion efficiency of 10 percent or greater.

By applying a carbon coating to one face of a ceramic substrate, molten silicon can be caused to wet only that carbon coated face and produce uniform thin layers of large grain polycrystalline silicon, thus, only a minimal quantity of silicon is consumed. It has been demonstrated to date, that crystalline grains as large as 1mm wide and 2 cm or more long are possible in silicon coatings as thin as 45 meters. Substructure does exist within these grains, but it has been shown to principally be twinning which is less likely to have the adverse effect on collection efficiency that conventional grain boundaries would ordinarily have. If the dip-coating approach can be shown to produce solar cell quality sheet silicon, it offers an outstanding cost effective way to produce large area inexpensive solar cells. Our investigation to date has shown no reason for us not to believe this to be possible. While the substrate material is believed to be the major cost in the dip-coating approach, it does provide a rigid and strong supportive backing to the sheet silicon. A similar supportive backing must be provided for sheet silicon produced by any method.

The dip-coating method has excellent scale-up potentialities. With this method it is possible to coat several wide, large-area substrates in one dipping. An alternative plan would be to dip-coat in a continuous manner linked large-area substrates. This investigation has shown that as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore as the substrate length is increased, (as would be the case in a scaled up process) the expectancy for larger crystallites increases.

Since the inception of this program an experimental dip-coating facility was designed and constructed and using this facility 29 ea. $2\frac{1}{2}$ " x 2" x ~0.05"

substrates fabricated from a variety of materials have been dip coated with silicon. All but three of these substrates were coated during this past reporting period, therefore the remainder of this document will address itself to reporting the results and conclusions of this work.

TECHNICAL DISCUSSION

EXPERIMENTAL DIP-COATING FACILITY

As reported in Quarterly Report No. 2, the original design for installing the "After-Heater" directly above the silicon melt had to be modified to overcome a possible carbon crucible holder breakage problem during the facility shut-down operation. To ensure that the carbon crucible holder will not be broken when the quartz crucible expands and breaks during the solidification of the silicon melt, the quartz crucible containing the molten silicon is raised out of its carbon holder at shut-down time. This made it necessary to reposition the "After-Heater" by an externally controlled lever. This modification has been completed and this "After-Heater" feature is now available for our use.

Following the first successful run (No. 7) of the facility where substrates were actually dip-coated and the run went well, problems with both the heater and melt temperature measuring thermocouples (T.C.) began to occur. The platinum-platinum + 13% rhodium T.C. wires were contained in mullite T.C. insulator tubes with quartz thimbles placed over the hot junctions. These thimbles were to protect the heater T.C. from reacting with carbon and the melt T.C. from dissolving after being immersed into the molten silicon. After experiencing two successive failures, the platinum T.C. wires were given an EDAX analysis which revealed that the platinum wires at and near the T.C. junction were combining with silicon to form a eutectic melting point less than that of silicon. Discussions with the McDanel Corp. made it clear that silicon is given up by mullite T.C. tubing at temperatures in excess of 1350°C. Thus they are not compatible with platinum at or near the melting point of silicon.

In an effort to solve the problem, 99.8% alumina T.C. tubing and thimbles were procured from McDanel and used to replace both the heater and melt T.C.'s. Subsequent dip-coating runs have demonstrated that the heater T.C. is now reliable, but that the melt T.C. is still a potential problem. The melt T.C. is designed to be lowered into the melt once the silicon has become

molten. Its function is one of significant importance since it more readily responds to small temperature changes in the melt than does the heater T.C. Unfortunately it is located in an environment of silicon vapors.

As such after two or three successive runs, silicon vapors apparently again combine with the platinum thereby perpetuating the previously described eutectic melting point problem. An effort will be made to seal off these vapors by stuffing platinum foil in the space between the T.C. tubing and the alumina thimble which shrouds it. (See Fig. 1) Larger diameter T.C. wire will also be used to more nearly fill up the T.C. tubing feed-through holes.

DIP-COATING RESULTS

As previously discussed a carbon coating must be placed upon the ceramic substrate as a medium for causing the silicon to wet the substrate when dipped into the molten silicon. To date, the following methods for applying this carbon coating have been explored:

1. Rubbing ultra pure carbon over one surface of the substrate with a scrubbing action.
2. Applying carbon soot to one surface of the substrate using an acetylene torch.
3. Applying black Aqua-Dag to one surface of the substrate and subsequently firing it at 900°C in an argon atmosphere.
4. Applying a liquid coating of pure acrylic (which had been dissolved in 1-2 Dichloroethane ($C_2H_4Cl_2$) to one surface of the substrate followed by a 900°C firing in an argon atmosphere.

Of the above listed methods, only the rubbed carbon and carbon sooted techniques have been actually dipped into silicon. The rubbed carbon technique (as previously reported) promotes excellent wetting and the soot produced only spotty wetting. The Aqua-Dag flaked off the substrate following the 900°C firing and the pyrolyzed acrylic produced a coating believed to be too thin

Figure 1. Silicon Melt Thermocouple Configuration

to effect wetting. Additional or perhaps heavier coatings of acrylic solutions may produce thicker carbon coatings. On the other hand, since these pyrolyzed acrylic coatings have not yet been dipped into silicon, there is no positive proof that they too, as applied, will not promote satisfactory wetting.

To date, Table I lists a variety of substrates which have been dip-coated with varying degrees of success. All of the materials listed withstood the thermal shock of being immersed into molten silicon with a relatively short preheat cycle prior to their immersion. Of those listed, the McDanel MV-20 mullite plastic composition, which was rolled dried and fired at 1640°C by Honeywell's Ceramics Center, stands out as a strong favorite at this time. This ceramic, as a substrate, has already been shown to satisfy two out of three important criteria for being defined as a suitable candidate for the dip-coating process. Its unique and cost effective fabrication process is believed to satisfy the long range economic goals of JPL's Low-Cost Silicon Solar Array Project and its thermal expansion coefficient ($5.0 \times 10^{-6}/^{\circ}\text{C}$) is sufficiently compatible with that of silicon. No obvious stress or strain has been evident, to date, in either the silicon coating or the substrate. The third important criterion, for which this form of mullite must satisfy, is the extent to which its chemical composition will influence the purity of the silicon coated upon it. This criterion is also being investigated.

Of the two types of alumina substrates listed, namely; 96% and 85% alumina, the 96% alumina appears least likely to accommodate the dip-coating process. The 96% alumina has a thermal expansion coefficient of about $6.7 \times 10^{-6}/^{\circ}\text{C}$, which represents a rather substantial mismatch with silicon. 96% alumina substrate No. A95-1 was dip-coated without a routine substrate cleaning process for the purpose of testing its resistance to thermal shock. Because of the uncleanness of its surface only a spotty silicon coating was achieved. As such, no visible signs of cracking took place. 96% alumina substrate No A95-2, on the other hand, was cleaned and fired prior to dip-coating it with silicon. The dip coating exercise produced a smooth 100 μmeter thick layer as viewed through the viewing port of the dip-coating facility. This layer, however,

TABLE I. SUMMARY OF DIP-COATED GROWTH DATA

SUBSTRATE NO.	RUN NO.	SUBSTRATE MATERIAL	PULLING RATE (Cm/Sec)	MELT TEMP. (°C)	LAYER THICKNESS (μ Meter)	LAYER AVE ρ (Ohm-Cm)
MR-1	7	Mullite ⁽¹⁾	0.12	1434	45	1.8
MR-2	7	"	0.33	1426	8-10	0.49
MR-3	7	"	0.33	1410	15-125 ⁽²⁾	0.7
MR-4	8	"	0.1	TCF ⁽³⁾	~15	0.64
MR-5	8	"	0.1	"	Given to JPL	
MR-5A	8	"	0.1	Substrate froze in melt		
MR-6	9	"	0.35	TCF ⁽³⁾	~8	0.77
MR-7	9	"	0.284	"	32-37	0.82
MR-8	10	"	0.233	1411	25-38	1.34
MR-9	10	"	0.1	1426	50	0.52
MR-10	11	"	0.155	1436	10	0.047
MR-11	11	"	0.086	1436	45	0.47
MR-12	11	"	0.054	1455-1457	25-37.5	1.7
MR-13	11	"	0.064	1412	279	1.12
MR-14	11	"	0.084	1439	N.M.	N.M.
MR-15	12	"	0.17	1441	N.M.	N.M.
MR-16	12	"	0.085	1448	N.M.	N.M.
MR-17	13	"	0.104	1433	N.M.	N.M.
MR-18	13	"	0.0933	1437	N.M.	N.M.
A95-1	7	ALUMINA ⁽⁴⁾	0.1	1444	~125	4.6
A95-2	9	"	0.1	TCF ⁽³⁾	SUBSTRATE	SHATTERED
A85-1	10	ALUMINA ⁽⁵⁾	0.175	1419	~50	N.M.
Z-1	12	See Note ⁽⁶⁾	0.085	1437	N.M.	N.M.
CA-1	12	See Note ⁽⁷⁾	0.097	1437	N.M.	N.M.
FF-1	13	See Note ⁽⁸⁾	0.117	1456	N.M.	N.M.
C-1	9	Carbon	0.109	TCF ⁽³⁾	N.M.	N.M.
C-2	10	Carbon	BROKE IN SILICON MELT			
C-3	10	Carbon	0.175	1416	N.M.	N.M.
G-1	11	"Graphoil"	0.175	1439	N.M.	N.M.

(1) McDanel MV-20 Rolled, Dried and Fired

N.M. - not measured

(2) Dendrites protrude above surface

(3) Thermocouples failed

(4) 96% Alumina

(5) 85% Alumina

(6) Zircon (Zirconia silicate - $ZrO_2 \cdot SiO_2$)

(7) Calcium Aluminate-bound Alumina

(8) Carborundum pressed "Fiberfrax"

prior to being removed from the dip-coating facility, shattered upon cooling apparently because of its thermal expansion mismatch with silicon. Prior to this contract program, a much thinner (~ 15 μ meter) silicon coating was successfully placed on a high purity alumina substrate, therefore 96% alumina, at this time, cannot yet be ruled out as a possible substrate candidate. Even though it may be possible to apply a thinner coating, or thicker coating for that matter, and keep the substrate intact by a controlled cooling cycle, the evidence remains that the resulting silicon coatings are likely to be highly stressed. This stress is likely to introduce excessive dislocations within the silicon.

An ~ 50 μ meter silicon coating was placed on an 85% alumina substrate and the substrate remained intact. Even though 85% alumina has a somewhat smaller thermal expansion coefficient than 96% alumina, there was still evidence of the silicon layer being strained. At the top of the substrate larger dendrites protruded above the main surface coating. As the substrate continued to be pulled from the melt the heat flow or melt temperature became such as to produce a smoother coating. In any event, in the region of these protruding dendrites, again it was observed that tiny chips of silicon flaked off of these protruding dendrites. This again is probably due to the existing thermal expansion mismatch. The existence of larger dendrites protruding from the surface followed by a smooth coating is not unique to this 85% alumina substrate. It has also happened under similar growth conditions with mullite substrates, but never have portions of the larger dendrites flaked off as they did on Substrate No. A85-1.

Zircon Substrate No. Z-1 is a zirconia silicate ($\text{ZrO}_2 \cdot \text{SiO}_2$) compound with a melting point of 1530°C and a thermal expansion coefficient of $6.0 \times 10^{-6}/^\circ\text{C}$. The silicon coating applied to this substrate also manifested a thermal expansion mismatch by having portions of the silicon coating flake off. There was no observable cracking in the substrate itself, but small (~ 0.5 mm) blisters formed on both sides of the substrate. In spite of these blisters rather large 1 mm x 2 cm grains were observed with the longer dimension, as usual, being aligned along the direction of growth.

Substrate CA-1 is a calcium aluminate bound alumina. The silicon coating very poorly adhered to this substrate. In addition to having large portions of the layer flake off, several cracks occurred in the substrate. On the basis of one coated substrate, this material would have to be rated as a poor candidate with respect to its compatibility with the dip-coating process.

Substrate No. FF-1 was fabricated by the Honeywell Ceramics Center from Carborundum "Fiberfrax." Fiberfrax is made up of mullite fibers. Sheets from which the above 2½" x 2" substrate was cut were formed by hot pressing (1400°C) double or triple layers of Fiberfrax (0.05" thick carborundum sheet). Flat, very porous but rigid sheets 0.04" to 0.06" thick with a density of 0.5 gm/cm³ were formed by this process.

The typical carbon coating technique of rubbing or scrubbing ultra pure carbon over one surface could not be used for this substrate due to its softness. Therefore, high purity carbon powder was poured on one surface and worked into the pores by rubbing the surface with a clean cloth. The results of the dip-coating process were somewhat surprising. Silicon did not coat the face of the substrate on which the carbon powder was applied, but oddly, a very thin coating of silicon occurred on the opposite face. Whether the silicon was wetted by the carbon and subsequently passed through the porous substrate to the opposite face by some wicking action or whether silicon will wet pressed-mullite fibers without the aid of carbon is not known at this time.

Substrates Nos. C-1, C-2 and C-3 were machined from high density carbon to the dimensions of 2½" x 2" x 0.015". The crystalline structure observed on substrate C-1 differed from the usual narrow, long dendritic type structure observed on all the ceramic backed coatings. This, as suggested by Dr. Martin Leipold of JPI., may result from the larger thermal conductivity of carbon as opposed to ceramic materials. This increased thermal conductivity could alter the heat flow pattern that customarily occurs with ceramic substrates.

Substrate No. C-2 cracked upon being immersed into the melt and pieces of the carbon initially floated on the surface of the melt. It is interesting to note that in a time frame of 2 to 3 min, these pieces of carbon were either dissolved into the silicon solution or were completely converted to SiC and sunk to the bottom of the melt. In any case, if thin wafers of carbon were to be considered as a substrate material for the dip-coating process, further consideration would have to be given to the length of time one is allowed to dip and pull from the melt.

Substrate No C-3 was given to JPL prior to any analysis.

A 5" x 2" piece of 5 mil "Graphoil" was wrapped around a 2½" x 2" x 0.05" mullite substrate and dip-coated with silicon. It was designated as substrate No. G-1. Graphoil is a product of Union Carbide and is a graphite foil that can be purchased in a number of thicknesses. G-1 was dipped and pulled from the melt allowing no soaking time in the melt. A thin coating of silicon occurred only on the exposed surfaces; unlike carbon substrate C-1, G-1 had long, narrow crystalline grains which were dendritic by nature and very similar to the size and type one would expect on a ceramic substrate coated under similar conditions.

As discussed in a previous portion of this report, we experienced thermocouple problems with the dip-coating facility. These problems have made it impossible to evaluate in a systematic manner the effect of pulling rate and melt temperature on layer thickness and grain size. Table II does, however, summarize data taken on a few silicon coated mullite substrates where the temperature measurements were fairly reliable. While this does not provide a systematic evaluation of the effect of pull rate and melt temperature on layer thickness and grain size, it does confirm the trend that the silicon coating thickens as the pulling rate or melt temperature decrease. It also was observed that grain sizes are generally larger in the thicker layers. This is not to say, however, that given an optimized set of growth parameters that large grain sizes cannot be made to occur in the thinner layers. As shown in Table II, substrates MR-2 and MR-9 were both dip-coated at a melt

TABLE II. EVALUATED DIP-COATED GROWTH DATA

SUBSTRATE NO.	RUN NO.	SUBSTRATE MATERIAL	PULLING RATE (Cm/sec)	MELT TEMP. (°C)	LAYER THICKNESS (μ METER)	LAYER AVE. ρ (ohm-Cm)
MR-1	7	Mullite*	0.12	1434	45-50	1.8
MR-2	7	"	0.33	1426	8-10	0.49
MR-8	10	"	0.233	1411	25-38	1.34
MR-9	10	"	0.1	1426	50	0.52
MR-10	11	"	0.155	1436	10	0.047
MR-11	11	"	0.086	1436	45	0.47
MR-12	11	"	0.054	1455 1457	37.5 25	1.7
MR-13	11	"	0.064	1412	279	1.12

* McDanel Corp. MV-20 Rolled, Dried and Fired

temperature of 1426°C. MR-2 was pulled from the melt at a rate 3.3 times that of MR-9 and thus had a layer thickness of only 0.16 to 0.2 that of MR-9. Substrates MR-10 and MR-11 were dip-coated at a melt temperature of 1436°C. Similarly MR-10 was pulled at a rate of 1.8 times that of MR-11 and as such had a layer thickness of only 0.22 that of MR-11. Likewise substrates MR-3 and MR-13 were pulled from the melt at similar temperatures 1411°C and 1412°C respectively. MR-8's pulling rate was 3.64 times that of MR-13 and again had a thickness of only about 0.1 that of MR-13. It is interesting to note that as the melt temperature is reduced the coating thickness difference appears to increase for similar differences in pulling rates.

A metallographic analysis was made on substrate nos. MR-8 and MR-9.

Cross sections of silicon films formed by the dip-coating process were prepared and examined using standard metallographic procedures. The sections were cut perpendicular to the pulling direction. The samples were etched with CP-4 to delineate grain and twin boundaries.

Fig. 2 shows the silicon-ceramic interface of substrate MR-8, unetched. The silicon-ceramic bond is apparently mechanical in nature, formed when the molten silicon penetrates the porous substrate. This intimate contact is achieved over less than ten percent of the surface, but is sufficient to provide excellent adherence of the film to the substrate. The black areas between the silicon and ceramic are actually holes where unreacted carbon was pulled out during polishing.

Fig. 3 shows a typical etched cross section of substrate MR-9 revealing twin and grain boundaries. Examination of such cross sections showed that the twin and grain boundaries usually ran from the substrate to the surface indicating that the film consisted mainly of a single layer of crystals. In a few instances some over growth was noted in small portions of the film, in which case that portion of the film consisted of two or three crystals on top of each other. A similar metallographic analysis was performed by Dr. Martin Leipold of JPL with very similar results and conclusions.

(200X) $\longrightarrow$ $\left| \right| \longleftarrow$ 50 μ

Figure 2- Silicon-Ceramic interface (Unetched) of Substrate MR-8

(100X) $\longrightarrow \quad \left| \quad \left| \quad \longleftarrow$ 100 μ

Figure 3- Etched Cross Section of Substrate No. MR-9

Since there are relatively few boundaries which run parallel to the surface of the silicon layer, this condition in a solar cell configuration should greatly reduce the number of recombination centers for photon generated hole-electron pairs generated above or below the space charge region.

SILICON LAYER ELECTRICAL PROPERTIES

As a quick check to ascertain whether or not the coated layers were being grossly contaminated by the mullite substrate, an EDAX analysis was performed on samples from substrates MR-1 and MR-7. Fig. 4 clearly shows that within the limits of an EDAX chemical analysis, only silicon is present.

Earlier in the program, based on relatively few samples, a pattern appeared to develop which indicated that the resistivity of thicker silicon coatings (as measured by the 4 point probe method) was generally larger than the resistivity of thinner coatings. Since the 4 point resistivity probe measurements were valid only for layers placed on insulators, it was for a period of time, postulated that the silicon carbide (SiC) film between the substrate and the silicon coating was contributing to the overall electrical conduction of the layer. As additional samples were measured and with the metallographic analysis revealing the discontinuous nature of the silicon-substrate interface, this postulate is probably in error. Examination of the average resistivity data shown in Tables I and II also tend to refute this original resistivity-layer thickness trend. The SiC and free carbon which appears to exist in islands at the silicon-substrate interface may yet, in some complex way, affect the conductivity of the coating. This effect, however, is not likely to be in a straightforward manner. These islands of SiC and carbon could, in fact, play some part in the nonuniform resistivity measured over the surface of large area coatings.

Since the primary means for determining the doping levels of these dip-coated layers has been with the 4-point resistivity probe, consideration was given to evaluating these layers using Hall measurements. The 4-point probe technique gives an accurate measure of resistivity if the thickness of the layer is known, but the carrier concentration is obtained by assuming that

MR-1

MR-7

Figure 4- EDAX Analysis of Samples from Substrates MR-1 and MR-7

the mobility in the polycrystalline layers is the same as in single crystal silicon. This assumption, in general, is not valid therefore 3 ea. Hall samples were prepared from two dip-coated substrates (MR-1 and MR-7). In addition to these 3 samples an additional Hall sample was prepared from a silicon melt (Run No. 8) which had only mullite substrates dipped into it. This particular melt did, however, have the final mullite substrate solidify around it and remain in the melt through the facility shut-down procedure. Of the 3 samples prepared from dip-coated layers, 2 of them were prepared from substrate MR-7 which also had the melt surface solidify around it. This required it to soak in the melt for 9 minutes before remelting and temperature equilibrium could be established. As such, the samples prepared from MR-7 could represent a "worst case" example as far as time allowed for the substrate to contaminate the silicon coating. The remaining substrate was prepared from substrate MR-1 which represents a more typical time in which the substrate is in contact with the molten silicon.

Preliminary measurements have been made on these three dipped layers and the one bulk polycrystalline sample taken from melt No. 8 to determine first, if the resistivity measurements can be used to determine the carrier concentration, and second, how the carrier concentration in the layers compares with the starting concentration in the melt.

These Hall samples were prepared from the layers by masking the sample configuration and sand blasting the remaining silicon from the substrate. The samples were about 1 cm long, .1-2 mm wide with the voltage side arms about 5mm apart. Contacts were made by evaporating Al and alloying at 750° C for 10 minutes. Electroless Ni was plated over the alloyed Al and In soldered to the Ni. The bulk polycrystalline sample was made in essentially the same manner except the thickness was 0.063 cm, rather than the 40 to 50 μ typical of the layers. The measurements were made in a standard manner using a dc field of 2K Gauss.

A summary of the room temperature measurements is given in Table III. The sample designations MR-7-P and MR-7-X refer to the crystallite orientation in the Hall sample, with "P" meaning the long axis of the grains were parallel to the direction of current, and "X" meaning the long axis of the grains were

TABLE III. SUMMARY OF 300°K ELECTRICAL PROPERTIES.

Sample No.	Carrier Conc. (Cm ⁻³)	Resistivity (Ω-cm)	Mobility (cm ² /V sec)
MR-7-P	6.7 x 10 ¹⁶	.45	208
MR-7-X	7 x 10 ¹⁶	.6	146
MR-1	7.5 x 10 ¹⁶	.54	153
BULK POLY (Melt-8)	1.8 x 10 ¹⁷	.24	146

oriented across the sample, perpendicular to the direction of current. As seen in the Table III, these two samples have slightly different mobilities, with the highest mobility in sample MR-7-P. The mobilities in all four samples is lower than the 250 to 300 $\text{cm}^2/\text{volt sec}$ expected for single crystal material with carrier concentrations in the 0.6 to $2 \times 10^{17}/\text{cm}^3$ range.

The temperature dependencies of carrier concentration, resistivity and mobility for sample MR-7-x are shown in Figures 5 and 6. In general they behave as expected for silicon; the carrier concentration decreases and the resistivity goes through a minimum before increasing as the sample is cooled. The one exception occurs at 77°K where the carrier concentration apparently increases over the 85°K value. The temperature dependence of the mobility is compared with a single crystal sample with a carrier concentration of $2 \times 10^{17}/\text{cm}^3$ in Figure 6. The notable difference is the sudden drop in mobility in the layers at 77°K . No explanation for this decrease is postulated at this time.

An attempt was made to measure the electrical properties of the bulk polycrystalline sample below room temperature, but the results were not sensible and will not be reported here.

Since this bulk sample was prepared from a solidified melt it could likely have had small cracks or voids in it which could explain the anomalies experienced below room temperatures.

The main point to note from these measurements is that the mobility in polycrystalline samples will be lower than in a single crystal sample with the same doping density. As a result, the resistivity measurements will indicate a higher purity, by as much as a factor of two.

The second point is the doping level in the melt after solidification. The crucibles are loaded to produce $2.5 \Omega\text{cm}$ ($5.65 \times 10^{15}/\text{cm}^3$) p-type crystals. The one bulk sample measured indicates a substantially higher value after layers have been dipped. There is some question as to the reliability of these measurements, but the doping level is apparently higher than expected. Further measurements will have to be made on other melts to determine if this occurs regularly. Tables IV and V include possible techniques for evaluating dip-coated layers.

Figure 5 - Carrier Concentration and Resistivity vs. $100/T (^{\circ}\text{K})^{-1}$

Figure 6. Mobility vs. Temperature (°K) for Sample MR-7-x and a Single Crystal

TABLE IV. TECHNIQUES FOR EVALUATING DIP COATED SILICON

<u>Technique</u>	<u>Information and Advantages</u>	<u>Disadvantages or Difficulties</u>
1. Resistivity	<ul style="list-style-type: none"> . Rapid . Non-destructive . Room temperature . Gives carrier concentration 	<ul style="list-style-type: none"> . Limited accuracy . Measures only an average effect . Does not identify impurity . Depends on mobility
2. Hall and Resistivity	<ul style="list-style-type: none"> . Carrier conc. and mobility are separable . Determine total impurity conc. 	<ul style="list-style-type: none"> . Requires specific sample geometry . Temp. dependence required for all information . Measures average effect
3. Differential Hall	<ul style="list-style-type: none"> . Determine parameters of thin layer . Can determine if SiC layer is insulating . Measurements at room temp. 	<ul style="list-style-type: none"> . Requires accurate thinning . Specific sample geometry . Will require many measurements per sample
4. I-V Characteristics	<ul style="list-style-type: none"> . Shunt leakage does not affect forward currents . No special geometry . Estimate minority carrier lifetime 	<ul style="list-style-type: none"> . Series resistance limits range . Does not identify impurities . May not have simple exp. . Mechanism limiting τ not determined

TABLE V. TECHNIQUES FOR EVALUATING DIP-COATED SILICON (continued)

<u>Technique</u>	<u>Information and Advantages</u>	<u>Disadvantages or Difficulties</u>
5. Reverse Recovery	<ul style="list-style-type: none"> . Determine τ . Requires only junction formation . Not limited by shunt resistance 	<ul style="list-style-type: none"> . Requires fast pulse to switch bias . Not specific to impurity . Can be limited by contacts in thin layers
6. Spreading Resistance	<ul style="list-style-type: none"> . Carrier concentration vs. depth . Depth resolution of $\sim 200 \text{ \AA}$ 	<ul style="list-style-type: none"> . Consistent surface preparation . Requires a calibration for absolute measurements . Depends on mobility . Accurate beveling to get depth dependence
7. MOS Recovery	<ul style="list-style-type: none"> . Determine minority carrier generation rate . Measured times much longer than carrier lifetime 	<ul style="list-style-type: none"> . Limited by surface shunting at oxide . Limited by bulk leakage in Si . Requires more elaborate processing . High impedance
8. Photoconductive Response	<ul style="list-style-type: none"> . Sample geometry not critical . Determines response time 	<ul style="list-style-type: none"> . Difficult to measure short lifetimes . Do not necessarily measure lifetime . Light pulse turned off in time less than lifetime
9. Thermally stimulated Currents	<ul style="list-style-type: none"> . Determine deep energy levels . Uses junction structure 	<ul style="list-style-type: none"> . Requires very low shunt leakage . Requires low temperature . Requires extensive modeling to obtain energy levels

JUNCTION DIFFUSION

It is important that we re-establish our expertise in the area of diffusing p-n junctions before diodes or solar cells are fabricated from dip-coated layers. Otherwise the characteristics of these diodes and cells, rather than reflecting their own merit, may become degraded by the diffusion process. Junction depth (x_j) and surface concentration (C_s) of the top layer of solar cells are key diffusion parameters in achieving high conversion efficiencies. The nature of the absorption coefficient, as a function of photon wavelength, dictates that x_j must be shallow if the shorter wavelengths absorbed near the surface are to play a part in the collection efficiency. At the same time this thin layer above the space charge must have sufficient electrical conductivity to not introduce excessive current-limiting series resistance to the cell. Thus C_s must be large and of the order of 3×10^{20} atoms/cm³. A large C_s plays another important role in providing a sharp or abrupt junction which is conducive to maximizing the open circuit voltage (V_{oc}).

Boron was selected to dope the base layer of the dip-coated samples because its segregation coefficient provides a uniform p-type impurity concentration. The logical n-type top layer diffusant then becomes phosphorus. Our diffusion system is set up to diffuse p-type control wafers and/or dip-coated layers in a very dry oxygen gas flow at temperatures of $\sim 975^\circ\text{C}$. Phosphorus pentoxide (P_2O_5) is used as a diffusant and is located in a temperature zone of 2350°C . In our past solar cell work, by using a diffusion time of ~ 18 minutes, we were able to routinely produce single crystal solar cells with conversion efficiencies in the 11 to 13% range. Figure 7 was taken from a report of our past solar cell work and demonstrates relatively good I-V characteristics. Such cells had a C_s of $3 \times 10^{20}/\text{cm}^3$ and had only the advantage of a clear "Krylon" as an anti-reflection coating.

More recently, we have diffused several 5 ohm-cm, p-type single crystal wafers to reacquaint ourselves with this past work. Our initial results have been poor. Figure 8 shows characteristics typical of our recent results using single crystal wafers. An evaluation of these solar cells reveal that they have a low C_s of the order of $2 \times 10^{19}/\text{cm}^3$. It was concluded that the oxygen flow rate was excessive and was beyond the limit of the dryer used. As such, less than dry oxygen was causing the top portion of the P_2O_5 to convert to phosphoric acid which has a much smaller vapor pressure than P_2O_5 . This low

Figure 7. Solar Cell Characteristics Typical of Past Solar Cell Work

Figure 8 - Solar Cell Characteristics of Control Cell A-19

C_s accounts for the large internal cell resistance and low V_{oc} evident in the I-V characteristics shown in Figure 8.

The cause for our recent poor diffusion results is believed to be understood and should be resolved in the near future.

BASE LAYER ELECTRODES

Since the dip-coated layer is being placed on an electrically insulating substrate, contact to the base layer cannot be made in a straightforward manner. Initially it was suggested that contact to the bottom layer would be made via the top layer. This was to be accomplished having interlacing fingers on the top layer of the solar cell which provide contact to both layers as shown in Figure 9. Troughs would be etched or in some other manner cut through the shallow junction to the bottom layer. This method has at least two disadvantages; first, a considerable amount of useful solar radiation area is lost and secondly, it leaves the edges of the space charge region exposed along each trough necessitating a passivation process.

During this reporting period it was demonstrated that it should be possible to make contact to the bottom layer by cutting narrow slits in the ceramic substrate prior to its firing. By doing so the silicon coating will seep through to the back side of the substrate. This side can then be plated and solder dipped in a conventional manner. These slits would be oriented in line with the growth axis in order to least disturb the crystalline layer growth (See Figure 10). Evidence of the possibility of this electroding scheme was demonstrated by dip-coating a mullite substrate which had a long narrow crack in it. Silicon very nicely seeped through the crack to the back side of the substrate.

SUBSTRATE DEVELOPMENT

With the exception of fabricating additional mullite substrates using the previously described rolled, dried and fired method, no further development work was performed during this reporting period.

Figure 9. - Initially Proposed Solar Cell Electroding Method

Figure 10. Recent Proposed Base Layer Electroding Method

CONCLUSIONS

From the efforts of this past quarter of work we have formed the following conclusions:

1. That all the types of ceramic substrates dip-coated, to date, withstand the thermal shock of being immersed into molten silicon.
2. That mullite substrates, fabricated by the Honeywell Ceramic Centers rolled, dried and fired process, appear to economically and physically qualify as a suitable substrate candidate for the dip-coating process. (The extent to which they will chemically contaminate the coating is being studied.)
3. That based on one dip-coated substrate, the larger thermal expansion coefficient of 96% alumina substrates would appear to present a problem particularly for thicker coatings.
4. That again based on one dip-coated layer zirconia silicate and calcium aluminate bound alumina appear to be incompatible with the dip-coating process.
5. That if carbon were to be used as a substrate the dip-coating time would have to be limited in order to preserve this substrate.
6. That the silicon-ceramic bond is apparently mechanical in nature, formed when the silicon penetrates the porous substrate and even though this intimate contact is made over less than 10% of the surface the bond is sufficient to provide excellent adherence of the coating.
7. That crystalline grains as large as 1 mm wide and 2 cm or more long can consistently be grown in layers 35 to 50 μ meters in thickness.
8. That these coatings for the most part have twin and grain boundaries running from the substrate to the surface of the layer indicating that the coating consists mainly of single layers of crystals. (This characteristic should reduce the number of recombination centers above and below the space charge region.
9. That within the sensitivity limits of an EDAX analysis, there is no gross contamination of the silicon coating.
10. That preliminary Hall measurements on samples prepared from coated layers show they in general behave as expected, but that samples doped to produce impurity levels of $5.65 \times 10^{15}/\text{cm}^3$ do, in fact, have impurity levels of about an order of magnitude higher.
11. That the mobility of these coated layers is about one-half that

that of single crystal silicon and thus resistivity measurements will indicate a higher impurity concentration by as much as a factor of two.

12. That the reliability of the Hall measurements made on the bulk sample from Silicon melt No. 3 is in question.
13. That our recent poor junction diffusion effort results from not sufficiently drying the oxygen which flows through the diffusion furnace.
14. And finally that through the use of slits in the ceramic substrate, electrical contact can be made to the base layer on dip-coated solar cells.

RECOMMENDATIONS

A review of the program's current status resulted in the following recommendations:

1. That while the physical properties of the present dip-coated layers show solar cell material potentialities, that in the near future a systematic study of the effects of pulling rate and melt temperature on layer thickness and grain size should be performed.
2. That the extent to which the chemical and physical properties of the layer will contribute to, or detract from the solar cell quality of the coated layer should be given our immediate attention.
3. That resistivity and minority carrier lifetime of the material are probably the most important electrical characteristics for obtaining a quick determination of the coated layer's potential solar cell quality.
4. That the tasks outlined in the "Projected Fourth Quarter Activities" section of this report should have top priority in responding to the above recommendations.

NEW TECHNOLOGY

During this reporting period there were two techniques developed which are believed to be technological firsts and could have an impact on the program's future. They are the following:

1. By dip-coating a mullite substrate having a narrow crack in it, it was demonstrated that silicon will seep through to the back side of the substrate. By preparing substrates with slits in them, as shown in Figure 10, a new method is available for making contact to the base layer of solar cells.
2. Dip-coated layers of silicon were placed on 5 mil thick "Graphoil." Graphoil is a product of Union Carbide and is a graphite foil available in several thicknesses. Pending its economic feasibility, it may qualify as an alternative substrate material.

PROJECTED FOURTH QUARTER ACTIVITIES

In response to the previous recommendations the tasks which will be pursued during the forthcoming quarter are as follows:

1. Material Evaluation

- a) Consideration will be given to having an independent laboratory perform a trace analysis on dip-coated samples using ion beam mass spectroscopy.
- b) A SEM analysis will be made on an angle-lapped sample to profile its electrical conductivity utilizing the magnitude of the beam current.
- c) An electrical conductivity profile will also be made on angle-lapped samples using the spreading resistance method (Honeywell's Solid State Electronics Center will perform this work.)
- d) Once the diffusion process problems are eliminated, a simple matrix of mesa diodes will be prepared on several dip-coated layers. This will be done in such a way that diodes will be formed on single crystal grains of the layer. Lifetime (τ) measurements will be made using the Reverse Recovery technique. Similarly I-V characteristics will be made on photo diodes with the objective of determining the collection efficiency and V_{oc} .
- e) Solar cells will be made together with single crystal control sample to ascertain what efficiencies are possible in these preliminary coated layers.
- f) If time permits spectral response measurements will be made on mesa type photo diode prepared on coated layers along with control samples to examine the cut-off wavelength differences. (This would provide another way of comparing single crystal and dip-coated layer τ 's)

2. Layer Growth

- a) Perform a systematic study to show the effects of pulling rate and melt temperature on layer thickness and grain size. (This

study will be conducted on mullite substrates which have been carbon coated using the "scrubbed ultra pure carbon method.")

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 11, 12 and 13.

NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE RESEARCH CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

△ - PLANNED GOALS
▲ - ACCOMPLISHED GOALS

* STARTING DATE 10/21/75

Figure 11. Updated Program Plan

Figure 12. Updated Program Labor Summary

Figure 13. Updated Program Cost Summary