**A CHARGED PARTICLE DETECTOR SYSTEM FOR THE MPS
AND ISABELLE SPECTROMETERS**

Edward D. Platner

October 11, 1976

NOTICE
This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Energy Research and Development Administration, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights.

INFORMAL REPORT

**BROOKHAVEN NATIONAL LABORATORY
ASSOCIATED UNIVERSITIES, INC.**

Upton, New York 11973

**under contract No. EY-76-C-02-0016 with the
UNITED STATES ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION**

MASTER

A CHARGED PARTICLE DETECTOR SYSTEM FOR THE MPS
AND ISABELLE SPECTROMETERS

Edward D. Platner
Physics Department, Brookhaven National Laboratory

A detector system combining the good time resolution and low dead time of PWC's and the good space resolution of drift chambers is proposed to upgrade the MPS and for future use in Isabelle spectrometers. Central to this detector is the development of two integrated electronic circuit systems. This paper will describe the detectors with special emphasis on the electronic systems. The detector system proposed here will be capable of handling particle flux rates typical of conventional PWC's yet providing a spacial resolution of 100 μm . Another advantage is that a large area detector of such performance will become technically feasible as well as economically viable.

The Detector

The detector is a conventional narrow anode spacing drift chamber with field wires (Fig. 1). By using an anode spacing of 4mm, the maximum drift distance is 2mm which with Argon-Isobutane (70:30) gives a maximum drift time of 50ns. Thus the resolving time is typical of conventional PWC's. Since the drift space is small, corrections required for the effects of magnetic fields, if any, will be small. These chambers will be configured as sets of planes with anode wires along x, y and 45° in a single gas envelope. Cylindrical versions will be constructed to surround the target with axial anode wires. In this case the image current on

the cathodes with radial and helical strips will also be read out to give three dimensional stereo.

Construction of these chambers is expected to be simple since large amplifications can be obtained with relatively low voltage between anode plane and cathode resulting in manageable electrostatic forces and the field wires help reduce the tendency toward electrostatic instability.

The Electronics

A close anode spacing drift chamber detector system has clear advantages in high rate experiments over conventional drift chambers or delay line readout PWC's. This advantage is gained, however, at the expense of increased numbers of independent electronic readout channels. Thus it is particularly important to develop electronics that are highly reliable as well as inexpensive. The electronics for each wire consists of two sections: an amplifier-shaper-discriminator section and a digital delay-time encoder section.

The amplifier-shaper-discriminator will be a hybrid IC using existing IC chips, Fig. 2 and Table I. Thus performance and reliability are already known. It is anticipated that 8 channels can be housed in a single electrostatically shielded package. This is a hybrid version of the PWC readout currently in use at BNL with successful results.

The digital delay-time encoder circuit¹ is the heart of this detector system. The development of this circuit will require state-of-the-art technology such as D-MOS. It is expected that a substantial development and engineering cost will be involved. The circuit consists of a

90 stage shift register followed by a 16 bit shift register (Fig. 3). The shift registers which are clocked at 100 MHz will be stopped 1000 ns after an event of interest has been detected. At this time the clock is stopped and the time history of the detected event over a 160 ns interval is held in the 16 bit shift register. Since the registers were clocked at 10 ns intervals, this history is quantized in 10 ns (implies 400 μ) intervals. Thus the 16 bit register gives 400 μ full width position information. Some time after the clock is stopped, control logic rearranges the 16 bit shift registers so that all of the 16 bit pieces are in series. To read out the data the clock is turned back on and the data for the whole chamber comes out serially on one line. This serial data retrieval cycle can proceed at 100 MHz so that each wire requires 160 ns to transmit the data to the encoding circuitry.

Drift chambers of this wire spacing are capable of a standard deviation of 80 μ resolution due to electron diffusion. For some applications it makes sense to approach this resolution in the electronics. This can be done by making two shift registers per wire and clocking them 180° out of phase (Fig. 4). The clock control circuitry now must be capable of accurately stopping the clock at 1/2 cycle intervals. If this is done the dual shift register is capable of resolving 5 ns. This gives a full width resolving power of 200 μ or an equivalent standard deviation of 60 μ , which with the diffusion resolution of 80 μ gives a system resolution of 100 μ .

The most economical IC configuration is probably 4 channels per package. A tentative pinout is shown in Fig. 5. With this arrangement an arbitrarily long chamber can be built with a single line of IC's along the readout edge of the chamber thus eliminating cables and connectors between the PWC and the electronics.

Preliminary cost estimates from several manufacturers indicate that the amplifier-shaper-discriminator will cost about \$2.00 per channel plus a few thousand for engineering and layout. The circuits could be in production in 4 to 6 months. The digital delay-time encoder will also cost about \$2.00 per channel, but the state-of-the-art engineering and mask set development will be \$40,000 to \$50,000. Because of the extensive engineering and development it will take approximately 12 months to put this circuit into production.

Reference

1. E.D. Platner, A Synchronous Delay — Binary Search Proportional Chamber Readout System. Paper presented at the Informal Meeting to Discuss Multiwire Proportional Chamber Electronics, New York City, November 2-3, 1970. BNL Report #15260.

Table Caption

Table I - Amplifier-Discriminator Specifications

Figure Captions

Fig. 1 - Drift-Proportional Wire Chamber Construction

Fig. 2 - 8-Channel Amplifier-Shaper-Discriminator Hybrid

Fig. 3 - Digital Delay-Time Encoder Block Diagram

Fig. 4 - Dual Digital Delay-Time Encoder IC with 5 nsec Resolution.

Fig. 5 - Pinout for Dual Digital Delay-Time Encoder IC

TABLE I

Amplifier - Discriminator Specifications

Amplifier ... Shall match or exceed Fairchild 733-393 Specifications

Gain $X100 \pm 20$

Bandwidth - 3db at greater than 80 MHz

Small signal risetime less than 6 ns

Delay match in package ± 2 ns

Input noise at 100 Ω less than 40 μ v rms

Differentiating Network

1K resistor tolerance $1K \pm 10\%$

15 pF capacitor tolerance 15 ± 5 pf

Discriminator ... Shall match or exceed Signetics 521 Specifications

Time slewing less than 3ns for 20 to 100 mv overdrive

Delay less than 15 ns at 20 mv overdrive

Delay match in package within 3ns for 20 mv overdrive

Offset match in package - all units within 3mv

Output - 10 standard TTL loads

Package: Complete enclosure in metal shield

DRIFT PROPORTIONAL WIRE CHAMBER

Figure 1

Figure 2

Figure 3

Figure 4

DIGITAL DELAY-TIME ENCODER IC

Figure 5