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SANDIA/BENDIX STANDARD PROCESS CAPABILITY
STUDY OF PRINTED WIRING BOARDS

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SANDIA/BENDIX STANDARD PROCESS CAPABILITY STUDY OF PRINTED
WIRING BOARDS

BDX-613-1349, UNCLASSIFIED Topical Report, Published August 1976

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A joint capability study of a standard process utilizing solder leveling for the manufacture of double-sided, plated-through-hole printed wiring boards has been made by Bendix and Sandia personnel. Process variables and final inspection results from 276 completed boards were examined. The study verifies the capability of the selected process to produce reliable, high-quality printed wiring boards and substantiates related specifications and design documents.

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SUMMARY

With the development of the SL/BX standard process for the manufacture of printed wiring boards, it was determined that a formal capability study should be undertaken at Bendix.

Work on the project began in May 1972. Manufacturing efforts in both production and the Engineering Shop were completed by July 1973. Ten lots of boards (252) were manufactured in the Bendix production department. One lot of boards (24) was manufactured in the Bendix Engineering Shop. (A similar study is being conducted on boards produced by the standard process at Sandia Laboratories Albuquerque.) Upon completion of inspection by Bendix, all boards were shipped to Sandia Albuquerque for further inspection and testing. Final inspection results of the 276 boards manufactured show the defects to be predominantly of a visual type. A total of 45 defective boards were found, for a 16 percent defective ratio. Of the 16 percent defective boards, 9 percent (26 boards) are considered nonfunctional and would result in scrap. The remaining 7 percent (19 boards) are considered functional but would require deviation.

The mean mislocation diameter of pattern locations on film photo-tools was found to be 0.0013 inch (0.033 mm). Path widths had a mean deviation of -0.00046 inch (-0.0117 mm).

Plated-through-hole diameters had a calculated mean deviation of 0.0006 ± 0.0009 inch (0.0017 ± 0.0229 mm). The non-plated-through holes were inspected to a ± 0.001 -inch (± 0.025 mm) tolerance. No discrepancies were found.

The mean mislocation diameter for all plated-through and non-plated-through holes was 0.0035 inch (0.089 mm) for boards produced on single-image panels, and 0.0029 inch (0.0736 mm) for boards produced on quadruple-image panels.

The mean mislocation diameters of the terminal areas varied from 0.0044 inch (0.1118 mm) on the single-image lots to 0.0039 inch (0.099 mm) on one multi-image lot and 0.0061 inch (0.1549 mm) on the other multi-image lot. The registration of holes with respect to their related terminal areas was within a diameter of 0.0045 inch (0.1143 mm).

The average surface tin-lead coating thickness was 0.00005 inch (0.0013 mm), as observed by cross sections. Beta backscatter measurements indicated thicknesses from 0.00003 to 0.00005 inch (0.0008 to 0.0013 mm).

Conductor widths on the solder-dipped lots had a mean *growth* of 0.00038 inch (0.0097 mm), while the solder-plated lots had a mean *reduction* of 0.0040 inch (0.101 mm). Circuit spacing was inversely proportional to conductor width deviations.

The mean deviation of terminal-area diameters was +0.0007 inch (0.018 mm) for the solder-dipped boards and -0.0034 inch (0.086 mm) for the solder-plated boards.

No discrepancies were found in either plating adhesion or board flatness.

A total of 45 boards were found to contain visual defects. Twenty-six of the defects were rejectable types, and 19 were considered marginal (capable of use through deviation). Since most defects were visual in nature, the inspection sampling plan was increased (October 1974) from five to ten boards per lot submitted.

As a result of this study, the conclusion was reached that the Bendix production and Engineering Shop departments have the capability for producing printed wiring boards within the requirements of the SL/BX standard process and related specifications.

DISCUSSION

SCOPE AND PURPOSE

Approximately 15 years of manufacturing printed wiring boards (PWB) resulted in Bendix using several processes to produce a "family type" product. These processes, together with numerous incompatible process specifications, led to a joint effort by Sandia Laboratories (SL) and Bendix to integrate existing specifications and processes into one set of documents applicable to all production-oriented, double-sided, plated-through-hole PWBs.

In November 1971 SL and Bendix collaborated to develop the *SL/BX Standard Process for Fabrication and Quality Assurance of Double-Sided, Panel-Plated, Plated-Through-Hole Printed Wiring Boards* and related documents, Design Guide DG 10011, Drafting Standard D 10220, and Process Specification 9928013. The primary requirements of this process are 0.010-inch (0.254 mm) minimum path width and circuit separation and 1-ounce (28 g) clad GH (heat resistant and flame retardant) laminate. The subject study was undertaken to provide data to substantiate or revise selected tolerance parameters. An additional objective was to determine the limits of processing capability and the type and frequency of defects encountered in the fabrication sequence.

A Process Knowledgeable Group (PKG) was established in October 1971 at SL and Bendix to monitor and control the SL/BX standard process and its related documents; this step represents a new concept in product definition and fabrication. All changes made to date on control documents have been closely coordinated and implemented only after full recognition and approval of SL and Bendix members of the PKG. Approximately 3 years of activity under the PKG concept resulted in a noted improvement in PWB quality and cost.

The need to qualify tolerance parameters selected for new product definition, in addition to encompassing existing product in work, resulted in four processes being used to evaluate possible variations within the SL/BX standard process:

- Solder Dip and Level;
- Tin-Lead Plate and Level;
- Solder Dip and Level, printing on step-and-repeat machine; and
- Solder Dip and Level, step and repeat on N/C Plotter.

The tin-lead plate and level variation was a fabrication option permissible under the SL/BX standard process agreement. The

latter two process variations are permissible options determined by the process engineer based on schedule quantities.

The 10 production lots received extensive in-process verification and extensive final inspection. The lot produced in the Engineering Shop received extensive final inspection only.

PRIOR WORK

The solder dip and level process developed under PDO 6984712 (BDX-613-739, *Solder Leveling*), provided the initial data necessary for development of the SL/BX standard process and its related documents (DG 10011, D 10220, and 9928013). This study conclusively proved that the solder leveling process did not damage printed wiring boards and that the leveled coating retained adequate to good solderability. In addition, BDX-613-1171 (PDO 6984684), *Effects of Thermal Expansion on Epoxy Glass Laminates*, was also instrumental in developing the SL/BX standard process. The results of this study showed that gradual or instant shock encountered during the process cycle had no adverse effects on board quality.

ACTIVITY

The two basic processes involved are defined in Table 1. The dip and level process, considered most economical, was specifically developed for all new product designed after release of the SL/BX standard process and related documents. For additional economic reasons, the solder plate and level process was included to encompass boards already in production which could not conform completely to 9928013 without extensive redesign of the artwork (circuit masters) and related phototooling, thereby creating added costs.

Lots 101, 102, 103, 104, 301, 401, and the Engineering Shop lot were built to the dip and level process (Table 1) on 6.0- by 9.0-inch (152.4 by 228.6 mm) panels. Lots 201, 202, 203, and 204 also utilized 6.0- by 9.0-inch panels, but were processed to the tin-lead plate and level concept. Lots 301 and 401 are multiple-image (4 images per panel) lots produced on 12.0- by 12.0-inch (304.8 by 304.8 mm) panels and processed to the solder dip and level concept. Lot 301 was stepped and repeated on a step-and-repeat machine using a single-image photomaster. Lot 401 was stepped and repeated on the N/C Plotter using the original digitizing format data.

Board material for all production department lots consisted of 0.062-inch-thick (1.575 mm) GH laminate with 1-ounce copper, 2 sides. The Engineering Shop lot was the same except that the copper was 2-ounce. Materials were procured from three laminate suppliers.

Table 1. Process Sequence for Solder Dip and Level and Solder Plate and Level

First 10 Steps for Both Processes

1. Shear panels and punch tooling holes
 2. NC drill plated-through holes (PTH)
 3. Remove drill burrs (surface) abrasive
 4. Wet blast panels to remove burrs and loose laminate in holes
 5. Clean panels by pumice-scrubbing surface
 6. Copper electroless plate; includes preplate cleaning; provides through-hole electrical continuity
 7. Copper electroplate (copper pyrophosphate bath) 0.001 minimum in holes
 8. Deburr panel surface
 9. Clean panels by pumice scrubbing
 10. Apply dry film resist
-

Solder Dip and Level Process

11. Expose negative circuit image
12. Develop (photoresist becomes etchant mask)
13. Etch to remove unwanted copper
14. Remove photoresist
15. NC drill NPTHs
16. 60 Sn/40 Pb solder dip
17. Solder level (liquid)
18. Cut pattern (board profile) from panel
19. Deburr
20. Clean part
21. Identify part
22. Package part
23. Final inspection

SnPb Plate and Level Process

11. Expose positive circuit image
 12. Develop (photoresist becomes plating mask)
 13. Electroplate 60 Sn/40 Pb (fluoroborate bath); plates circuitry only (SnPb becomes etchant mask)
 14. Remove photoresist
 15. Etch (removes unwanted copper)
 16. NC drill NPTHs
 17. Solder level (liquid)
 18. Cut pattern (board profile) from panel
 19. Deburr
 20. Clean part
 21. Identify part
 22. Package part
 23. Final inspection
-

Figure 1 displays the circuit pattern (2 sides) used. Various sizes of an identification number and letter were applied to establish minimum sizes necessary for adequate legibility after etching. The definition of the capability board was released under drawing DL SO-3885.

In-process verification by manufacturing during production normally captures defects as they occur or become noticeable and results in the defective product becoming line scrap. To fully comprehend the capability of the SL/BX standard process, a decision was made to retain in-process defective boards with their respective lots throughout the process, unless grossly inadequate, and submit them to final inspection without the benefit of discrete identification.

The 10 production lots produced in D/61 were subjected to numerous in-process sample inspections by Quality Control, thereby adding significantly to handling-caused defects not encountered in the normal standard process.

The test board circuitry, designed specifically for this study, contained features considered beyond the known capability of the selected process. These are hole diameters of 0.022 inch (0.559 mm) nominal, conductor widths 0.005 inch (0.127 mm) wide, and terminal area diameters of 0.050 inch (1.270 mm). Of these, only the latter two caused discrepancies; the 0.005 inch conductors were lost on all the solder-plated boards and were intact on the majority of the solder-dipped boards. The 0.050-inch-diameter terminal areas caused minimum annular ring discrepancies on approximately 10 percent of the boards. Discrepancies attributable to these parameters are excluded from this report.

Phototools

The phototools were produced from artwork plotted at Bendix. A single-image plot was used to produce the negative and positive phototools for all single-image lots (101 through 104, 201 through 204, and the Engineering Shop lot), and one multi-image lot (301). A multi-image circuit master was plotted to produce a multi-image phototool for Lot 401. The multi-image phototool for Lot 301 was produced on a step-and-repeat machine.

The artwork was also plotted at SLA and compared with the Bendix plots. In an environment controlled to 68°F (20°C) and 50 percent relative humidity (RH), the mean X deviation of terminal area locations was 0.0004 ±0.0003 inch (0.010 ±0.008 mm) for the SLA plots and 0.0001 ±0.0002 inch (0.003 ±0.005 mm) for the Bendix plots. In the Y direction, the mean deviation was 0.0001 ±0.0002 inch for the SLA plots and 0.0002 ±0.0004 inch for the Bendix plots.

SIDE 1A

SIDE 2A

Figure 1. Circuit Pattern

Figures 2 and 3 are histograms of terminal area location accuracies of the Bendix plots and the phototools used to produce all lots. The mean mislocation diameter for the phototools was 0.0013 inch (0.033 mm), while the mean mislocation diameter for the plots was 0.00128 inch (0.0325 mm).

The path widths on the Bendix single-image plot and those on the negative and positive phototools made from this plot were inspected at 68°F and 50 percent RH. The deviations from nominal were plotted on a single graph (Figure 4). Path width deviations from nominal on the SLA plot are also in Figure 4. The mean deviation from nominal on the Bendix plot was -0.00046 inch (-0.0117 mm). The major reasons for these deviations from nominal are a result of aperture size discrepancies which have since been corrected at Bendix. The path widths on the phototools varied only slightly from those of the plot with the positive tool having a mean deviation of +0.00013 inch (0.0033 mm) and the negative tool having a mean deviation of -0.00013 inch.

Hole Size

All holes were drilled on an N/C drilling machine using standard, commercially available, production-type PWB drills. Design Guide DG 10011 specifies a TP tolerance of 0.008 inch (0.203 mm) minimum (0.010 inch or 0.254 mm preferred) on hole sizes after plating. The capability board design requires a 0.010-inch tolerance on all finished hole diameters except Datum Holes 1 and 2, which require a 0.004-inch (0.102 mm) tolerance. Both plated-through-holes (PTHs) and non-plated-through-holes (NPTHs) were drilled to a processing tolerance of ± 0.001 -inch (0.025 mm) diameter. All PTHs were drilled 0.002 inch (0.051 mm) over their maximum AY drawing requirement to allow for a 0.001-inch minimum copper plating buildup in the holes. This results in the largest possible hole size after plating, thereby allowing use of the MMC modifier on hole-location requirements. In addition, holding PTHs to the high side of their tolerance usually prevents small plating nodules from causing ULL conditions. All NPTHs were drilled to their mean AY requirement.

Immediately after drilling 31,232 PTHs, approximately 3600 holes, representing ten lots, were inspected for size by go/no-go plug gages to a ± 0.001 -inch processing tolerance. Results of this check showed that all but two of the 3600 holes fell within the required tolerance. The two exceptions measured 0.001 inch over the processing tolerance.

Immediately after plating, the PTHs were again checked for size. A total of approximately 1200 holes representing the ten lots were inspected. Figure 5 shows the variation from nominal and reflects the value of holding hole sizes toward the high side of their tolerance to compensate for plating nodules and provide use of the MMC modifier on hole location.

Figure 2. Terminal Area Mislocations on Phototools Used on All Lots

Figure 3. Terminal Area Mislocations of Gerber Plots Used to Make All Phototools

Figure 4. Path Widths From Phototools Used in Fabrication of All Single-Image Lots and the Plot From Which These Phototools Were Made (Also SLA Plot)

The calculated mean deviation from nominal (midpoint of the hole-size tolerance range) on PTH sizes was 0.0006 ± 0.0009 inch (0.015 ± 0.022 mm) for the 1200 holes inspected. These deviations include plating and solder-coating variations.

Immediately after drilling 16,640 NPTHs, approximately 1900 holes, representing ten lots, were inspected for size by go/no-go plug gages to a ± 0.001 -inch processing tolerance. No discrepancies were found.

Figure 5. Plated-Through Hole Sizes

Hole Location

All holes were produced on an N/C drilling machine capable of drilling nine various size holes in one operation cycle. The PTHs are drilled in relationship to two tooling holes in the panel to provide coordination with the NPTHs drilled at a later operation from the same tooling holes.

Figure 6 shows the hole pattern for all PTHs and NPTHs; the hole data is provided in Table 2. Datum Holes 1 and 2 are NPTHs and are used as datum and datum-orient, respectively, to determine the location of all other holes. To maintain processing tolerance continuity, Datum Holes 1 and 2 are coordinated with the panel tooling holes used in the two drilling operations.

A total of 187 holes, consisting of 122 PTHs and 65 NPTHs, were drilled in each single-image panel. A total of 748 holes, consisting of 488 PTHs and 260 NPTHs, were drilled in each multi-image panel. Table 2 shows the various hole sizes and the quantity of each produced. Single-image, 6.0- by 9.0-inch (152.4 by 228.6 mm) panels were drilled in two stacks, one high per machine cycle. Multiple-image 12.0- by 12.0-inch (304.8 by 304.8 mm) panels were drilled in one stack, one high per machine cycle.

Coordinate hole locations X and Y are defined by Engineering Drawing NC-SO3885. The hole location tolerance specified in DG 10011 is 0.005-inch (0.127 mm) diameter TP MMC (0.010 inch preferred). Since all PTHs were drilled 0.002 ± 0.001 inch over their AY maximum size, the use of the MMC modifier on hole locations would result in a hole-location tolerance of 0.010- to 0.013-inch (0.330 mm) TP diameter. However, all hole-location data in this report was compiled as if the tolerance modifier were "regardless of feature size" (RFS). Table 3 summarizes the results for hole mislocation. Results are grouped by the stage of processing when measured.

A total of 47,872 holes were drilled in the 252 boards. Of this total, 4945 holes were checked in-process and at final inspection. The in-process holes (1248) were checked from tooling holes in the panels. Final inspection on the remaining 3697 holes was made with respect to Datum and Datum-Orient Holes 1 and 2, respectively. The largest computed upper statistical tolerance limit was 0.0088 inch (0.2235 mm). The mean mislocation diameter varied from 0.0023 to 0.0035 inch (0.0584 to 0.0889 mm). Both the actual and estimated percent of holes mislocated more than 0.0100 inch were zero, in most cases. The basic analysis methods were the same for each characteristic and consisted of calculating the mean, standard deviation, and statistical tolerance limits so that with 90 percent confidence, 99 percent of the population of measurements would fall within the computed limits.

Figure 6. Hole sizes and Locations

Table 2. Hole Data

Hole Print Diameter*	Drilled Diameter	Land Diameter	Hole Numbers Used On Board	Hole Numbers Checked In Process	Total Of Each Size
0.018/0.026 0.018/0.026	0.028	0.050 0.062	3-26 30-41	11,20,30	36**
0.030/0.040 0.030/0.040	0.042	0.075 0.086	50-73 80-103	52,66,98	48**
0.040/0.050	0.052	0.100	110-121	111,113, 118	12**
0.050/0.060 0.050/0.060	0.062	0.125 0.150	130-143 150-161	142,143, 159	26**
0.085/0.095	0.090	0.040	220-270	220,228, 238,247 266,270	51***
0.120/0.130	0.125	0.040	280-291	1,2,283, 287,289, 291	14***

*1 inch equals 25.4 mm

**Plated-through holes

***Non-plated-through holes

Table 4 displays the individual data for single- and multiple-image lots used to compile the PTH section of summary data shown in Table 3. Figures 7 and 8 are histograms supporting Table 4.

Table 5 displays the individual data for single- and multiple-image lots used to compile the NPTH section of summary data in Table 3. Figures 9 and 10 are histograms supporting Table 5.

Table 6 displays the individual data for single-image, multiple-image, and the Engineering Shop lots used to compile the Final (All Holes) section of summary data shown in Table 3. Figures 11, 12, and 13 are histograms supporting Table 6.

Table 3. Hole Mislocation Summary

Characteristic and Sample Size	Mean Mislocation Diameter (TP Deviation)	Standard Deviation	Computed Upper Limit*	Estimated Percent Over 0.0100**
PTH Before Plating***				
Single Image (576)	0.0025††	0.0011	0.0054	0
Multi Image (192)	0.0028	0.0011	0.0053	0
NPPTH After Plating and Etching***				
Single Image (384)	0.0033	0.0017	0.0081	0.06
Multi Image (96)	0.0023	0.0014	0.0068	0
Final--All Holes†				
Single Image (2959)	0.0035	0.0016	0.0080	0.05
Multi Image (738)	0.0029	0.0012	0.0061	0

*With 90 percent confidence, 99 percent of the population will be less than the upper limit

**None actual

***Measured from tooling holes

†Measured from Datum Holes 1 and 2

††1 inch equals 25.4 mm

Terminal Area Location

The terminal area mislocation diameters shown in Table 7 were derived from final inspection measurements on Terminal Areas 142 and 143. These terminal areas, located on the opposite corners of the board, were measured on each side of six boards per lot. The method of analysis was the same as for hole mislocations. The mean mislocation was greatest, 0.0061 inch (0.155 mm), with Lot 301, and smallest, 0.0039 inch (0.099 mm), with Lot 401. The upper statistical tolerance limit varied from 0.0094 to 0.0131 inch (0.239 to 0.333 mm).

Although these upper limits are higher than anticipated, the registration of hole locations with respect to terminal area locations was well within 0.005 inch (0.127 mm) for the boards built in the production department.

The registration of a particular hole with respect to its terminal area location on either side of the PWB was obtained by accurately plotting the center locations (with respect to true position) of Holes 142 and 143 and their related terminal areas from both sides

Table 4. PTH Mislocation (Before Plating)

Lot	Mean Mislocation Diameter (TP Deviation)	Standard Deviation*	Sample Size	Upper Limit***
101	0.0031**	0.0008	72	0.0054
102	0.0027	0.0012	72	0.0061
103	0.0029	0.0010	72	0.0058
104	0.0016	0.0008	72	0.0040
201	0.0025	0.0008	72	0.0045
202	0.0025	0.0012	72	0.0064
203	0.0025	0.0011	72	0.0060
204	0.0024	0.0011	72	0.0055
Single Image Total	0.0025	0.0011	576	0.0054
301	0.0025	0.0012	96	0.0054
401	0.0031	0.0008	96	0.0053
Multi Image Total	0.0028	0.0011	192	0.0053

*Based on measurements of these 12 holes: 11, 21, 30, 52, 66, 98, 111, 113, 118, 142, 143, and 159.

**1 inch equals 25.4 mm.

***With 90 percent confidence, 99 percent of the population of all hole mislocation diameters will be less than the upper limit; none exceeded 0.0100.

of the PWB, and then determining the smallest possible diameter which would encircle all three points. The largest circle diameter encountered from the 10 production lots was 0.0045 inch (0.114 mm), while the largest from the Engineering Shop lot was 0.0055 inch (0.140 mm). A histogram and an example of the procedure used are shown in Figure 14.

Copper Plating and Copper Clad Thickness

A copper pyrophosphate bath with PY-81-H additive was used for the plating. Assuming uniform distribution and 100-percent cathode efficiency, the theoretical calculated average copper-plating

Figure 7. PTH Mislocation Diameters, Before Plating (Single Image)

Figure 8. PTH Mislocation Diameters,
Before Plating (Multi-Image)

thickness was 0.0020 inch (0.051 mm) for the 10 production department lots and 0.0015 inch (0.038 mm) for the Engineering Shop lot.

Hole Wall Copper Thickness

Specification 9928013 requires a 0.001-inch (0.025 mm) minimum copper thickness on the hole walls. Plating thickness in holes was determined by axial cross section and resistance measurements. For the latter, a Micro-Ohm Meter and a Model CD-3 Caviderm were used in accordance with Test Method 2.2.13.2 in IPC-TM-650. Hole-wall copper-thickness measurements taken from metallurgical mounts are displayed by a histogram in Figure 15. These measurements resulted in a mean thickness of 0.0015 inch (0.036 mm) for the 10 production shop lots and 0.0012 inch (0.030 mm) for the Engineering Shop lot.

Micro-Ohm Meter resistance measurements from the 10 production department lots are shown in Table 8. Mean resistances for eight holes measured on each board of each lot are given. Also shown

Table 5. NPTH Mislocation

Lot	Mean Mislocation Diameter (TP Deviation)	Standard Deviation*	Sample Size	Upper Limit***
101	0.0025	0.0013	48	0.0060
102	0.0040	0.0018	48	0.0097†
103	0.0022	0.0009	48	0.0042
104	0.0025	0.0012	48	0.0066
201	0.0043	0.0016	48	0.0084
202	0.0039	0.0020	48	0.0100††
203	0.0036	0.0015	48	0.0077
204	0.0033	0.0018	48	0.0081
Single Image Total	0.0033	0.0017	384	0.0081†††
301	0.0030	0.0016	48	0.0073
401	0.0016	0.0008	48	0.0039
Multi Image Total	0.0023	0.0014	96	0.0068

*Based on measurements of these 12 holes: 1, 2, 220, 238, 247, 266, 270, 283, 287, 289, and 291

**1 inch equals 25.4 mm

***With 90 percent confidence, 99 percent of the population of all hole mislocation diameters will be less than the upper limit

†Estimated 0.28 percent over 0.0100; none actual

††Estimated 0.43 percent over 0.0100; none actual

†††Estimated 0.06 percent over 0.0100; none actual

are the standard deviations within a lot. Lot-to-lot variations are greater than those within a lot. Analysis of the resistances between boards within a lot shows plating-rack position is not as important as expected. However, the holes in the interior of the pattern were, on the average, slightly higher in resistance than those on the perimeter. For the quadruple-image panels, the holes which were from 0.5 to 1 inch (12.7 to 25.4 mm) from the panel edge were approximately 12-percent lower in resistance than those near the center. The relative variations in hole-wall thickness are much less than those observed for surface plating.

Figure 9. NPTH Mislocation Diameters (Single Image)

There are two procedures for converting hole-resistance measurements to copper-thickness values. The first and most reliable makes use of conversion curves generated from the cross-section thicknesses of holes of the same type as those being measured. The other uses calibration curves furnished with the instruments. The latter requires favorable hole geometry or the application of correction factors. For both instruments, the current probe makes contact on the opposite side of the terminal area from the voltage probe during a measurement. If the voltage drop across the terminal area from the current to the voltage probe is not negligible as compared to the voltage drop between the voltage probes, that is, through the hole, then a correction factor must be applied. This correction becomes larger as the hole diameter and copper thickness increase and the terminal area and laminate thickness decrease. A new Caviderm probe system has recently become available to alleviate these corrections.

Figure 10. NPTH Mislocation Diameters (Multi-Image)

To check the effectiveness of the correction factors derived from Caviderm charts, 20 holes on four boards were read on the Caviderm and then cross sectioned. On other boards, for which cross section thickness data was available, Caviderm readings were taken on holes of the same size and in the same board area as those sectioned. Actual terminal area diameters were estimated from the cross sections to obtain more reliability in the correction factors.

Average cross-section thicknesses for the four hole sizes along with average thicknesses derived from corrected Caviderm readings are given in Table 9. For several cross sections, especially those for the smallest hole, the section was not through the diameter of the hole. For those cases, the observed copper thickness had to be converted to the thickness corresponding to a section through the hole diameter. The corrections ranged up to 0.0003 inch (0.008 mm). Cross-section thicknesses were averaged from six readings, three for each side of the hole.

The production shop boards were safely above the required 0.0010-inch (0.025 mm) minimum. Standard deviations for five holes of the same size on each board are 0.00006 inch (0.0015 mm). Standard deviations between boards for the same hole size are larger, 0.00012 to 0.00016 inch (0.0030 to 0.0041 mm), excluding the Engineering Shop boards.

Text continued on page 32.

Table 6. Hole Mislocation--Final

Lot*	Mean Mislocation Diameter (TP Deviation)	Standard Deviation	Sample Size	Upper Limit**
101	0.0029***	0.0012	370	0.0060
102	0.0041	0.0018	370	0.0083
103	0.0030	0.0011	369	0.0058
104	0.0032	0.0014	370	0.0070
201	0.0026	0.0011	370	0.0058
202	0.0045	0.0018	370	0.0097†
203	0.0037	0.0016	370	0.0085††
204	0.0037	0.0016	370	0.0075
Single Image Total	0.0035	0.0016	2959	0.0080†††
301	0.0033	0.0013	368	0.0065
401	0.0025	0.0011	370	0.0052
Multi Image Total	0.0029	0.0012	738	0.0061
Eng Shop	0.0042	0.0018	370	0.0088††††

*Final inspection was conducted after printed wiring boards were trimmed to size with tooling holes removed; all holes were measured with Holes 1 and 2 on the board as datum and datum orient.

**With 90 percent confidence, 99 percent of the population of all hole mislocation diameters will be less than the upper limit.

***1 inch equals 25.4 mm

†Estimated 0.54 percent over 0.0100; actual was 0.27 percent

††Estimated 0.11 percent over 0.0100; none actual

†††Estimated 0.05 percent over 0.0100; actual was 0.03 percent

††††Estimated 0.07 percent over 0.0100; none actual

Figure 11. Final Hole Mislocation Diameters (Single Image)

Figure 12. Final Hole Mislocation Diameters
(Multi-Image)

Figure 13. Final Hole Mislocation Diameters (Single Image, Engineering Shop Processing)

The copper was thinnest in the 0.028-inch (0.711 mm) holes. This was expected because of the more restricted flow of solution through the smaller diameter. Plating in the holes was lower, in general, than that on the terminal areas. It must be recognized that Table 9 reflects the average thicknesses of terminal areas that were measured after a sanding operation.

Hole walls were reasonably straight (Figure 16). There were, however, some with nodules, as shown in Figures 17 and 18. These irregularities usually originate from drilling. One hole-size may show irregularities, whereas other sizes on the same board show uniform walls.

With small hole sizes, the corrected Caviderm thicknesses are within experimental error of the cross-section thicknesses. For large hole sizes, the Caviderm measurements indicate a positive thickness bias. The differences between average thicknesses from cross sections and those from corrected Caviderm measurements increased

Table 7. Terminal Area Mislocations

Characteristic And Sample Size	Mean Mislocation Diameter (TP Deviation)*	Standard Deviation	Computed Upper Limit**	Estimated Percent Over 0.0100
Single Image-Solder Dip and Level (96)	0.0043	0.0020	0.0099	0.49
Single Image-Tin Lead Plate (96)	0.0044	0.0019	0.0094	0.17
Multi Image- Step and Repeat (24)	0.0061	0.0019	0.0131	3.40†
Multi Image- Gerber Plot (24)	0.0039	0.0014	0.0081	0
Single Image- Engineering Shop (24)	0.0050	0.0026	0.0128	3.27†

*1 inch equals 25.4 mm

**With 90 percent confidence, 99 percent of the population will be less than the upper limit

†Actual was 4.17 percent

with hole size. The 0.052-inch (1.321 mm) hole had only one nominal terminal area diameter. For the other hole sizes, the resistance readings were consistently lower for a smaller terminal area. For example, the average resistance of a 0.062-inch (1.575 mm) hole with a 0.150-inch (3.81 mm) terminal area diameter was from 1.109 to 1.119 times greater than an adjacent 0.062-inch hole with a 0.125-inch (3.17 mm) terminal area diameter. This effect was observed with both instruments.

Surface-Copper Thickness

The total surface-copper thickness consists of the copper cladding, plus the copper plating, minus the copper removed during the sanding operations and the preplating etch. The sanding operations before and after plating are used to remove drilling burrs and plating nodules. Although specification 9928013 does not have a requirement for surface-copper thickness, it is obviously important that the process does not remove an excessive amount of copper and

Text continued on page 39.

DIAMETERS ARE OF THE SMALLEST CIRCLES WITHIN WHICH ALL THREE ELEMENTS WILL FALL REGARDLESS OF THEIR LOCATION WITH RESPECT TO TRUE POSITION.

THIS DATA IS A TRUE INDICATION OF THE REGISTRATION (FRONT-TO-BACK PATTERN AND HOLE-TO-HOLE PATTERN) CAPABILITY.

EXAMPLE: BOARD 1, TERMINAL AREA AND HOLE 142

Figure 14. Terminal Area Locations Versus Related Hole Locations

Figure 15. Copper Thickness in Holes From All 11 Lots

Table 8. Lot to Lot Hole Resistance Measurements

Lot*	Hole Number***								Total
	21	30	52	98	111	159	142	143	
101	328	324	162	189	108	96	75	68	1349
Std Dev	25	15	11	12	7	6	5	4	
102	249	251	138	139	85	75	62	59	1058
Std Dev	8	12	10	11	7	7	7	6	
103	339	328	154	178	99	91	69	61	1319
Std Dev	32	18	9	12	7	7	6	4	
104	270	301	131	151	94	78	62	59	1147
Std Dev	31	19	17	13	13	8**	8	6	
201	293	295	159	180	102	91	68	61	1248
Std Dev	32	29	15	15	10	10	9	8	
202	315	331	155	174	92	91	68	61	1285
Std Dev	23	28	17	12	15	9	9	5	
203	246	249	111	129	72	60	49	47	959
Std Dev	18	15	9	9	6	3	3	2	
204	249	264	116	126	77	62	52	49	946
Std Dev	16	15	10	12	8	8	5	5	
Mean	286	293	141	158	91	81	63	58	
Std Dev	38	34	20	25	12	14	9	7	
301	237	241	119	130	73	67	52	52	968
Std Dev	38	34	35	17	10	10	7	6	
401	261	277	128	131	83	68	58	59	1064
Std Dev	38	32	19	8	6	5	7**	6	
0.0015 Thickness Reading	300	300	178	178	131	100	100	100	

*Microohm meter measurements on Lots 101 to 204 are from 24 boards per lot; on Lots 301 and 302, 32 boards per lot

**Excludes holes with infinite or very high resistance

***Drill diameter of Holes 21 and 30 was 0.028 inch; for Holes 52 and 98 it was 0.042 inch; for Hole 111 it was 0.052 inch; and for Holes 159, 142, and 143, it was 0.062 inch. Terminal Area diameters were as follows: Hole 21, 0.050 inch; Hole 30, 0.062 inch; Hole 52, 0.075 inch; Hole 98, 0.086 inch; Hole 111, 0.100 inch; Hole 159, 0.150 inch; Holes 142 and 143, 0.0125 inch.

Table 9. Copper Plating Thickness of Holes and Terminal Areas (In Microinches)

Lot	Drilled Hole Diameter*				Mean
	0.028	0.042	0.052	0.062	
101	1.47 (1.49)** 1.43 (1.52)	1.48 (1.65) 1.51 (1.68)	1.54 (1.83) 1.55 (1.92)	1.48 (1.60) 1.56 (1.58)	1.49 (1.66) 1.51 (1.68) 1.62
TA-1A***					1.78
TA-2A					
104	1.33 (1.33)	1.56 (1.85)	1.52 (2.00)	1.50 (1.68)	1.48 (1.72) 1.83
TA-1A					1.63
TA-2A					
201	1.29 (1.45) 1.29 (1.38) 1.43 (1.50)	1.26 (1.57) 1.30 (1.51) 1.57 (1.68)	1.43 (1.74) 1.39 (1.70) 1.65 (1.90)	1.38 (1.55) 1.38 (1.55) 1.49 (1.73)	1.34 (1.58) 1.34 (1.54) 1.53 (1.70) 1.40
TA-1A					1.54
TA-2A					
202	1.28 (1.33)	1.40 (1.62)	1.46 (1.68)	1.37 (1.58)	1.38 (1.55) 1.71
TA-1A					1.37
TA-2A					
203	1.68 (1.79) 1.57 (1.65) 1.65 (1.77)	1.57 (1.98) 1.63 (1.97) 1.59 (1.94)	1.64 (2.17) 1.77 (2.22) 1.60 (2.21)	1.67 (2.00) 1.75 (2.02) 1.60 (1.96)	1.64 (1.99) 1.68 (1.97) 1.61 (1.97) 1.57
TA-1A					1.64
TA-2A					
204	1.46 (1.68) 1.54 (1.65)	1.61 (1.83) 1.62 (1.75)	1.56 (2.03) 1.58 (2.00)	1.62 (1.78) 1.60 (1.75)	1.56 (1.83) 1.59 (1.79) 1.51
TA-1A					1.64
TA-2A					
401	1.54 (1.67) 1.50 (1.62)	1.62 (1.94) 1.49 (1.89)	1.62 (2.08) 1.45 (2.06)	1.68 (1.93) 1.57 (1.82)	1.62 (1.91) 1.50 (1.85) 1.85
TA-1A					1.40
TA-2A					

Table 9 Continued. Copper Plating Thickness of Holes and Terminal Areas (In Microinches)

Lot	Drilled Hole Diameter*				Mean
	0.028	0.042	0.052	0.062	
Mean	1.46 (1.56)	1.52 (1.78)	1.55 (1.97)	1.55 (1.75)	1.52 (1.77)
Sigma	0.16 (0.15)	0.12 (0.16)	0.10 (0.18)	0.12 (0.17)	0.11 (0.16)
Eng Shop	1.03 (1.18)	1.17 (1.24)	1.01 (1.45)	1.18 (1.32)	1.10 (1.29)
	1.10 (1.20)	1.11 (1.25)	1.17 (1.44)	1.21 (1.34)	1.15 (1.31)

*1 inch equals 25.4 mm

**Values in parentheses are from resistance measurements; all others from cross sections

***Terminal area copper thickness

Figure 16. Typical Hole Wall (Sandia Photograph)

thereby reduce the current-carrying capabilities of the PWB conductors. Figures 19 and 20 show histograms of the thicknesses of the copper cladding, the copper plating, and the total (cladding plus plating) copper. These measurements were taken from metal-lurgical mounts of specimens taken from the edges of the PWB panels during the fabrication process. The mean thicknesses for each category are 0.00115 inch (0.0292 mm) for the clad (as compared to a range of 0.00128 to 0.00140 inch [0.03251 to 0.03556 mm] as received), 0.00168 inch (0.0426 mm) for the plated copper and 0.00288 inch (0.07315 mm) for the total (plated plus clad) copper.

The copper-clad thicknesses were reduced more than expected in some cases, varying from less than 0.0001 to nearly 0.0004 inch (see Table 10). Beta backscatter measurements over the clad

Figure 17. Rough Hole Wall (Sandia Photograph)

surfaces of unprocessed panels showed variations of less than 0.0001 inch. These clad-thickness variations from lot to lot are attributable to the as-received clad-thickness variations, plus the variations from sanding and preplating etch operations.

The copper-plating thickness measurements from the panel-edge specimens are given in Table 11. This table lists the thicknesses before and after sanding operations. In some instances, the value of the comparison was lost because sampling locations were selected from opposite sides of the panel, thus producing inconsistencies in the before- and after-sanding thickness measurements.

Thickness of the copper cladding and the plating in the pattern area was determined from conductor and terminal area cross sections.

Figure 18. Nodular Hole Wall (Sandia Photograph)

Ten conductors were sectioned on two boards from each lot. The conductors on Side 1A were sectioned on the first board of the lot, and those on Side 2A were sectioned on the second board. Terminal area thicknesses were measured from PTH cross sections. Average plating thicknesses for these measurements, along with those from the edge samples, are given in Table 12. The values are not directly comparable because they represent different sampling sites.

Plated-copper thickness variations greater than 2:1 were found when samples were taken from different locations on a panel surface. The thickest copper, up to 0.0028 inch (0.071 mm), was found on panel edges making up the perimeter of the plating rack.

Figure 19. Surface Copper Thickness From Panel Edge Samples, Clad and Plate

Figure 20. Surface Copper Thickness From Panel Edge Samples, Total Copper

The mean thickness of plated copper on the surface of finished boards was 0.0015 inch (0.0381 mm). The plated-copper thickness was reduced by an abrasive sanding, but the amount removed was not determined. The plating thickness before post-plate sanding is estimated to be 0.0016 inch (0.0406 mm).

Beta backscatter measurements were made according to ASTM-B-567 on seven 0.100-inch-wide (2.54 mm) conductors on the first six boards of each lot. Three of these were on Side 1A, and four were on Side 2A. Small corrections were made for the thin solder coating and for the differences in laminate material. The results are given in Tables 12 and 13. Plating thickness was obtained by subtracting the average clad thickness (Table 13) from the total copper thickness. The uncertainty in the measurement is 0.0001 inch (0.0025 mm).

The differences between the two sides of the same board, as shown by beta backscatter measurements in Table 13, are real. They

Table 10. Copper Clad Thickness

Lot	Samples Measured*		Terminal Areas	Average (μ -inch)	Difference From Initial
	Wedges	Conductors			
101	1.24	1.19	1.18	1.20	
102	1.16	1.24		1.20	0.11
103	1.11	1.23		1.17	0.14
104		1.29	1.34	1.32	
201	1.21	1.20	1.21	1.21	
202		1.13	1.19	1.16	0.15
203	1.00	0.93	0.88	0.94	0.37
204	1.27	1.28	1.27	1.27	
301	1.11	1.08		1.10	0.21
401		1.22		1.22	0.09
Eng Shop		2.34		2.34	

*1 inch equals 25.4 mm

arise from one side of the plating rack being closer to the anode than the other, and from a different solution flow pattern on one side than the other. Note that the 1A and 2A thicknesses for the conductor cross sections represent different boards.

Mean plating thicknesses were less in the pattern area than at the panel edges. These differences would have been greater had all the edge samples been taken from the panel edge toward the solution.

There appeared to be no general pattern of thickness variation related to plating position. The average spread between the highest and lowest thickness on the same side of the six boards of each lot was 0.0003 inch (0.0076 mm).

Tin-Lead Coating

From cross sections viewed at a magnification of 550X, the leveled tin-lead thickness measured approximately 0.000050 inch (1.270 μ m). Beta backscatter measurements with a promethium 147 source indicated thicknesses from 0.000035 inch (0.889 μ m) to 0.000050 inch for the

Table 11. Copper Plating Thickness on Panel Edge Samples (In Microinches)

Lot	Average*		Range	
	1A	2A	1A	2A
101-BS** -AS	1.66***	1.70	0.63 (1.49-2.12)	0.51 (1.46-1.97)
102-BS	1.60	1.50	0.54 (1.35-1.94)	0.42 (1.35-1.77)
-AS	2.15	2.08	1.29 (1.36-2.65)	1.52 (1.39-2.91)
103-BS	1.50	1.81	0.29 (1.32-1.61)	0.59 (1.45-2.04)
-AS	1.50	1.77	0.30 (1.37-1.67)	0.56 (1.41-1.97)
201-BS	1.45	1.71	0.56 (1.27-1.83)	0.58 (1.49-2.07)
-AS	1.53		0.71 (1.32-2.03)	
203-BS	1.67	1.58	0.43 (1.50-1.93)	0.27 (1.44-1.71)
-AS	1.82	1.69	0.39 (1.65-2.04)	0.21 (1.60-1.81)
204-BS	1.69	1.58	0.44 (1.45-1.89)	0.20 (1.53-1.73)
-AS	1.69	1.55	0.58 (1.36-1.94)	0.44 (1.39-1.83)
301-BS	1.87		1.17 (1.59-2.76)	
-AS	1.75	1.76	0.64 (1.46-2.10)	0.56 (1.54-2.10)

*Average of six samples per side

**BS means after plating but before sanding; AS means after plating and after sanding

***1 inch equals 25.4 mm

dipped and leveled boards, and 0.000030 inch (0.760 μ m) for the plated and leveled boards. The greater thickness for the dipped boards is probably associated with the formation of more copper-tin intermetallic because of the greater exposure to solder and heat.

Solder formations, often as thick as the copper (0.001 to 0.002 inch or 0.025 to 0.051 mm), were found in several holes of the dipped and leveled boards. This formation was usually seen on only one side of a hole, as shown in Figure 16. This condition occurs as a result of residual molten solder running to the lower side of the hole as the PWB panel is withdrawn from the solder-leveling machine.

Circuit Pattern Definition

Conductor Width and Circuit Spacing

Deviations from nominal were measured on 70 conductors (35 per side) and 18 separations (9 per side) before etching (after resist

Table 12. Average Surface Copper Plating Thicknesses (In Microinches)

Lot	Cross Sections						Beta Backscatter	
	Edges*		Conductors**		Terminal Areas***		Conductors†	
	1A	2A	1A	2A	1A	2A	1A	2A
101	1.66††	1.70	1.57 1.54	1.58 1.67	1.62	1.78	1.66	1.68
102	2.15	2.08	1.22	1.41			1.38	1.34
103	1.77	1.50	1.66	1.43			1.60	1.34
104			1.88	1.59	1.83	1.63	1.73	1.59
201	1.53		1.24	1.51	1.40	1.54	1.36	1.76
202			1.59	1.37	1.71	1.37	1.54	1.31
203	1.82	1.69	1.37	1.64	1.57	1.64	1.42	1.30
204	1.67	1.55	1.65	1.31	1.51	1.64	1.43	1.33
301	1.75	1.76		1.63			1.48	1.68
401					1.85	1.40	1.74	1.34
Eng Shops			1.29	1.32			1.33	1.41

*One sample per panel side; six panels per lot

**Nine conductors per side; one board per lot

***Twenty terminal areas per side; one to two boards per lot

†Three or four conductors per side; six boards per lot

††1 inch equals 25.4 mm

Table 13. Copper Plating Thicknesses By Lot (Beta Backscatter Measurements With Sr⁹⁰ Source)

Board Number--Side 1A*							
Lot	1	2	3	4	5	6	Average .. Mean
101	1.60	1.55	1.70	1.60	1.55	1.97	<u>1.18</u> <u>1.66</u>
102	1.13	1.31	1.49	1.54	1.31	1.49	<u>1.19</u> <u>1.33</u>
103	1.60	1.65	1.42	1.51	1.80	1.60	<u>1.13</u> <u>1.60</u>
104	1.92	2.02	1.45	1.60	1.65	1.76	<u>1.23</u> <u>1.73</u>
201	----	1.47	1.39	1.29	1.29	----	<u>1.21</u> <u>1.36</u>
202	1.65	1.75	1.42	1.51	1.37	1.55	<u>1.13</u> <u>1.54</u>
203	1.43	1.43	1.38	1.20	1.61	1.47	<u>1.03</u> <u>1.42</u>
204	----	1.42	1.47	1.24	1.57	----	<u>1.26</u> <u>1.43</u>
301	1.56	1.60	1.38	1.56	1.33	1.47	<u>1.08</u> <u>1.48</u>
401	1.77	1.83	1.57	1.83	1.74	1.67	<u>1.16</u> <u>1.74</u>

Board Number--Side 2A							
Lot	1	2	3	4	5	6	Average .. Mean
101	1.81	1.88	1.55	1.50	1.90	1.46	<u>1.18</u> <u>1.68</u>
102	1.31	1.31	1.41	1.27	1.54	1.22	<u>1.19</u> <u>1.34</u>
103	1.33	1.28	1.42	1.24	1.37	1.37	<u>1.13</u> <u>1.34</u>
104	1.70	1.60	1.50	1.60	1.60	1.55	<u>1.23</u> <u>1.59</u>
201	----	1.76	1.67	1.62	1.97	----	<u>1.21</u> <u>1.76</u>
202	1.42	1.33	1.33	1.11	1.28	1.40	<u>1.13</u> <u>1.31</u>
203	1.43	1.34	1.23	1.43	1.13	1.23	<u>1.03</u> <u>1.30</u>
204	----	1.34	1.26	1.29	1.44	----	<u>1.26</u> <u>1.33</u>
301	1.75	1.80	1.60	1.70	1.52	1.68	<u>1.08</u> <u>1.68</u>
401	1.72	1.44	1.23	1.37	1.23	1.07	<u>1.16</u> <u>1.34</u>

*1 inch equals 25.4 mm

development) and after etching on each of two boards per lot. Conductor widths were measured at the base (the interface between the copper cladding and the epoxy laminate). Figure 21 is a typical conductor cross section showing the etched sides of a conductor. Nominal conductor widths ranged from 0.005 to 0.100 inch (0.127 to 2.540 mm), while separations ranged from 0.010 to 0.250 inch (0.254 to 6.35 mm). Mean and standard deviations were calculated along with statistical tolerance limits. Conductor-width results are listed by process category in Table 14. For single-image lots, standard deviations between lots and within lots were calculated using the analysis-of-variance technique. The data for conductor separations corresponded inversely to that for conductor widths.

The results in Table 14 represent the summations of deviations from all sizes of conductor widths. The mean deviations for the various single-image conductor widths before and after etching are shown in Figures 22 and 23. Phototool deviations on the same graph show the changes in width from phototool to developed resist. For the solder dip process (negative phototool), these widths grew 0.0001 to 0.0004 inch (0.003 to 0.010 mm), while for the solder plate process (positive phototool) they were reduced by 0.0007 to 0.0016 inch (0.018 to 0.041 mm).

The effect of etching was distinctly different for the two processes. All of the solder-plated lots showed appreciable reductions in conductor widths from etching, with a mean reduction of 0.0028 inch (0.071 mm). The solder-dipped lots had a mean growth of 0.0003 inch (0.008 mm).

Figures 24 and 25 are histograms of actual measurements of final conductor widths from two boards per lot.

Terminal Area Diameters

The average deviation of the terminal area diameters was $+0.0007 \pm 0.0014$ inch (0.018 ± 0.036 mm) for the solder dip boards and -0.0034 ± 0.0017 inch (0.086 ± 0.043 mm) for the solder plated boards.

Wedge Lengths

A wedge test pattern was included within the circuit pattern on each side of the boards to provide another indication of the capability of the processes to reproduce narrow conductors. The wedge was 1 inch (25.4 mm) long and tapered from 0.015 inch (0.381 mm) wide to zero. It was not plotted on the phototools but was added separately and was essentially full length. It had graduation marks along its side which corresponded to each 0.001 inch (0.38 mm) of width reduction. Figures 26 and 27 show the wedge definition and histograms of actual measurements of wedge length

Figure 21. Typical Conductor Cross Section (Sandia Photograph)

reductions for the two major processes. These reductions represent changes resulting from the resist exposure, resist development, and etching operations. The average reductions and standard deviations for the separate processes are shown in Table 15. As was observed with conductor widths and terminal area diameters, the wedges were significantly smaller on boards made by the solder plate process.

Legibility

A number "2" and the letter "B", that is, "2B", were plotted in several sizes to determine a realistic minimum character size for identification that can be legibly reproduced with the processes

Text continued on page 54.

Table 14. Conductor Width Deviations

Process Category	Standard Deviation	Mean	Lower Limit*	Upper Limit*	Sigma	
					Between Lots	Within Lot
Before Etch: Resist Stage						
Solder Dip and Level Lots 101 to 103	0.0006**	-0.0003	-0.0020	+0.0013	0.0002	0.0006
Tin Lead Plate Lots 201 to 204	0.0007	-0.0012	-0.0030	+0.0005	0.0003	0.0006
Step and Repeat Multi Image; Lot 301	0.0006	-0.0007	-0.0026	+0.0011	- - -	- - -
Gerber Plot Multi Image; Lot 401	0.0005	-0.0001	-0.0015	+0.0013	- - -	- - -
After Etch						
Solder Dip and Level Lots 101 to 104	0.0011	+0.0007	-0.0021	+0.0036	0.0006	0.0009
Tin Lead Plate Lots 201 to 204	0.0013	-0.0040	-0.0075	-0.0004	0.0010	0.0010
Step and Repeat Lot 301	0.0011	-0.0006	-0.0037	+0.0025	- - -	- - -
Gerber Plot Lot 401	0.0010	-0.0004	-0.0031	+0.0024	- - -	- - -

*With 90 percent confidence, 99 percent of the population of path width deviations will fall between the lower and upper limits

**1 inch equals 25.4 mm

Figure 22. Conductor Width Deviations, Single Image, Solder Dip and Level Process

Figure 23. Conductor Width Deviations, Single Image, Solder Plate and Level Process

Figure 24. Path Width Deviations From Nominal, Lots 101 Through 104, 301, and 401 (Solder Dip and Level)

Figure 25. Path Width Deviations From Nominal, Lots 201 Through 204 (Tin-Lead Plated)

used in this study. The character height and line width combinations tested are given in Table 16. The results indicate that the optimum character size is 0.096 inch high by 0.015 inch wide (2.438 by 0.381 mm).

Copper Adhesion

Process Specification 9928013 specifies that no obvious separations shall exist between the base material and the copper cladding, and between the copper cladding and the copper plate.

Figure 26. Reduction of Test Wedge Lengths and Widths, Lots 101 Through 104, 301, and 401 (Solder Dip and Level)

Figure 27. Reduction of Test Wedge Lengths and Widths, Lots 201 Through 204 (Tin-Lead Plated)

Table 15. Wedge Length Reductions

Characteristic	Boards Measured	Mean*	Standard Deviation
Solder Dip and Level, Single Image	190	-0.0026	0.0007
Solder Dip and Level, Lot 301	64	-0.0033	0.0006
Solder Dip and Level, Lot 401	64	-0.0024	0.0006
Solder Plate and Level, Single Image	183	-0.0055	0.0007

*1 inch equals 25.4 mm

Inspection by microscope of 10 sectioned and mounted conductors from each of 22 PWBs (representing 11 lots) revealed no adhesion discrepancies. (Many 0.005-inch conductors were detached from the base material but were not considered a rejectable characteristic because 0.005-inch conductors are not allowed under Process Specification 9928013.) One 0.010-inch conductor was lifted on one board.

Board Flatness

All boards met the requirement of Process Specification 9928013 that the maximum warp and twist from a true plane not exceed 0.010 per inch for a 0.062-inch (1.575 mm) nominal board thickness.

Visual Defects

The finished boards received 100-percent visual inspection at Bendix without prior screening to remove boards with obvious workmanship defects, as is customarily done with production boards. After inspection at Bendix, the boards received a second visual inspection at SLA. Defects then were classified according to the degree of severity.

- Rejectable: A defect which either prevents the board from fulfilling its electrical function or which degrades (or has the potential to degrade) the electrical performance of the board under adverse environmental or electrical conditions. Examples: a broken or missing conductor, a bridged conductor, a very high resistance or an open circuit in a plated-through-hole, an indentation in a conductor which covers an appreciable fraction of the conductor width, a circuit pattern projection which reduces the minimum spacing below the specified minimum, and conductive foreign material.

Table 16. Character Height
and Line Width
Combinations

Height*	Line Width	Legibility
0.048	0.015	Poor
0.048	0.020	Nil
0.072	0.015	Fair
0.072	0.020	Poor
0.096	0.015	Good
0.096	0.020	Fair
0.096	0.025	Poor
0.120	0.015	Good
0.120	0.020	Good
0.120	0.025	Fair
0.192	0.020	Good
0.192	0.025	Good

*1 inch equals 25.4 mm

- Marginal: A defect which may increase component assembly time or is a potential source of degradation of circuit performance in a corrosive environment. Examples: solder-plugged holes, scratches or exposed copper on conductors, particulate matter attached to the board surface, and residual or corrosive salts in non-critical locations.

Of 183 boards processed using the solder dip and level process, 15 (8 percent) were rejectable and 13 (7 percent) were marginal. The solder plate and level process was used for 93 boards; of these, 11 (12 percent) were rejectable and 6 (6 percent) were marginal. A total of 276 boards were processed; 26 (9 percent) were rejectable, and 19 (7 percent) were marginal.

It should be noted that excessive handling of these boards during the in-process inspection operations could have contributed to the incidence of visual defects. This is especially true when handling boards in the resist stage (after exposure and development).

ACCOMPLISHMENTS

The results of this study have shown that the standard process can reliably produce double-sided, plated-through-hole printed wiring boards. The control documents (Process Specification 9928013, Design Guide 10011, and Design Standard D 10220) are adequate for the solder dip and level process.

Other significant findings are as follows.

- The standard process will yield product to tighter tolerances than the requirements of the above documents. Tighter tolerances must be negotiated through the Process Knowledgeable Groups of the design and manufacturing agencies.
- Nondestructive testing offers significant cost and quality benefits in board inspection related to plating thickness in plated-through-holes.
- Boards produced to the solder dip and level process had significantly less deviation from nominal of conductor widths and terminal area diameters than boards produced to the solder plate and level process.
- Final inspection results indicate the capability of the Engineering Shop to produce boards which meet the quality requirements of the standard process specification. (The current-time used by the Engineering Shop on these boards was not sufficient to guarantee a hole wall copper thickness above a 0.001 inch minimum. A change has since been made which should provide a mean thickness of 0.0015 inch.)

FUTURE WORK

The following recommendations, resulting from this study, are presently in work.

- Continued study of dry film resists to reduce or eliminate defects related to missing copper in PTH holes and open or bridged conductors.
- Further study of probe geometry for nondestructive testing will be completed to minimize or eliminate errors associated with resistance testing of large hole diameters, small annular rings, and thin laminates.
- Beta backscatter measurement of plating thicknesses will be developed to provide the capability for checking clad and plated copper during processing.

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