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CADMIUM SULFIDE/COPPER SELENIDE CELL RESEARCH

COPPER SELENIDE-BASED THIN FILM SOLAR CELLS

(XG-Ø-9216-1)

First Quarterly Technical
Progress Report
June 1, 1980 - September 1, 1980

MASTER

Boeing Aerospace Company
P. O. Box 3999 M/S 88-43
Seattle, Washington 98124

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S. P. Sauve' - Program Manager

R. A. Mickelsen - Technical Leader

J. M. Stewart

W. S. Chen

DISCLAIMER

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CADMIUM SULFIDE/COPPER SELENIDE CELL RESEARCH

Reid A. Mickelsen
John M. Stewart
Wen S. Chen

Boeing Aerospace Company
P.O. Box 3999 M/S 88-43
Seattle, Washington 98124

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Abstract

The objective of this program is to investigate the use of $Cu_{2-x}Se$ to produce low cost, high efficiency photovoltaic solar cells. This program is the first phase of an effort leading to the development of low cost thin film arrays. The goal is to: (1) develop a polycrystalline thin film photovoltaic device capable of 10% conversion efficiency, (2) demonstrate feasibility of large scale production at a cost of approximately $0.30/watt.

The $Cu_{2-x}Se$ films are produced by coevaporation of Cu and Se from separate, individually controlled vapor sources onto heated glass substrates. This method gives greater composition controllability and is readily adaptable to large scale production efforts. Two quartz crystal microbalances are used to separately monitor the Cu and Se deposition rates.

The structural, electrical, and optical properties of the $Cu_{2-x}Se$ films have been measured for deposits made on 250°C substrates. The optical absorption measurements shows the material having an indirect band gap of 1.4ev and a direct gap of 2.2ev. These values are for stoichiometric indices in the range of $0.17 \leq x \leq 0.26$. Hall and conductivity measurements give hole mobilities in the range of 3-7 $cm^2/Vsec$ and hole densities of the order of 4×10^{22} cm^{-3}. For deposits made on substrate at 160°C, the mobility is in the range of 3-10$cm^2/Vsec$ and hole densities on the order of 10^{19} to 10^{21} cm^{-3} for $0.1 \leq x \leq 0.3$.

The stoichiometric parameter, "x", was determined by coulometric measurements. A highly significant experimental result is that the $Cu_{2-x}Se$ film composition saturates at an "x" value in the range of 0.22 to 0.26 for a substrate temperature at 250°C and at a high Se deposition rate. For $Cu_{2-x}Se$ deposits on substrates at 160°C, no saturation effect is observed.

The cell efficiency has been recently improved from less than 1% to 3.3%. Earlier cells formed by depositing $Cu_{2-x}Se$ on CdS at 250°C have low short circuit current (< $4mA/cm^2$) and poor fill factor (< 0.4) with high series resistance. Recent improved cells were achieved by the

following procedure: (1) a Mo/Au film grid was sputtered onto Corning 0211 glass; (2) an ITO film was RF sputtered to a thickness of 1000Å with sheet resistivity of 10Ω/□; (3) a CdS film was deposited, removed from the vacuum chamber and etched in 10% HCl for 40 sec; (4) $Cu_{2-x}Se$ was evaporated onto the CdS at a substrate temperature of 160°C; (5) a solid gold film electrode formed the final layer. To date, the best cell has photovoltaic characteristics of J_{sc} = 11.6mA/cm^2, V_{oc} = 460mV, F.F. = 0.62 and η = 3.3% as tested under simulated AM1 illumination.

It has become apparent that the $Cu_{2-x}Se$ must be deposited on low temperature substrates or significant deterioration of cell performance occurs. This is most likely due to diffusion of Cu into the CdS film. In addition, texturing of the CdS film by etching in HCl is an important step.

1.0 SUMMARY

The major results for the reporting period June 1, 1980 through September 1, 1980, can be summarized below:

a. It has become apparent that $Cu_{2-x}Se$ must be deposited on substrates at less then 200°C temperature. This is most likely due to diffusion of Cu into CdS.

b. Electrical properties of $Cu_{2-x}Se$ deposited on a substrate at 160°C have been measured. The results show a region of high resistance for small values of the stoichiometric index "x". Device output is highest for the high resistance $Cu_{2-x}Se$.

c. Cell efficiency has improved from less than 1% during the last report period to 3.3% at present (AM1 illumination).

2.0 INTRODUCTION

This is the first quarterly report of a 12-month research program to investigate the use of $Cu_{2-x}Se$ to produce low cost, high efficiency photovoltaic solar cells. This program is the first phase of an effort leading to the development of low cost thin film arrays. The goal is to: (1) develop a thin film photovoltaic device capable of 10% conversion efficiency, (2) demonstrate feasibility of large scale production at a cost of approximately $0.30/watt.

$Cu_{2-x}Se$ has a number of characteristics that give it excellent potential for yielding a 10% efficient solar cell. Band gap measurement by previous investigators have found values in the range of 1.1 to 1.29eV[1,2]. Measurements by this laboratory have given values of 1.4eV for the indirect band gap and 2.2eV for the direct band gap. The f.c.c. structure obtained has a lattice constant of a = 5.76Å. This will then give a very small lattice mismatch with the N-type CdS layer. With the use of N-type CdS, consideration of the electron affinity of the materials shows there will be no detrimental interfacial spike in the conduction band between the two materials.

Specific objectives of this contract are: (1) development of the $Cu_{2-x}Se$ thin film deposition process; (2) characterization of the electrical, optical, and structural properties of the $Cu_{2-x}Se$/CdS films; (3) the fabrication of $Cu_{2-x}Se$/CdS cell structures; (4) perform theoretical and experimental modeling of the $Cu_{2-x}Se$/CdS heterojunction, making detailed measurements so that the mechanisms that limit the conversion efficiency of the cell can be determined; (5) produce a 6% efficient cell by the end of the contract.

3.0 TECHNICAL DISCUSSION

3.1 CdS/$Cu_{2-x}Se$ Film Formation

The $Cu_{2-x}Se$ film was produced by simultaneous coevaporation of Cu and Se in elemental form. When $Cu_{2-x}Se$ was deposited onto CdS at 250°C, it appeared that there may be some $_{2-x}$ diffusion of the Cu into the CdS. Devices made with $Cu_{2-x}Se$ deposited on a substrate at 250°C show a large cross over effect. This is indicative of an "overbaked" condition. As a consequence of this probable diffusion process, the substrate temperature was lowered to 160°C. No cross over was then observed after the device was formed. If the device was baked at 200°C in a H_2/Ar ambient for more than 15 minutes, a "cross over" behavior was again observed.

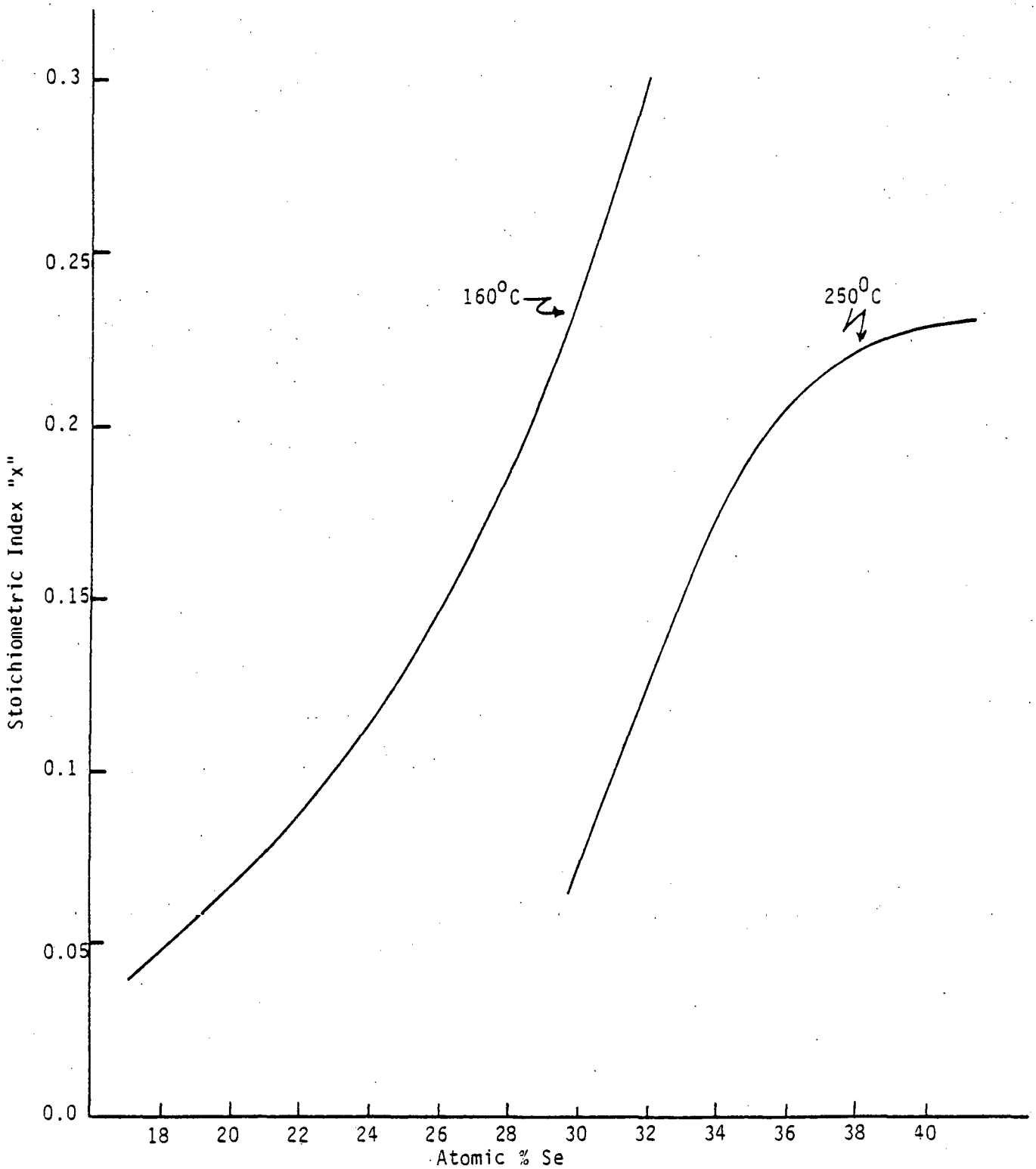
When $Cu_{2-x}Se$ was deposited on a substrate at 250°C, careful control of the deposition procedure was not required. Any excess Se would saturate to a "χ" value of approximately 0.2. With the lower substrate temperature no saturation effect is observed. A plot of the film composition (determined by coulometric techniques[3]) versus the quartz crystal reading shows this effect in Figure 1. More careful control of the Cu and Se rate of evaporation is now required for deposition on the lower temperature substrate. In the past, a rather massive gold plated copper ring was used as an evaporation source for the Se. This massive ring source would not give the necessary rate control for the Se evaporation needed to give $Cu_{2-x}Se$ films of uniform composition across the substrate and through the film. Two small tungsten boats are now connected in series and appear to give the needed rate control.

The CdS/$Cu_{2-x}Se$ devices made in the past have been plagued by low open circuit voltage and high series resistance. We believe that most of this problem can be traced to the high resistance of the CdS film. In an effort to lower the resistance of the CdS film it was baked in an ultrapure H_2 atmosphere at 400°C. These efforts were not successful.

A new CdS source has now been designed and appears to be capable of making very low resistance CdS films with very few pinhole defects. A schematic of the CdS source appears in Figure 2. The CdS powder is placed in a quartz tube with an aperature of approximately 1mm in diameter. A Mo sheet wrapped around the quartz tube provides the heat. A carbon cloth is placed between the heater and the quartz tube to minimize breakage of the tube due to any non uniformity in heating. Radiation shields are placed around the entire source to minimize power requirements. A Mo plug is placed in each end of the tube. Since the Mo plug is cooler than the tube, the CdS will quickly seal the tube end. The source is capable of temperatures to 1200°C.

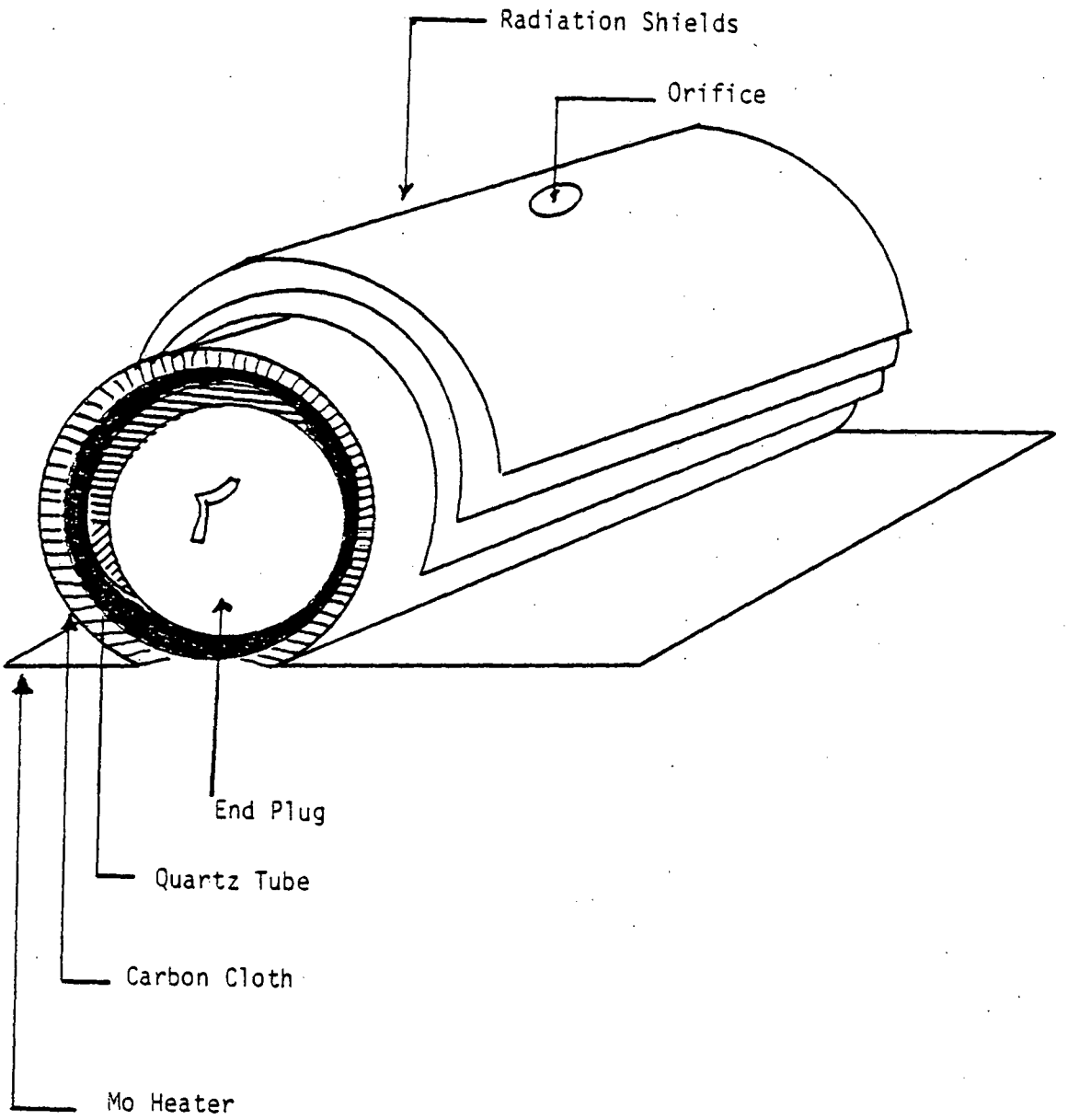
3.2 CdS/$Cu_{2-x}Se$ Characterization

Measurements of the resistivity vs. source temperature have been made on the CdS films produced by the new evaporation source. The source is capable of reproducibly making high to low resistance films (3Ωcm) dependent on the source temperature. These results are shown in Figure 3.



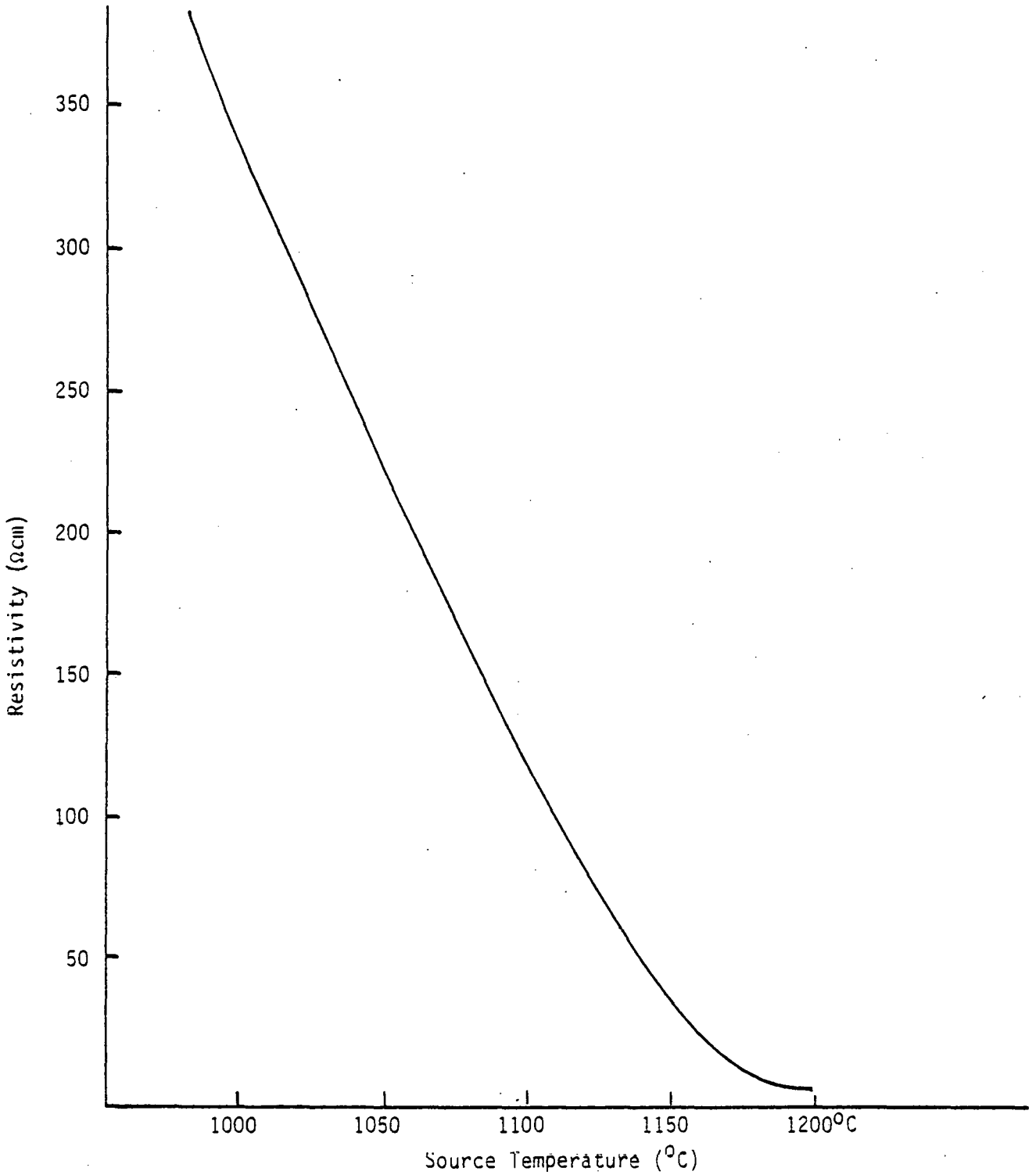
Stoichiometric Index "x" vs. Atomic % Se as Determined by Quartz Crystal Microbalance

Figure 1



CdS Evaporation Source

Figure 2



Resistance of CdS Film vs CdS Source Temperature

Figure 3

Electrical properties of $Cu_{2-x}Se$ deposited onto 160°C substrates have been measured. A plot of stoichiometric index "χ" versus resistivity shows a high resistance near χ approximately 0.1 (Figure 4). One would expect the resistance to be a maximum near $\chi = 0$, however, we observed some Cu nodule formation in the range $0 \leq \chi \leq 0.1$. While the best match of the $Cu_{2-x}Se$ lattice to CdS lattice occurs for χ approximately 0.2, there are indications that total device performance may be higher near χ equal to 0.1.

The carrier concentration was determined by the Van der Pauw technique.[4] The carrier concentration was approximately 10^{20} holes/cm^3 for all values of χ except near χ equal to 0.1. At this value of χ the carrier concentration dropped to 10^{18} holes/cm^3. The mobility was approximately 10 cm^2/vsec.

3.3 Cell Construction and Analysis

3.3.1 Cell Construction

Earlier cells were fabricated by first depositing CdS onto Mo/Au gridded glass substrates and subsequently depositing the $Cu_{2-x}Se$ onto CdS at 250°C. Problems associated with this process are unreliable Au/CdS contacts, high series resistance and a low photocurrent.

During this quarter, a new fabrication process has been developed. A schematic of the cell layers in Figure 5 shows the procedure used in making the improved cell. First a Mo/Au grid is sputtered onto the Corning 0211 glass substrate (Figure 5a). An ITO film is sputtered to a thickness of 1000Å and a sheet resistivity of 10 Ω/□ (Figure 5b). The CdS film is deposited to a thickness of 11μm (Figure 5c). The substrate is then removed from the vacuum system and etched in 10% HCl at room temperature for 30 sec. The $Cu_{2-x}Se$ film is then evaporated onto the CdS at a substrate temperature of 160°C (Figure 5d). Finally a gold electrode is placed on top of the $Cu_{2-x}Se$ film (Figure 5e). A cross section of the back wall cell structure is shown in Figure 6.

3.3.2 Cell Characteristics and Analysis

Since the last report, a substantial improvement in cell performance has been achieved. Earlier cells made by depositing $Cu_{2-x}Se$ onto CdS at 250°C had low short circuit currents (< 4mA/cm^2), poor fill factors (< 0.4) and, hence, low efficiencies (< 1%). The poor fill factor is mainly due to the high series resistance from the high sheet resistivity CdS and the low short circuit current is attributed to excess Cu diffusion into the CdS caused by the high substrate temperature deposition of $Cu_{2-x}Se$.

These deficiencies have been corrected by adopting the new cell fabrication procedure described in the last section. A low resistivity ITO layer has been introduced to reduce the series resistance. In order to enhance the short circuit current, the deposition temperature of $Cu_{2-x}Se$ has been reduced and the CdS surface has been textured. Cells fabricated from the new process show greatly improved performance with J_{sc} > 10mA/cm^2 and F.F. > 0.6.

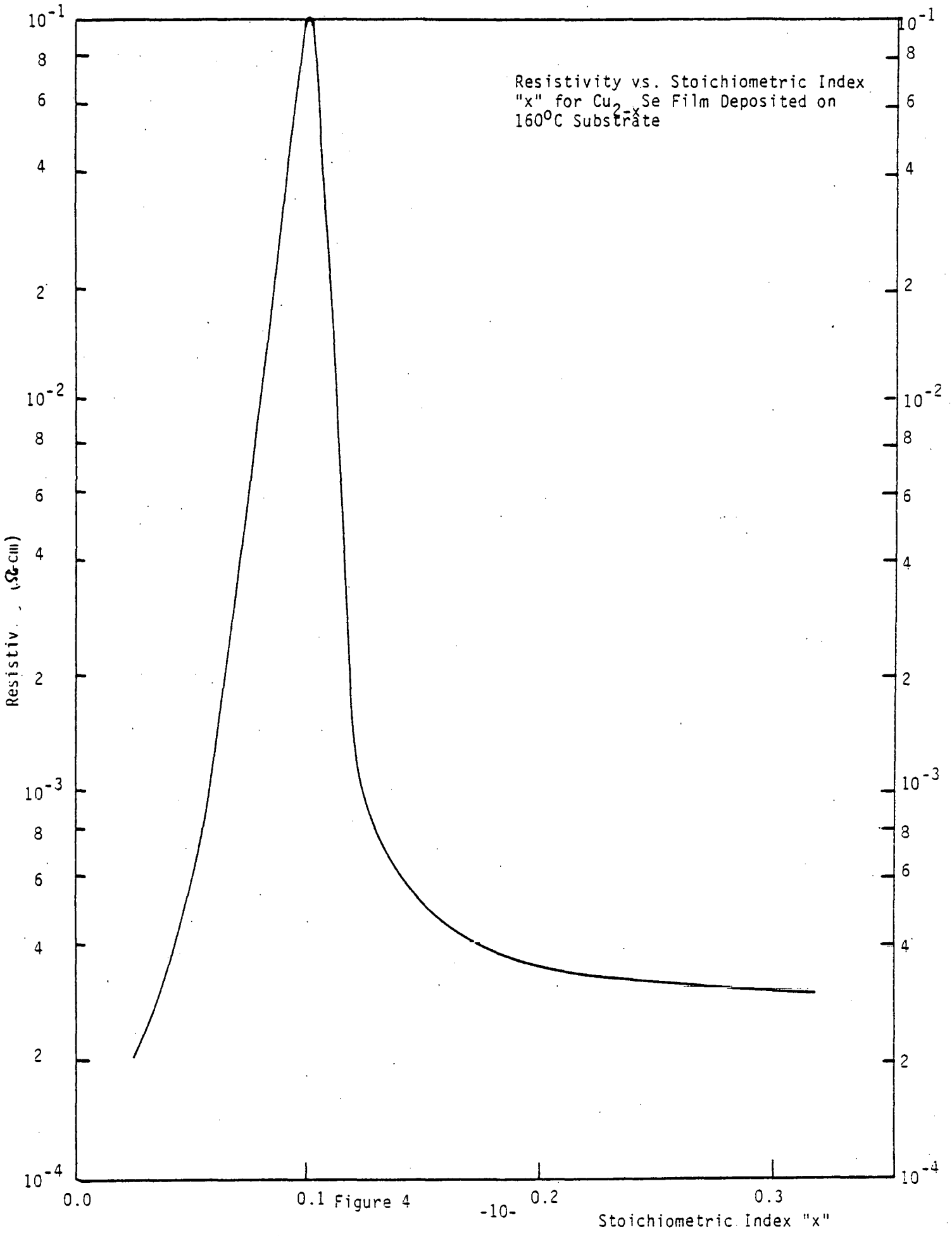
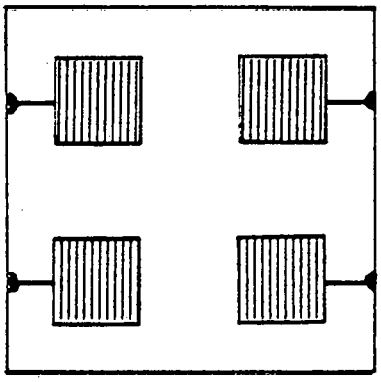
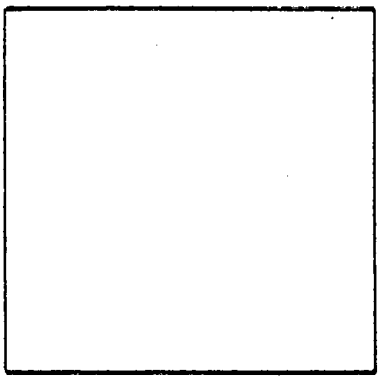

Resistivity vs. Stoichiometric Index "x" for $Cu_{2-x}Se$ Film Deposited on 160°C Substrate
Resistivity (Ω-cm)
10^{-1}
8
6
4
2
10^{-2}
8
6
4
2
10^{-3}
8
6
4
2
10^{-4}
0.0
0.1
0.2
0.3
Stoichiometric Index "x"

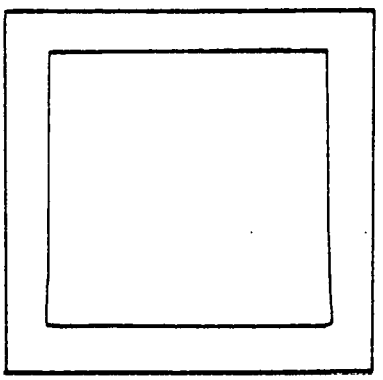
Figure 4



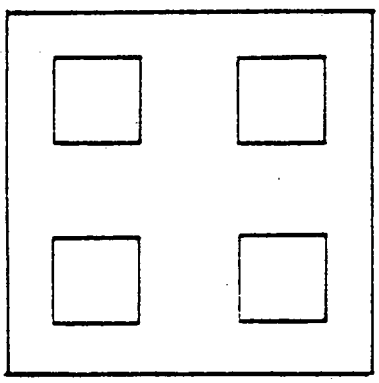
(a) Base metallization grid Mo/Au



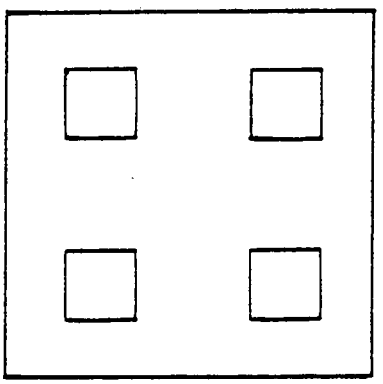
(b) ITO film



(c) CdS film



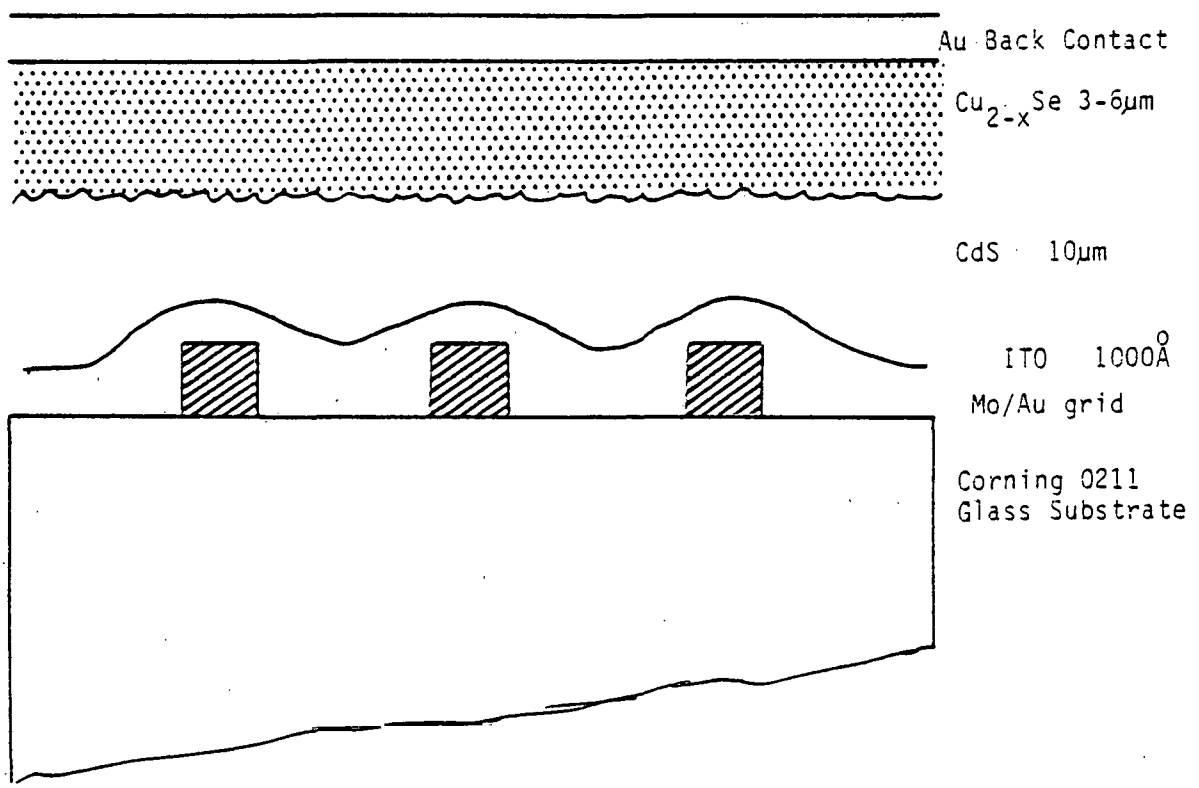
(d) $Cu_{2-x}Se$ film



(e) Au top electrode

Solar Cell Test Structure, 1 cm^2 Area Cell
Back Wall Design

Figure 5



Back Wall Cell Structure

Figure 6

In Figure 7, the photovoltaic characteristics of an improved cell are shown. To indicate the progress, the characteristics of an earlier cell made at the end of the last contract are shown on the same figure. The most recent cell is of the back wall type (no AR coating) with:

V_{oc} = 0.46V

J_{sc} = 11.6mA/cm^2

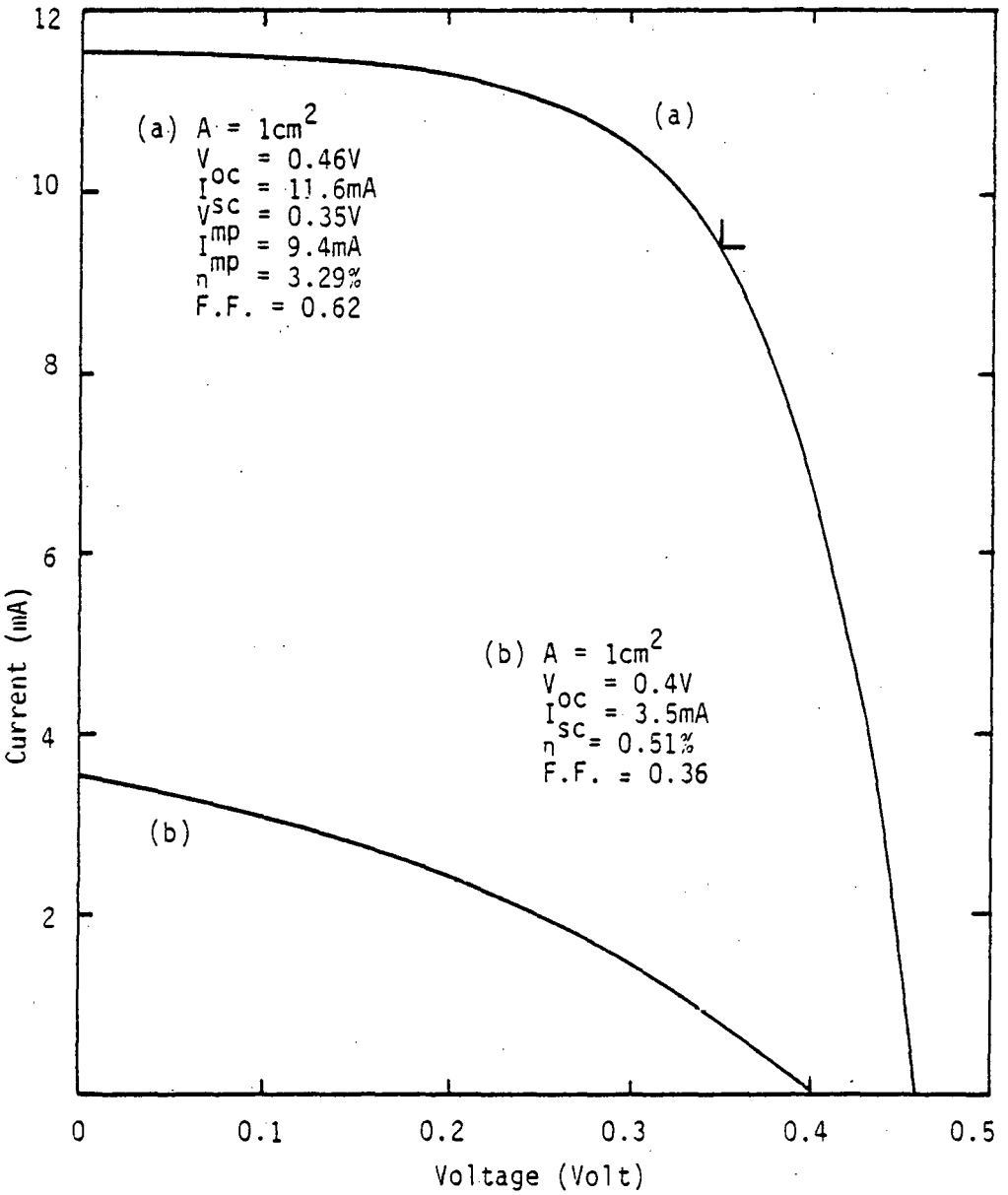
F.F. = 0.62

η = 3.29% (total area)

under simulated AM1 (ELH Lamp, 100mw/cm^2) illumination. The cell had optimum performance without any baking after deposit.

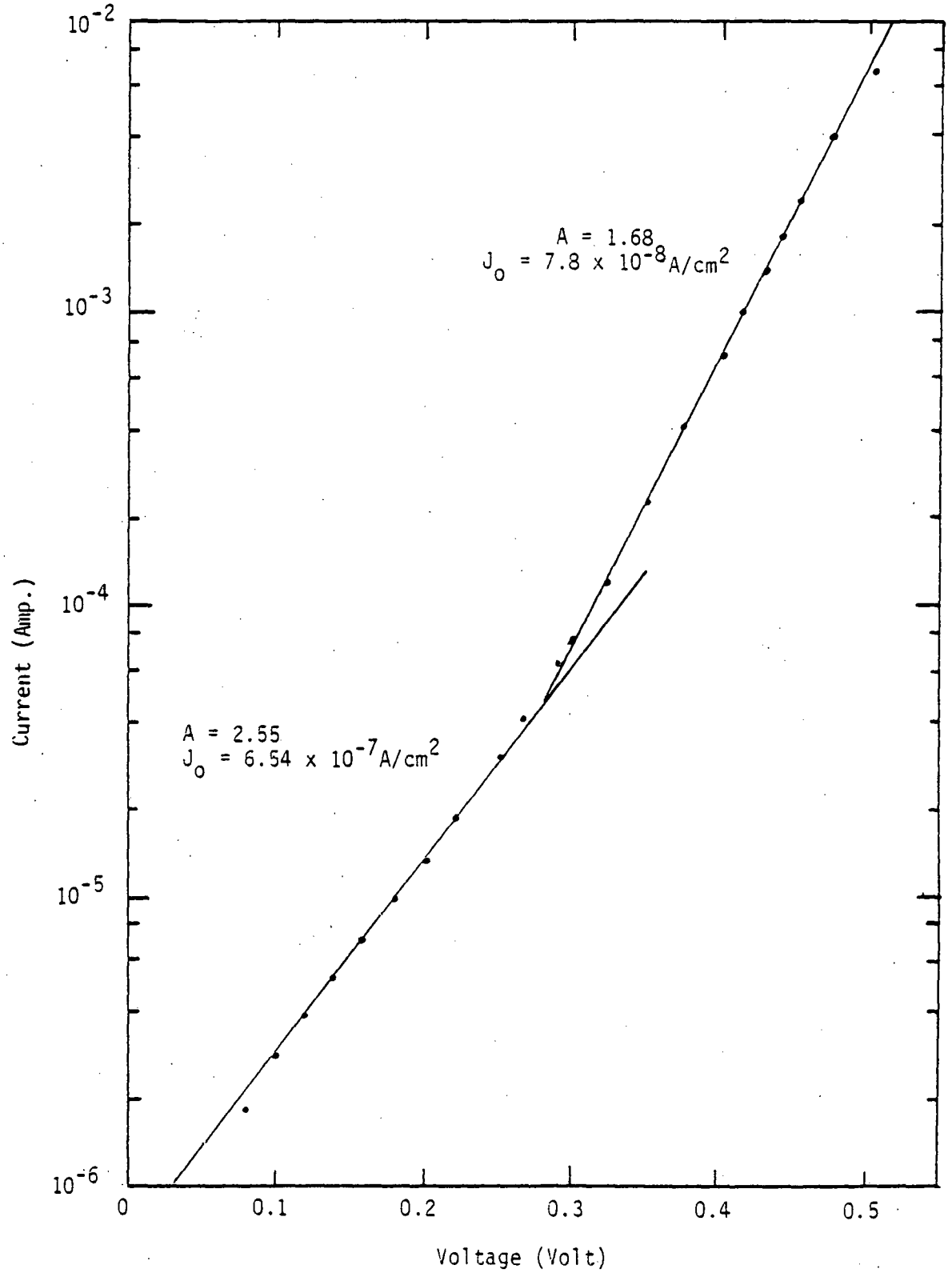
The dark I-V characteristics of this cell have been measured and are shown in Figure 8. Two diode characteristics have been observed. In the low current region (< 4 x 10^{-5}A/cm^2), the diode factor, A, is 2.55 and the reverse saturation current, J_o, is 6.54 x 10^{-7}A/cm^2. In the high current region (> 4 x 10^{-5}A/cm^2) the A factor is 1.68 and J_o is 7.8 x 10^{-8} A/cm^2.

The effects of heat treatment in H_2/Ar on this cell have been studied. After 5 minutes at 175^{o}C, the open circuit voltage increased to 500mv but the short circuit current decreased to 6.5mA/cm^2. Further treatment at 150^{o}C for 20 minutes degraded the current to 3.2ma/cm^2 with a minor decrease of V_{oc}(480mv). Detailed studies of this cell have been hindered due to the overbaking.



Photovoltaic characteristics of $Cu_{2-x}Se/CdS$ cells under simulated AM1 illumination.
(a) Improved Cell (b) Earlier Cell

Figure 7



Dark I-V Characteristics of Recent $Cu_{2-x}Se/CdS$ Cell

CuSe/CdS
223 · 0
6/12/80

Figure 8

4.0 REFERENCES

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4. H. H. Wieder, Thin Solid Film, 31 (1976), 123-138.

5. R. B. Hall, R. W. Birkmire, E. Eser, T. L. Hench and J. D. Meakin, 14th IEE Photovoltaic Specialists Conference, San Diego, California, 7-10 Jan 1980, pg. 706-714.

5.0 PLAN FOR NEXT QUARTER

Since the depletion layer is mostly in the CdS region, the properties of this material will be most crucial to optimum device performance. A thorough investigation of the CdS will be done with particular emphasis on an examination of the photoluminescent spectra. It appears that for optimum device performance of the Cu_2S/CdS cell, the CdS should have a particular photoluminescent spectra.[5]

Further investigation will be done on the optical absorption properties of $Cu_{2-x}Se$ deposited on low temperature substrates (160^oC) the band gap of the material will be examined as a function of material composition.