PROGRAMMABLE COMBINATIONAL LOGIC TRIGGER SYSTEM FOR HIGH ENERGY PARTICLE PHYSICS EXPERIMENTS

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Abstract

A fast logic system designed to select predetermined combinations of three hits in three detectors is described. Central to this system is a random access memory IC that was especially designed for this application.

Introduction

In many high energy particle physics experiments involving scintillation counter hodoscopes, proportional wire chambers and spark chambers, it is necessary to generate triggers on the basis of space correlated signals from several detectors. This requirement is used in addition to the usual time correlation in order to select event candidates with the topological characteristics of the final states involved.

For many years experimenters in high energy particle physics have used two dimensional diode or transistor gate arrays or matrixes to define tighter trigger conditions for a wide variety of experimental situations. Usually these matrixes were used with scintillation counter hodoscopes of 10 to 50 or so elements each to define coplanarity or opening angle of two particles or to ensure the right charge of an outgoing particle in a magnetic field. These diode or transistor arrays were practical as long as the number of elements in each detector was not too large (~ 50) and a two-fold combinational logic system was capable of defining the trigger sufficiently tightly.

High energy physicists have been looking for a means to make a high speed three dimensional space correlation to gain an additional degree of freedom for trigger selection logic. The need for high speed decision making (250 nsec or less) comes about from the necessity to trigger spark chambers and other short memory detection systems.

Advances in microelectronic technology have made possible an enormous increase in the number of elements in matrix arrays as well as the extension into a third dimension. Now it is possible to construct a logic system of combinations of three with 10^6 to 10^7 possible combinations. This is accomplished with the use of a special static random access memory (RAM) integrated circuit designed to allow simultaneous access to any or all locations. The memory is organized as a square array of 256 bits. That is, addressed by 16X and 16Y address lines that are brought outside the IC package. The output of the RAM is the logical NOR of all locations that are addressed in one read cycle. Thus the RAM is the equivalent of a 16 by 16 diode or transistor two-fold gate array, the outputs of which are NOR tied together (Fig. 1). In the RAM the two-fold AND gates are present whenever logical "ones" have been programmed into the memory. Logical "zeros" correspond to the absence of AND gates.

The RAM Device

Central to the development of this programmable combinational logic trigger system is the idea of

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Figure 1 Two-dimensional Gate Matrix

using a semiconductor RAM as a two-dimensional gate matrix. To accomplish our purpose of simulating a gate matrix where a logical "1" corresponds to the presence of a two-fold AND gate on the corresponding address lines, a special IC was designed. The RAM is organized as a square array of static flip-flops, the contents of which are gated by the address lines to an OR (NOR) output. A conventional RAM of 256 bits would internally be a 16 by 16 array of flip-flops. Since only one location in the RAM is ever addressed in a single read cycle, the address lines are internally decoded from two 4-bit binary inputs. Our special IC has all 32 address lines brought out to 32 terminals so that more than one location can be addressed in one read cycle (corresponding to more than one particle through the detector array). At the IC circuit level this required a new memory cell design that would allow simultaneous access to several cells without altering the contents of the simultaneously addressed cells.

The RAM IC to meet these requirements we specified as indicated in Table I and was designed and put into production by Synertek.¹ It proved economically advantageous to organize the memory as two 256-bit arrays in one IC with common address lines but separate input and output terminals. Thus each IC is a three-dimensional array of 16 by 16 by 2 elements. The pin layout is shown in Fig. 2. The output circuit is a NMOS transistor which allows a wire NOR tie of as many as 8 RAM's without exceeding the 140 ns worst case access time specification.

Two hundred prototypes were constructed and extensively tested both by Synertek and BNL. The specifications of Table I were easily met by all circuits under worst case address combination conditions. The 200 prototype IC's were exercised for 7 days at 120°C and no failures occurred. Propagation delays become longer at elevated temperatures (10 nsec at 50°C) but all circuits remained functional even at 120°C.

A two-dimensional matrix of 128 by 128 elements requires only 64 RAM IC's, while a diode or transistor

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TABLE I

16 x 16 x 2 RAM IC Synertek C10115

Input

$V_{in\ low}$	less than .4 volts
$V_{in\ high}$	greater than 2.4 volts
I_{in}	less than 2 μ a from 0-5 volts
C_{in}	less than 7 pf

Output

$V_{out\ low}$	less than .45 volts at $I = 6.5\ ma$
Data access time	less than 140 ns with 8 way "wire OR" and one standard TTL load

Power

V_{cc}	5 volts $\pm$ 5%
I_{cc}	less than 75 ma

All inputs are positive logic, output is NOR of addressed cells.

Figure 2 Random Access Memory Integrated Circuit Pin Layout

matrix of this size would require 16,000 possible gate intersections. A pattern or 5% filling of the matrix

would mean physically putting into position 800 diodes or transistors, a task that severely discourages ever changing the pattern. With the RAM array, the pattern is changed simply by programming a different set of "1"s and "0"s.

Sixty-four IC packages can be readily mounted on a single printed circuit board (Fig. 3). Now it becomes

Figure 3 Printed Circuit Board with 64 RAM IC's. Each IC is a 16 by 16 by 2 Memory Array.

possible to construct a three-dimensional combinational logic system simply by making one such PC board for each element in the third-dimension. Logically this means forming a two-fold AND function between the OR output of each two-dimensional array and a corresponding element in the third-dimension, then taking an OR of all such AND gates (Fig. 4). Thus for each element

Figure 4 Three-dimensional Gate Matrix

in the third-dimension (third detector set) the RAMS are programmed to have "1"s at the appropriate combinations in the other two dimensions (first and second detector sets).

This three-dimensional array of programmed AND gates makes possible trigger arrangements that define any combination of three projected points in space. For example a topological arrangement of two or three particles in space or to define angle-momentum correlations of one or more particles. It should be noted that unlike some digital arithmetic logic systems this

three-dimensional programmable matrix array will respond correctly in the presence of arbitrary numbers of simultaneous particles. Additional particles simply increase the probability of accidentally hitting a combination that was programmed into the array. This probability of accidental combinations is an ambiguity that exists in the detectors and is not introduced by the RAM array.

The System

The three-dimensional trigger systems in use at BNL are organized as 128 by 128 by 128 input matrices (Fig. 5). The detector outputs (mostly MWPC's) are strobed into a fast register which serves to address the RAM's. 180 ns later the overall OR tree is strobed to see if any of the addressed combinations contain logical "one's".

Figure 5 128 x 128 x 128 Trigger Matrix with Computer Interface

The pattern of "0"'s and "1"'s is loaded and tested by switching the RAM address lines to a set of buffers that are driven by a large remote computer (PDP10). Normal operating procedure is to load the RAM's from the computer at the beginning of an experimental run, then, during the time interval between accelerator beam spill cycles (~ 1 sec) the contents of the RAM are tested to ensure that noise pulses haven't altered the pattern.

Application

Several experiments have been approved to run on the BNL MPS (Multi-Particle Spectrometer) that will use one or more of these 128 x 128 x 128 array combinational logic trigger systems. These experiments illustrate some of the wide variety of application possible with this device.

The MPS has been described in detail elsewhere.² Fig. 6 is a general layout of the MPS where trigger

Figure 6 Trigger Detector Configurations for Three Experiments in the MPS

detectors for three different experiments have been overlayed to show the use of the RAM matrix in each trigger system.

Forward K^+

This trigger requires combinations of 128 elements in TPX2 with 45 elements of H4-C6 and 112 elements in H5. TPX2 is a multiwire proportional chamber and H4, H5 are scintillation counter hodoscopes. The purpose is to require a positive particle between 3 and 10 GeV/c that isn't detected by C6. C6 is a threshold Cerenkov hodoscope of 10 cells that detects particles with $\gamma > 20$. Thus only a K^+ or p^+ will pass the trigger selection criterion since a π^+ above 3 GeV/c will be detected by C6 and thus rejected.

Recoil Proton

This trigger is designed to require a recoil particle in P1, P2 and P3 that has the appropriate scattering angle and momentum correlations which correspond to a recoil proton with missing mass and momentum transfer in a predetermined range. P1, P2 and P3 are MWPC's with 128, 256 and 128 elements respectively. The MPS detectors will be triggered with this signature so that the behavior of this missing mass can be measured.

Forward Electron

This detector uses two MWPC transition radiation detectors, TR1, TR2 and H4 to require the spatial correspondence of a forward going electron or positron, so that the MPS can be triggered on events which include an electron or positron with momentum greater than 3 GeV/c in the final state.

It is interesting to note that by linearly adding the signals from the AND gates between the two-dimensional arrays and the third dimension detector rather than performing a logical OR, one can require more than one of the required combinations to occur in the same event. Thus, in the K^+ trigger example, two K's could be required or in the electron example, two electrons or an electron-positron pair could be selected. It should also be noted that additional particles detected only increase the chance of an accidental trigger and do not increase the time required to select a trigger or reduce the efficiency for detecting valid combinations.

Conclusion

We have developed a fast three-dimensional programmable combinational logic array for use in three-way topological trigger systems. Central to this program is our success (along with Synertek) in producing a cost effective RAM IC that accurately simulates the characteristics of a gate matrix.

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