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ORELA Data Acquisition System Hardware

Vol. 5: SEL 810B/PDP-4/PDP-9 Intercomputer Link

J. W. Reynolds
J. H. Holladay

OAK RIDGE NATIONAL LABORATORY

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ORELA DATA ACQUISITION SYSTEM HARDWARE

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J. W. Reynolds and J. H. Holladay

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REA

Other volumes in this series of reports on *ORELA Data Acquisition System Hardware* are:

ORNL/TM-5638	Introduction
ORNL/TM-5639 (Vol. 2 of ORNL/TM-5638)	Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)
ORNL/TM-5640 (Vol. 3 of ORNL/TM-5638)	Scaler Interfaces (Q-5036-1, -2, -4 through -11, -29, and -30)
ORNL/TM-5641 (Vol. 4 of ORNL/TM-5638)	ORELA Device Controllers (Q-5098)
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ORNL/TM-5644 (Vol. 7 of ORNL/TM-5638)	Instruction Manual for the Multiplexer Channel and Scaler Interface Tester (Q-5130)
ORNL/TM-5645 (Vol. 8 of ORNL/TM-5638)	Instruction Manual for the Ground Isolation Driver and Receiver Cards on the Quiet Ground System at ORELA

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ABSTRACT

This report describes the IOT assignments and programming for the PDP-4 and PDP-9, the ground isolation wiring, the connector pin assignments, a simplified theory of operation for the SEL 810B link interface, a detailed theory of operation for the link interfaces at the PDP-4 and the PDP-9, and the use of the PDP-4 and PDP-9 link interfaces as an input to the SEL 810B Four-Channel Priority Multiplexer.

1. INTRODUCTION

The ground-isolated, asynchronous, 16-bit parallel transfer inter-computer link between an SEL 810B and the PDP-4 or PDP-9 provides the PDP computers with the capability to use the peripherals on the SEL 810B for such things as reading cards, listing, plotting, transferring information to or from magnetic tape, and transferring data files to the Immediate Analysis and Coordinating Computer.¹ Simultaneous transfer of data, by both PDP computers, is not possible.

The intercomputer link, attached to the SEL 810B designated as the Peripheral Equipment Controller (PEC), has been built in five parts: three interfaces, one each in the SEL 810B, the PDP-4, and the PDP-9; and two ground isolation² modules constructed in NIM hardware, one located at the SEL 810B and the other located near the PDP-4. The ground isolation for the PDP-9 is part of its interface. The three interfaces are shown in SEL Drawing Series 53422 for the SEL 810B (ORNL Instrumentation and Controls Division Drawing Series Q-5187 consists of sepia copies of the SEL drawings) and in ORNL I&C Division Dwg. Nos. Q-2956-30 through -38 for the PDP-4 and Q-5072-1 through -4 and -17 for the PDP-9. The drawings are listed in Tables 1, 2, and 3.

Table 1. SEL 810B Intercomputer Link Interface drawings
ORNL I&C Division Drawing Series Q-5187
Revised Sepias of SEL Drawing Series 53422

Number	Title
-1	Unit I/O Sync Logic, PDP-4 Link
-2	Sync Logic, PDP-4 Link
-3	BTC Interface, PDP-4 Link
-4	Interrupt Logic, PDP-4 Link
-5	Interrupt Logic, PDP-4 Link
-6	I/O Bus Output Buffer, Bits 0-7, PDP-4 Link
-7	I/O Bus Output Buffer, Bits 8-15, PDP-4 Link
-8	I/O Bus Input Buffer, Bits 0-7, PDP-4 Link
-9	I/O Bus Input Buffer, Bits 8-15, PDP-4 Link
53305	Block Diagram 810B PDP-4

Table 2. PDP-4 Intercomputer Link Interface drawings
ORNL I&C Division Drawing Series Q-2956

Number	Title
-30	Module Utilization
-31	Program Interrupts and Skip Bus Expansion
-32	Device Selector Extension
-33	Control and Input from SEL 810B
-35	Output to SEL, Bits 0 to 7
-36	Output to SEL, Bits 8 to 15
-37	PDP-4 Ground Isolators and Power Supply, Metalphoto Panels
-38	PDP-4 Ground Isolators, Drivers, and Receivers

Table 3. PDP-9 Intercomputer Link Interface drawings
ORNL I&C Division Drawing Series Q-5072

Number	Title
-1	Program Interrupt Skip and Data Transfer Control
-2	Data Channel Control
-3	Input and Output Gating
-4	Cabling and Device Selectors
-5	Ground Isolating Driver, 0 to -3 Input
-6	Etched Circuit for Q-5072-5
-9A	Ground Isolating Receiver, Dual Isolator 0 to -3 Output
-9C	Ground Isolating Receiver, Dual Isolator 0 to +3 Output
-10	Etched Circuit for Q-5072-9A & B
-11A	Ground Isolating Driver, 0 to +3 Input
-12	Etched Circuit for Q-5072-11A
-15	SEL 810B Ground Isolators, Master Receivers, and Drivers
-17	Module Utilization

Drawings -7, -8, -9B, -13, and -14 are schematics or etched circuit layouts for ground isolating circuits not used by the PDP-9.

The cabling between these units and a typical ground isolation circuit to and from the SEL 810B computer is shown on the SEL 810B ground isolation schematic, ORNL I&C Division Dwg. No. Q-5072-15.* The connector pin assignments are listed in Table 4. The drivers and receivers for the PDP-4 and PDP-9 are tied in parallel when both computers are connected; however, the usual method of operation is with a connection to the PDP-9 only.

The reader is assumed to have a knowledge of electronics, digital control logic, and machine language programming. However, references are provided to manuals which give details of operation for the PDP-4, the PDP-9, and the SEL 810B.

1.1 810B Input

Input to the 810B uses a Buffer Empty signal from the 810B to indicate to the PDP-9(4) that it is ready to receive a 16-bit word and a Data Here signal from the PDP-9(4). The Data Here signal is generated as a result of testing the status of the Buffer Empty signal. It is routed through the 810B link interface,³ to generate either a Data Transfer Request for control of block transfers⁴ to memory or a Buffer Ready signal for single word transfers⁵ to the accumulator or memory.

1.2 810B Output

Output from the SEL 810B⁶ uses a Buffer Full signal to indicate to the PDP-9(4) that a word is ready for transfer and a Data Accepted signal from the PDP-9(4) when the word has been transferred into the PDP-9(4). The Data Accepted signal also generates a Data Transfer Request or a Buffer Ready signal at the 810B.

* See Sect. 5, Engineering Drawings for a list of Q-drawings pertinent to the topics discussed in this volume. These drawings are available from the authors.

Table 4. Connector pin assignments for the SEL 810B/PDP-4/PDP-9
Intercomputer Link

Pin ^a	Function	Pin ^a	Function
101	0	501	0
102	1	502	1
103	2	503	2
104	3	504	3
105	4	505	4
106	5	506	5
107	6	507	6
108	7	508	7
109	System Tag Bit 2 (Multiplexer FWB2)	509	PDP-4 Busy
110	810B Busy	510	PDP-4/9 On-line
111	Tag Bit (Multiplexer FWB3)	511	Telephone pair
112	Bit 16 Input (Multiplexer SWB14)	512	PDP-9 Busy
113	Bit 17 Input (Multiplexer SWB15)	513	PDP EOR PI
301	8	701	8
302	9	702	9
303	10	703	10
304	11	704	11
305	12	705	12
306	13	706	13
307	14	707	14
308	15	708	15
309	SEL Output Interrupt	709	PDP Output PI
310	SEL End of Record Interrupt	710	PDP Input PI
311	SEL Input Interrupt	711	PDP Data Here
312	810B Buffer Empty	712	PDP Data Accepted
313	810B Buffer Full	713	Cable Shield

^aPins 201-213, 401-413, 601-613, and 701-713 are the ground side of a twisted pair, for example, 101/201.

1.3 Transfer Modes

Hardware restrictions will not permit simultaneous transfer of information through the PDP-4 and PDP-9 link interfaces; however, a separate busy line from both the PDP-4 and the PDP-9 is available for testing at the other computer. The PDP-4 interface is restricted to accumulator transfers via the information collector and information distributor of the PDP-4 Real Time option.⁷ The PDP-9 interface can be used for either accumulator or data channel (to or from memory in blocks) transfers.⁸

1.4 Multiplexer Input

An alternate method of connection has been provided for data input to the SEL 810B via the Four-Channel Priority Multiplexer⁹ from the link interfaces of the PDP-4 or PDP-9. The PDP-4 and PDP-9 link interfaces can be connected into separate multiplexer channels for simultaneous input of 18 bits of data. The link interfaces use the not-true condition of the multiplexer Channel Busy signal as Buffer Empty, and the Data Here signal from the link interface is used as a Data Ready signal at the multiplexer. The multiplexer logic returns the Data Here pulse as a Channel Busy level.

The connector pin assignments for the 37-pair multiplexer cable are given in Table 5. Table 6 lists the interconnections between the 102-pin link interface connector and the 75-pin multiplexer connector. Typical ground isolation wiring to and from the multiplexer is shown in Figs. 1a and 1b.

2. SEL 810B INTERCOMPUTER LINK INTERFACE

The SEL 810B Intercomputer Link Interface is logically divided into six functional parts: I/O synchronization, status testing, block transfer control, priority interrupt, output buffering, and input buffering. The first four parts are given general detailed explanations in ref. 4,

Table 5. Connector pin assignments for the SEL 810B
Four-Channel Priority Multiplexer

Pin+	Pin-	Function	Pin+	Pin-	Function
101	201	MPXR Control	408		Channel 2 Indicator
102	202	MPXR Interrupt	308		Channel 3 Indicator
103	203	System Tag, Bit 2	309	409	Second Word, Bit 0
104 ^a	204	First Word, Bit 3	310	410	Second Word, Bit 1
105 ^a	205	First Word, Bit 4	311	411	Second Word, Bit 2
106 ^a	206	First Word, Bit 5	312	412	Second Word, Bit 3
107 ^a	207	First Word, Bit 6	313		Channel 1 Indicator
108	208	First Word, Bit 7	501	601	Second Word, Bit 4
109	209	First Word, Bit 8	502	602	Second Word, Bit 5
110	210	First Word, Bit 9	503	603	Second Word, Bit 6
111	211	First Word, Bit 10	504	604	Second Word, Bit 7
112	212	First Word, Bit 11	505	605	Second Word, Bit 8
113		Channel 0 Indicator	506	606	Second Word, Bit 9
301	401	First Word, Bit 12	507	607	Second Word, Bit 10
302	402	First Word, Bit 13	508	608	Second Word, Bit 11
303	403	First Word, Bit 14	509	609	Second Word, Bit 12
304	404	First Word, Bit 15	510	610	Second Word, Bit 13
305	405	Data Ready	511	611	Second Word, Bit 14
306	406	Data Accepted	512	612	Second Word, Bit 15
307	407	Channel Busy	513		Cable Shield

^aExperimenter tags (typical).

Table 6. P202/P108 pin assignments for the
PDP-4 or PDP-9 multiplexer cable

Connector			Contact	Part Number ^a		ORNL Stores Number		
P202			Pin	201330-1		06-867-2013		
P108			Pin	201330-1		06-867-2013		

Connector			Connector			Connector		
P202	P108	Color	P202	P108	Color	P202	P108	Color
Pin	Pin		Pin	Pin		Pin	Pin	
101		brown	301	<i>b</i>	brown	501	507	green
201		white	401		black	601	607	yellow
102		red	302	<i>b</i>	red	502	508	red
202		white	402		black	602	608	brown
103	109	orange	303	501	orange	503	701	orange
203	209	white	403	601	black	603	801	brown
104	111	yellow	304	502	yellow	504	702	yellow
204	211	white	404	602	black	604	802	brown
105	<i>b</i>	green	305	711	green	505	703	green
205		white	405	811	black	605	803	brown
106	<i>b</i>	blue	306		blue	506	704	blue
206		white	406		black	606	804	brown
107	<i>b</i>	violet	307	312	violet	507	705	violet
207		white	407	412	black	607	805	brown
108	<i>b</i>	gray	308		gray	508	706	gray
208		white	408		black	608	806	brown
109	<i>b</i>	black	309	503	blue	509 ^d	707	green
209		white	409	603	red	609 ^d	807	orange
110	<i>b</i>	orange	310	504	violet	510	708	blue
210		red	410	604	red	610	808	orange
111	<i>b</i>	yellow	311	505	gray	511	112	violet
211		red	411	605	red	611	212	orange
112	<i>b</i>	green	312	506	yellow	512 ^e	113	gray
212		red	412	606	orange	612 ^e	213	orange
113	<i>c</i>	blue	313	<i>c</i>	yellow	513		shield

^aAMP Inc., Harrisburg, Pennsylvania.

^bSolder and insulate pair at P108, 104 pins.

^c113 and 313 are a twisted pair.

^dFor PDP-9: jumper 509 to 813 and 609 to 713 in P108. See Dwg. No. Q-5072-1.

^eFor PDP-4: jumper 512 to 813 and 612 to 713 in P108. See Dwg. No. Q-2956-38.

Fig. 1. FDP Intercomputer Link ground isolation for signals (a) to and (b) from the multiplexer.

Sect. 3 and Sect. 4. A detailed explanation of the latter three parts can be found in ref. 3, with an acronym list on pp. 3-37. A theory of operation using the simplified logic diagram of Fig. 2 for priority interrupts, output buffering, and input buffering follows here in Sects. 2.2, 2.3, and 2.4 respectively. A list of detailed logic drawings is given above in Table 1.

2.1 SEL 810B Intercomputer Link Programming

The bit definitions for the CEU and TEU second words¹⁰ as used by the link interface are given in Table 7. A Master Clear signal from the SEL 810B sets the Buffer Empty flip-flop and resets the Buffer Full flip-flop. There is no way in the hardware to separate the data from and to PDP-4 and PDP-9 computers.

2.1.1 Programming Notes

1) The link tests BUSY if the PEC Block Transfer Control (BTC) has been initialized, or if the PDP-4 is enabled. The PDP-9 cannot be tested for busy.

2) The interrupts are designated by their engineering labels. Two interrupts, Input and End of Record, are available but not used by the ORELA Data Acquisition Monitor System.¹¹ The End of Record (EOR) interrupt is hardware-generated.

3) An On-Off Line switch on the 4/9 link can be used to turn off the incoming interrupts to the PEC. The normal mode is ON-LINE.

2.1.2 Programming Cautions

1) The link will always accept a CEU instruction. The second CEU will override a transfer that has been started but not completed by the first CEU.

Fig. 2. Simplified logic of the Intercomputer Link Interface at the SEL 810B for the SEL 810B/PDP-4/PDP-9 Intercomputer Link.

Table 7. SEL 810B/PDP-4/PDP-9 Intercomputer Link,
CEU and TEU second-word formats

Bit	CEU Second Word	Bit	TEU Second Word
0	Initialize BTC	0 ^b	
1 ^a		1	
2		2	Skip if link is not busy
3	Input Interrupt	3	Skip if link is on-line
4	1/0 Input/Output	4	
5	Output Interrupt	5	
6		6	
7		7	
8		8	
9		9	
10		10	
11		11	
12		12	
13	Transfer CWA	13	
14		14	
15		15	

^aBits 1, 2, 6-12, 14, and 15 are not used in the CEU Second Word.

^bBits 0, 1, and 4-15 are not used in the TEU Second Word.

2.2 SEL 810B Priority Interrupts

2.2.1 To the PDP-9 or PDP-4

There are three interrupts in each direction in the intercomputer link. Two of the interrupts from the SEL 810B, Input and Output, are generated by executing a CEU instruction when either bit 3 or 5 is set in the CEU second word. The third interrupt, EOR is automatically generated by the End of Block signal when the BTC completes a transfer.

A text program 8CHK (see Sect. 2.6.1), generates Input, EOR, and Output interrupts with a 5-kHz repetition rate separated by approximately 4 μ sec.

2.2.2 From the PDP-9 or PDP-4

The interrupt pulses generated as a result of an Input/Output Transfer (IOT) instruction in the PDP-4 or PDP-9 are stretched in the interface under control of the 810B I/O Bus Clock (TPULSE) to a minimum width of 2.25 μ sec and a maximum width of 3 μ sec.

Two test programs are available in the PDP-4 to generate the interrupts: CHECK4 and SELPDP (see Sect. 3.6). A subroutine of the LNKCHK program operating in the PDP-9 (see Sect. 4.6) can generate the interrupts and other control pulses in sequence, or they can be generated by switch register control in the main LNKCHK program.

2.3 SEL 810B Output Buffering

The output buffering of the 810B end of the interface is controlled when operating under BTC or accumulator control by the signals Data Transfer Request (Buffer Ready) to the computer and BTC Data Accepted (Register Strobe) from the computer. The BTC Data Accepted signal strobes the data from the 810B I/O Bus into the Output Buffer flip-flops and sets the Buffer Full flip-flop signal to the PDP-9. Recognition of the Buffer Full signal by the PDP-9 results in strobing of the data into the PDP-9 and generation of a Data Accepted pulse through an IOT instruction. When the Data Accepted signal is received at the 810B, it resets the Buffer Full flip-flop and generates a Data Transfer Request to the 810B. A memory access cycle is then granted to the interface via the Block Priority Control (BPC) and BTC7 in approximately 3 μ sec, resulting in the transfer of another word into the link interface. (If the Buffer Ready signal is present during an output instruction, AOP or MOP, a word is transferred to the link; otherwise, the instruction will loop until the Buffer Ready signal occurs.) The last word transferred via the BTC generates an End of Record interrupt at the PDP-9 when the End of Block (EOB) signal from the BTC occurs.

The 8CHK test program (see Sect. 2.6.1) allows transmission of either the control switch pattern or an alternating pattern of ones and zeros via the accumulator. 8PDP (Sect. 2.6.2) and 8LNK (Sect. 2.6.3)

are more elaborate programs that operate via the BTC, with automatic checking of data sent and received.

2.4 SEL 810B Input Buffering

The input buffering of the 810B end of the interface is controlled when operating under BTC or accumulator control by the signal Data Transfer Request (Buffer Ready) to the computer and BTC Gate Data In (Gate Data In) from the computer. The normal condition for the Buffer Empty flip-flop is empty. The Buffer Empty condition at the PDP-9 results in gating data to the input lines and generation of the Data Here signal. The Data Here signal at the 810B interface strobes the input data into a buffer register, removes the Buffer Empty condition, and generates a Data Transfer Request. In response to the Data Transfer Request, a memory access cycle is granted to BTC7 via the BPC. The resultant signal, BTC Gate Data In, then gates the data from the input buffer into the 810B. (The data is strobed into the accumulator or memory when the Buffer Ready signal is present during an AIP or MIP instruction; otherwise, the instruction will loop until the Buffer Ready occurs.) The BTC Gate Data In signal sets the Buffer Empty flip-flop and the cycle repeats. The last word transferred into the computer via the BTC also generates an End of Record interrupt at the PDP-4 when the EOB signal from the BTC occurs.

The 8CHK test program (see Sect. 2.6.1) allows reception and display of the data sent from the PDP-4 or PDP-9. 8PDP (Sect. 2.6.2) and 8LNK (Sect. 2.6.3) are more elaborate programs that operate via the BTC, with automatic checking of data received and transmitted.

2.5 SEL 810B Ground Isolation

The ground isolation between the SEL 810B, shown in Dwg. No. Q-5072-15, is provided by Iso-switch Model 1513 isolated digital line driver/receivers. The ground isolation drivers (Dwg. No. Q-5072-5) and receivers (Dwg. No. Q-5072-9A)² at the SEL 810B are contained in a four-wide Nuclear Instrument Module (NIM).

The cabling between the SEL 810B, the PDP-4, and the PDP-9, and typical wiring for the ground isolation to and from the intercomputer link are shown on Dwg. No. Q-5072-15. Note that logic ground A is connected to the SEL 810B computer ground, while logic grounds B and C are connected to the PDP-9 and the PDP-4 computer ground respectively. The cable ground on the OUT- and IN- lines is isolated from the computer ground and tied to the chassis.

2.6 SEL 810B Intercomputer Link Test Programs*

There are three programs for testing the link: 8CHK, 8PDP, and 8LNK. Another program, 8MPX, is used for multiplexer input testing from the PDP-4 or PDP-9.

2.6.1 8CHK

8CHK is the most elementary test program and the simplest to use. There are four subsections to this program: ITRN — for interrupt generation, TRNS — to transmit the contents of the control switches, TRNA — to transmit alternate words of ones and zeros, and RCVA — to receive and display data in the A and B registers of the SEL 810B.

TRNS and TRNA require operation of the REC subsection in either the CHECK4 or LNKCHK program for the PDP-4 or the PDP-9 respectively. RCVA is used with the TRANSS and TRANSA subsections in either the CHECK4 or LNKCHK program.

2.6.2 8PDP

8PDP uses the control switches, also called sense switches, on the SEL 810B operator's console to generate interrupts, to send and receive fixed-length blocks of known data via the accumulator, to send and receive fixed-length blocks of known data via the Block Transfer Control (BTC), to compare the data received with the known data, to print the

* Test program listings are available from the authors.

data in error on comparison, and to print monitor characters. The control switches are executed in numerical order. See a program listing for the function of the sense switches. 8PDP is used with either SELPDP (at the PDP-4) or LNKCHK (at the PDP-9).

2.6.3 8LNK

8LNK is a test program to be used with LNKCHK on the PDP-9 or with SELPDP on the PDP-4. It sends a fixed block of known data, receives a fixed block of known data, checks the block of data received against the known data that was sent, and keeps a count of errors for any interrupt on BTC complete, Input, Output, or End of Record that is received out of the programmed sequence. Printing of the monitor teletype characters and comparison printout can be suppressed. See a program listing for the control switch settings.

3. PDP-4 INTERCOMPUTER LINK INTERFACE

The PDP-4 Intercomputer Link Interface is logically divided into six parts: I/O Skip Facility and Program Interrupt Request (Dwg. No. Q-2956-31), Device Selector extension (Dwg. No. Q-2956-32), incoming program interrupts (Dwg. No. Q-2956-33), outgoing priority interrupts (Dwg. No. Q-2959-33), output data control (Dwg. No. Q-2956-33, -35, and -36), and input data control (Dwg. No. Q-2956-33). A drawing list is given above in Table 2.

The unit is constructed in part of a DEC Type 1943 Mounting Panel using R Series Logic Modules¹²; in spare slots of the computer mainframe DEC System Modules¹³ are used for the Skip and the Program Interrupt facilities. All signals between the SEL 810B and the PDP-4 are routed through ground isolators (Dwg. No. Q-2956-38, see Sect. 3.5) at the PDP-4 through a 51-pair cable (see Table 4) to ground isolators at the SEL 810B (see Sect. 2.5).

The interface electrical characteristics of the PDP-4 are contained in ref. 7, pp. 52-56. The citations in Sects. 3.2, 3.3, 3.4, 3.5, and

3.7 refer to drawings in Drawing Series Q-2956 by drawing number and location as referenced by coordinates on the drawing edges. For example, [31D7] indicates drawing series Q-2956, drawing 31, location D7.

3.1 PDP-4 Intercomputer Link Programming

The IOT Pulse Assignments for the PDP-4 Intercomputer Link Interface are listed in Table 8. Each of the interrupts, Inputs, Output, and End of Record, has three instructions associated with it; a skip if flag is set (LISF, LOSF, LESF), a clear flag flip-flop (LICF, LOCF, LECF) for the received interrupt, and a generate interrupt (LIPG, LOPG, LERG) for the transmitted interrupt.

Two instructions are used to enable (LNBL) and disable (LDIS) the link. The link must be enabled; otherwise, the incoming interrupts will not be allowed to set their respective flag flip-flops, the outgoing interrupts will not be transmitted to the 810B, data will not be placed on the output lines, and the control pulses to the 810B will not be generated. The Enable flip-flop is used by the 810B as a PDP-4 Busy and inhibits the PDP-9 Intercomputer Link Interface from becoming enabled.

One instruction (LBSF) is used to test for the BTC unit connected (Busy) signal in the 810B. Data can be transmitted and received at the 810B via the accumulator or one word can be transmitted to or from memory without connecting the BTC.

Two instructions are used to output data: LBES to test the condition of the SEL input buffer and LDHG to strobe the data from the accumulator into the SEL input buffer.

Three instructions are used to input data: LBFS to test the condition of the SEL output buffer, LLAC to transfer data to the accumulator, and LDAG to return a Data Accepted pulse to the 810B.

3.1.1 PDP-4 Intercomputer Link Programming Restrictions

When programming the PDP-4 for operation with the PDP-9 computer also connected, the following instruction sequence should be executed to connect to and control the link:

```

NBL  LNBL
      LIPG or LOPG as required
      Delay loop to allow 810B setup
      LBSF
      JMP NBL.

```

The above sequence of instructions does not prevent the simultaneous connection of the PDP-4 and PDP-9 when the link enable instructions are executed simultaneously in both computers. The delay loop should be less than a millisecond and will probably require modification as a result of operating experience. The activity in the 810B and the level of the 810B priority interrupt are the determining factors for the delay.

Table 8. PDP-4 IOT assignments for the SEL 810B/PDP-4 Intercomputer Link Interface

<u>Mnemonic</u>	<u>Instruction</u>	<u>Function</u>
LISF	705001	Skip if SEL Input (to PDP-4) flag is set
LICF	705002	Clear SEL Input flag
LIPG	705004	Generate PDP Input interrupt
LOSF	705101	Skip if SEL Output (from PDP-4) flag is set
LOCF	705102	Clear SEL Output flag
LOPG	705104	Generate PDP Output interrupt
LESF	705201	Skip if SEL End of Record flag is set
LECF	705202	Clear SEL End of Record flag
LDIS	705204	Disable 810B/PDP-4 link
LBES	705301	Skip if SEL buffer is empty
LDHG	705302	Generate PDP Data Here (data is in AC)
LNBL	705304	Enable 810B/PDP-4 link
LBFS	705401	Skip if SEL buffer is full
LLAC	705402	Clear AC and gate data to AC
LDAG	705404	Generate PDP Data Accepted
LBSF	705501	Skip if the link Busy flag is set
LERG	705502	Generate PDP End of Record interrupt
	705504	Not used

3.2 PDP-4 Program Interrupts

There are three incoming interrupts and three outgoing interrupts in the PDP-4 Intercomputer Link Interface: Input, Output, and End of Record in each direction. The link must be enabled before interrupts can be received or transmitted.

3.2.1 From the SEL 810B

If the Link Enable signal [33D6] is present at the input AND gate, each of the incoming interrupts sets an R203 flip-flop [33D7 & 8]. The output of the flip-flops is then routed to type 4129 capacitor-diode gates¹³ [31D7] connected to the I/O Skip Facility.⁷ An IOT1 pulse from the device selectors [32D7 & 8] is used to test for the presence of the interrupts. (See the SELPDP program for a typical skip test chain.) Each of the flip-flops can be cleared via collector gating¹² [33C7] through an IOT2 pulse from the device selector [32D7 & 8] associated with the interrupt.

The signal Begin [33D8] from the START switch on the PDP-4 clears the three interrupt flip-flops and the Link Enable flip-flop so that the executing program has control of the interface through the LNBL and LDIS instructions.

3.2.2 To the SEL 810B

The IOT pulses from the device selectors [32D6 & 8] are routed through two-input AND gates controlled by Link Enable, to generate the priority interrupts [33A & B7] to the SEL 810B.

3.3 PDP-4 Input Control

The 16 bits of the SEL 810B are input into the msb locations of the PDP-4 (bits 16 and 17 are not used).

The Buffer Full signal [33C8] from the SEL 108B (Sect. 2.3) is tested in the I/O Skip Facility [31C7] by a skip test (LBFS) instruction. If it tests full, clear and load accumulator signals are generated through the device selectors [32D6] which gate the data from the Bit Out to PDP-4/9 lines from the ground isolators into the Information Collector⁷ on the PDP-4, via inverters [33] in the link interface. The next instruction (LDAG) executed generates a Data Accepted pulse [33B7] to the 810B through the device selector [32D5]. Data Accepted at the SEL 810B link interface (Sect. 2.3) removes the Buffer Full condition. The SEL 810B link interface uses the absence of the Buffer Full signal to load another word into the SEL Output buffer, thereby repeating the cycle. See the test program CHECK4, REC subsection for the typical input instruction sequence. A timing diagram for the REC test of CHECK4 is shown in Fig. 3. The numbers are the time in microseconds from the 0 reference.

3.4 PDP-4 Output Control

The 16 msb of the accumulator are gated through the Information Distributor⁷ to one input of a two-input AND/NOR(R141) gate [34 and 35]. (Six other AND inputs to the R141 gate were included for future expansion.) The second input is controlled by Link Enable [33D6]. The gate outputs are connected to the SEL 810B Input Buffer on 16 data lines (Bit In from the PDP-4/9) via the ground isolators. The data is loaded into the accumulator after the condition of Buffer Empty [33D7] has been tested with an IOT skip test [31D7] from the device selectors [32D7]. A Data Here signal [33B7] is then generated by an IOT pulse [32D7]. Data Here at the SEL 810B interface (Sect. 2.4) removes Buffer Empty, strobes the data into the Input Buffer, and causes a transfer of data into the SEL 810B from the link interface. Eventually, Buffer Empty returns to allow another transfer cycle. See the test program CHECK4, TRANSS or TRANSA subsections for a typical output instruction sequence. A timing diagram for the TRANSA test is shown in Fig. 4.

Fig. 3. Timing of input, REC in CHECK4, and TRNA in 8CHK.

Fig. 4. Timing of output, TRANSA in CHECK4, and RCVA in 8CHK.

3.5 PDP-4 Ground Isolation

The ground isolation for the PDP-4 is contained in a four-wide NIM using ground isolator receiver cards (Dwg. No. Q-5072-9A) and driver cards² (Dwg. No. Q-5072-5). Typical wiring for the drivers and receivers on the intercomputer link is shown on the ground isolation schematic (Dwg. No. Q-5072-15) for the SEL 810B.

The schematic for the PDP-4 ground isolation is Dwg. No. Q-2956-38, which also shows the cabling between the PDP-4, the SEL 810B, and the PDP-9. Note that the cable pairs to and from the 810B at the center of the drawing are not connected to the PDP-4 ground.

3.6 PDP-4 Intercomputer Link Test Programs

Three test programs for the PDP-4 Intercomputer Link Interface have been written and used in the installation and debugging of the link interface. They are CHECK4, SELPDP, and TEST4.

3.6.1 CHECK4

CHECK4 is a simple test routine that (1) generates the priority interrupts and the data control signals in subsection OUT, (2) transmits the PDP-4 control switches as selected by the operator in subsection TRANSS (received by REC subsection in 8CHK, see Sect. 2.6.1), (3) transmits alternate ones and zeros in subsection TRANSA (received by REC subsection in 8CHK), and (4) receives the data sent by 8CHK in the REC subsection.

3.6.2 SELPDP

SELPDP uses the control switches on the PDP-4 operator's console to generate interrupts, receive or send data, or both. A character E, I, or O is printed when the End of Record, Input, or Output interrupt is received. The switch assignments are executed in numerical order. See a program listing for the function of the control switches.

The data buffer must be sent from the 810B to the PDP-4 or manually loaded at location '1000 before the PDP-4 can send data to the SEL 810B program 8PDP (see Sect. 2.6.2), because the 8PDP program checks the received data against a stored data file. The data is not contained in SELPDP.

3.6.3 TEST4

TEST4 is a program that transmits either of two stored patterns of data through the SEL 810B Multiplexer to the 810B program 8MPX. One set of received data is checked by the 8MPX program. The BUFFER location in the TEST4 program is manually changed to '1100 for the alternating ones and zeros test, which cannot be checked by 8MPX (SNS 8 is set). See Fig. 5 for test program timing. Note that the 1.54 msec between LDHG 1 and LDHG 2 is the time consumed by data checking in the 810B.

3.7 PDP-4 Multiplexer Connection

The connection between the PDP-4 Intercomputer Link Interface and the Four-Channel Priority Multiplexer⁹ on the SEL 810B is made via a special cable to the multiplexer (Table 6) consisting of a 102-pin connector (P108) at the PDP-4 ground isolation module and a 75-pin connector (P202) at the multiplexer. Connector P202 has the standard multiplexer connections, as listed in Table 5. Note that the jumper connections in P108 are different for the PDP-4 [38D2] and the PDP-9 [Q-5072-1D4]. The link signals are received or transmitted in the multiplexer ground isolation module (Dwg. No. Q-5036-25) by a receiver (Dwg. No. Q-5072-9C) or a driver (Dwg. No. Q-5072-11A) respectively. See Fig. 1.

A timing diagram for the PDP-4 multiplexer connection is given in Fig. 6. Note that the PDP-4 output to the multiplexer is not in time sequence with respect to the actual collection of data. The instruction sequence for data acquisition is not the same as in the TEST4 program (see Sect. 3.6.3).

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NOTE:-

JUMPER PDP-4 BUSY (B8P) TO SYSTEM TAG 2 (B12D) DRAWING Q-2956-38 FOR THIS TEST

Fig. 5. TEST4-8MPX timing diagram.

ORNL-DWG 76-15930

Fig. 6. PDP-4 timing to SEL 810B Four-Channel Priority Multiplexer for data acquisition.

4. PDP-9 INTERCOMPUTER LINK INTERFACE

The PDP-9 Intercomputer Link Interface (Drawing Series Q-5072) is logically divided into eight parts: Skip Request [1D4]*, Program Interrupt Request [1C3], Device Selectors [Dwg. No. Q-5072-4], incoming program interrupts [1D6, 7 & 8], outgoing priority interrupts [1A/B6], output data control [3/1A6], input data control [3/1A6], and data channel control [Dwg. No. Q-5072-2]. The unit is constructed in two DEC Type 1943 Mounting Panels, using R Series Logic Modules.¹² The drawings are listed above in Table 3. All signals are routed through ground isolators (see Sects. 2.5 and 4.5) on twisted pairs in a 51-pair cable (see Table 4).

The interface electrical characteristics of the PDP-9 are contained in ref. 8. In particular, see the Program Controlled Transfer Timing of Figs. 3-5, pp. 3-7, and Data Channel IO Timing of Figs. 3-15, pp. 3-23.

4.1 PDP-9 Intercomputer Link Programming

The IOT pulse assignments for the PDP-9 are listed in Table 9. One instruction (LBSF) is used to test for the PDP-4 Busy signal (Enable).

The next two instructions are used to enable (LNBL) and disable (LDIS) the PDP-9 link interface. The PDP-9 link must be enabled; otherwise, the incoming interrupts will not be allowed to set their respective flag flip-flops, the outgoing interrupts will not be transmitted to the SEL 810B, data will not be placed on the output lines, and the control pulses to the 810B will not be generated. The Enable flip-flop also inhibits the PDP-4 Intercomputer Link Interface from becoming enabled.

Each of the interrupts, Input, Output, and End of Record, has three instructions associated with it: a skip if flag flip-flop is set (LISF, LOSF, LESF), and a clear flag flip-flop (LICF, LOCF, LECF) for the

* Refers to Drawing Series Q-5072, Dwg. No. 1, location D4 as referenced by coordinates on the drawing edges.

Table 9. PDP-9 IOT assignments for the SEL/PDP-9
Intercomputer Link Interface

<u>Mnemonic</u>	<u>Instruction</u>	<u>Function</u>
LBSF	705661	Skip if the PDP-4 is not busy
LNBL	705664	Enable the SEL/PDP-9 link
LDIS	705642	Disable SEL/PDP-9 link
LISF	705601	Skip if the SEL Input (to PDP-9) flag is set
LICF	705604	Clear the SEL Input flag
LIPG	705602	Generate the PDP Input interrupt (from PDP-9)
LOSF	705621	Skip if the SEL Output (from PDP-9) flag is set
LOCF	705624	Clear the SEL Output flag
LOPG	705622	Generate the PDP Output interrupt (to PDP-9)
LESF	705641	Skip if the SEL End of Record flag is set
LECF	705644	Clear the SEL End of Record flag
LERG	705662	Generate the PDP End of Record interrupt
LBES	705701	Skip if the SEL input buffer is empty
LDHG	705704	Generate PDP Data Here for accumulator output to SEL
LBFS	705721	Skip if the SEL output buffer is full
LDAG	705712	Clear accumulator, take input from SEL, and generate PDP Data Accepted
LSMR ^a	705722	Set data channel mode for Read (input)
LSMW ^a	705742	Set data channel mode for Write (output)
LOFS	705741	Skip if the data channel has overflowed
LDSF	705761	Skip if the data channel is busy
LDCF	705762	Clear the data channel Busy and Overflow
LSTG	705744	Generate System Tag 2 pulse (also known as SB2)
	705764	Not used

^aAlso sets Channel Busy flip-flop.

received interrupt and a generate interrupt (LIPG, LOPG, LERG) for the transmitted interrupt. Only one interrupt in each direction is used by the systems program, 7LNK,¹¹ on the SEL 810B.

Two instructions are used to output data: LBES to test the condition of the SEL 810B input buffer and LDHG to strobe the data from the accumulator (or memory, if the data channel is active) into the PDP-9 output buffer, where it is then strobed a few microseconds later into the 810B input buffer. The hardware executes these instructions when the data channel is connected.

Two instructions are used to input data: LBFS to test the condition of the SEL 810B output buffer (Buffer Full from the 810B) and LDAG to clear the accumulators, to take input from the 810B output buffer lines, and to generate the PDP Data Accepted pulse.

Five instructions are associated with the data channel control: LSMR or LSMW sets the data channel Busy flip-flop and sets either the Read (input) or Write (output) mode flip-flop; LDSF tests the data channel for busy; LOFS tests the data channel for overflow; and LDCF clears both the data channel Overflow and Busy flip-flops.

One instruction, LSTG, generates a System Tag bit 2. It is used during multiplexer input. See Sect. 4.7.

4.1.1 PDP-9 Intercomputer Link Programming Restrictions

When programming the PDP-9 for operation with the PDP-4 connected, the following instruction sequence should be executed to connect to and control the link:

```

                LDIS
NBL  LBSF
                JMP      .-1
                LNBL
                LBSF
                JMP      NBL-1
                LIPG or LOPG as required
                Delay loop to allow 810B setup.
```

The above sequence of instructions does not prevent the simultaneous connection of the PDP-4 and the PDP-9 when the link enable instructions

are executed simultaneously in both computers; however, it disables the PDP-9, allowing the PDP-4 to finish. The delay loop should be less than a millisecond and will probably require modification as a result of operating experience. The activity in the 810B and the level of the 810B priority interrupts are the determining factors for the delay.

See Sect. 4.7.1 for a programming caution applicable to the multiplexer connection.

4.2 PDP-9 Program Interrupts

There are three incoming interrupts and three outgoing interrupts in the PDP-9 Link Interface: Input, Output, and End of Record in each direction. The link must be enabled before interrupts can be received or transmitted.

4.2.1 From the SEL 810B

If the Link Enable signal [1D5] is present at the input AND gate, each of the incoming interrupts sets an R203 flip-flop [1D6/7]. The output of the flip-flops is then routed to R111 AND gates [1D4] connected to the Skip Request bus.⁸ An IOT1 pulse from the device selectors [4D5] is used to test for the presence of the interrupts at the AND gates [1D4] on the Skip Request bus. Each of the flip-flops [1C6] can be cleared by an IOT4 pulse [1C7] from the device selector [4D5].

The signal PWR CLR⁸ from the PDP-9 I/O bus clears the interrupt flip-flops and the Link Enable flip-flops so that the executing program has control of the interface through the LNBL and LDIS instructions.

4.2.2 To the SEL 810B

The IOT pulses from the device selectors [4D5] are routed through three input AND gates [1A5, 1B5] controlled by Link Enable, to generate the priority interrupts to the SEL 810B.

4.3 PDP-9 Input Control

The 16 bits from the SEL 810B are read into the 16 lsb bits 0 and 1 are not used) of the PDP-9. Data can be transferred to the accumulator or direct to memory (via the data channel) via the I/O bus of the PDP-9 [3C].

4.3.1 Input to the Accumulator

The Buffer Full [1B7] condition from the SEL 810B (Sect. 2.3) is tested by a skip instruction (LBFS) in an AND gate [1B4] connected to the Skip Request bus. If it tests full, a clear and load accumulator signal is generated by the device selector [4D5]. This signal (IOT 5712) opens the B163 AND gates [3C8] to gate the input data to the I/O Bus and hence to the accumulator. IOT 5712 also triggers a 3- μ sec delay [1A7], which is followed by a 1.7- μ sec-wide Data Accepted pulse. The Data Accepted pulse through the 810B Intercomputer Link Interface (Sect. 2.3) removes the Buffer Full signal. The absence of Buffer Full at the 810B causes a word to be transferred to the Link Output Buffer and the Buffer Full signal to return, thereby allowing repetition of the transfer cycle at the PDP-9. IOT 5712 also sets the RDRQ line [2D3] to the I/O Bus.

See the test program, LNKCHK, REC subsection for a simple input instruction sequence and LNKCHK, subsection RECV for receiving a buffer of fixed length via the accumulator.

4.3.2 Input via the Data Channel

When the Read Mode (LSMR) is selected, the data channel Busy flip-flop [2C3] and the mode flip-flop [2C3] are set. The Buffer Full signal (SBFL) from the 810B is routed through an AND gate [2C3] to set the data channel flag [2A6]. When the data channel request has been granted,⁸ an IOT 5702 is forced by the data channel control. The execution then follows the accumulator input control, with the exception that data is transferred into the PDP-9 memory. Upon return of the Buffer Full signal (SBFL), the data channel flag is set, thereby repeating the cycle.

See the test program LNKCHK, RECBUF subsection for an instruction sequence that receives a fixed length buffer via the data channel.

4.4 PDP-9 Output Control

Data can be transferred either from the accumulator or direct from memory using the data channel control via the I/O Bus of the PDP-9 [3C] to the output buffer [3B] of the link. The 16 lsb (bits 0 and 1 are not used) from the PDP-9 are transferred to the SEL 810B.

4.4.1 Output from the Accumulator

The first step of the program enables (LNBL) the link. This is followed by testing the Buffer Empty [1B7] signal in a skip gate [1B4] for the skip condition. The accumulator is then loaded with the data and an LDHG instruction is executed to generate IOT 5704. IOT 5704 generates the clear register [CLO REG, 1A8] signal on the leading edge of the IOT pulse and triggers a 0.7- μ sec delay. The trailing edge of this delay strobes [STO REG, 1A7] the data into the output register.

The trailing edge of the STO REG pulse triggers a 1- μ sec delay that allows the data lines to settle before the Data Here signal is sent to the SEL 810B. Data Here removes Buffer Empty and initiates a transfer into the 810B. The Buffer Empty signal returns at the completion of the transfer into the SEL 810B (see Sect. 2.4), which then allows the transfer cycle to repeat until terminated by the program.

See the test program LNKCHK, TRANSS or TRANSA subsection for a simple output instruction sequence and LNKCHK, subsection SEND for transmitting a buffer of fixed length via the accumulator.

4.4.2 Output via the Data Channel

Execution of LSMW sets the data channel Busy flip-flop [2C3] and sets the Mode flip-flop [2C3] to write. If the link has been enabled, the presence of Buffer Empty (SBMT) at a three-input AND gate [2C3] sets the data channel flag [2A6]. The data channel control⁸ forces an

IOT 5704, which then generates a CLO REG, a delay, a STO REG, a delay, and a Data Here pulse sequence to transfer the data from the PDP-9 memory to the SEL 810B Input Buffer. See Sect. 2.4 for 810B operation. The Buffer Empty signal is removed while the 810B transfers data. Its return then causes another transfer cycle, which continues until the data channel goes not-busy at IO OFLO [4D3] from the PDP-9 data channel control.

See the test program LNKCHK, SENBUF subsection for an instruction sequence that sends a fixed length buffer via the data channel.

4.5 PDP-9 Ground Isolation

The ground isolation of the PDP-9 is contained in row A (Dwg. No. Q-5072-17) using ground isolator receiver cards (Dwg. No. Q-5072-9A) and driver cards² (Dwg. No. Q-5072-5). Typical wiring for the drivers and receivers is shown on the ground isolation schematic, Dwg. No. Q-5072-15, for the SEL 810B. The ground isolators are shown on Dwg. Nos. Q-5072-1D6, -1B6, -1B2, -3D, and -3B. Note that the cable pairs to and from the 810B are not connected to the PDP-9 computer ground.

4.6 PDP-9 Intercomputer Link Test Programs

Two test programs for the PDP-9 Intercomputer Link Interface have been written and used in the installation and debugging of the link interface. They are LNKCHK and MULTCHK. These two programs are available from the authors. LNKCHK also contains a set of simple test routines similar to those in CHECK4.

4.6.1 LNKCHK

LNKCHK consists of a collection of test routines for the PDP-9 similar to those for the PDP-4. The simple test routines are: (1) OUT — which generates the priority interrupts and the data control signals, (2) TRANSS — which transmits the PDP-9 control switches as

selected by the operator (received by REC in 8CHK, Sect. 2.6.1), (3) TRANSA — which transmits alternate ones and zeros (received by REC in 8CHK, Sect. 2.6.1), and (4) REC — which receives data sent by 8CHK (Sect. 2.6.1).

The second section of LNKCHK uses the control switches on the PDP-9 to generate interrupts, receive or send data, or both. Teletype characters are printed to monitor the operation as follows;

- I - received input interrupt
- Ø - received output interrupt
- E - received EOR interrupt
- T - teletype interrupt
- 7 - buffer sent
- 4 - buffer received (NOPed)
- § - PDP-4 not busy
- 8 - buffer full (NOPed)
- 6 - buffer empty (NOPed)
- C - data channel overflow
- K - 262,143 buffers received OK.

The switch assignments, executed in numerical order as selected, are the following:

- SW-0 - perform operations selected
- SW-1 - send input interrupt
- SW-2 - send output interrupt
- SW-3 - send EOR interrupt
- SW-4 - receive via accumulator
- SW-5 - send via accumulator
- SW-6 - receive via accumulator and check
- SW-7 - receive and send same buffer
- SW-8 - receive via data channel
- SW-9 - receive via data channel and check
- SW-10 - send via data channel
- SW-16 - repeat until SW-0 is lowered
- SW-17 - suppresses all typing.

The check routine on SW-6 and -9 prints the address of the first incorrect word, the incorrect word, the word counter, and the number of good buffers received since the last error.

4.6.2 MULTCK

MULTCK is a program that transmits either of two stored patterns of data through the SEL 810B Four-Channel Priority Multiplexer to the 810B program 8MPX. One set of received data is checked by the 8MPX program.

The BUFFER location in the MULTCK program is manually changed to '16077 for the alternating ones and zeros test pattern which cannot be checked by 8MPX (SNS 8 is set).

See Fig. 7 for test program timing. Note that the 1.7 msec between LDHG 1 and LDHG 2 is the time consumed by data checking in the 810B.

4.7 PDP-9 Multiplexer Connection

The connection between the PDP-9 Intercomputer Link Interface and the Four-Channel Priority Multiplexer on the SEL 810B is made via a special cable to the multiplexer (Table 6) consisting of a 102-pin connector (P108) at the PDP-9 and a 75-pin connector (P202) at the multiplexer. Connector P202 has the standard multiplexer connections, as listed in Table 5. Note that the jumper connections in P108 are different for the PDP-9 (Dwg. No. Q-5072-1D4) and the PDP-4 (Dwg. No. Q-2956-38D2). The link signals are received or transmitted in the multiplexer ground isolation module (Dwg. No. Q-5036-25) by a receiver (Dwg. No. Q-5072-9C) or a driver (Dwg. No. Q-5072-11A).

4.7.1 Programming Caution for the Multiplexer Connection

The timing from Data Here to LBES when the instruction sequence is LDHG/LBES/JMP.-1 is 1.5 μ sec when the one-shot multivibrator output on pin Cl6V is set for a 1- μ sec-wide pulse. The trailing edge of Data Here triggers the multiplexer Channel Busy, with a 1.5- μ sec delay in the return to the PDP-9. This timing is critical and should be checked if the potentiometer on one-shot Cl6V [1A7] is changed. A timing adjustment of approximately 4.8 μ sec will cause intermittent memory parity errors in the SEL 810B when the multiplexer input data is read.

NOTE:-

JUMPER PDP-9 BUSY (A27H) TO SYSTEM TAG 2 (A23D) DRAWING Q-5072-1

Fig. 7. MULTCK-8MPX timing diagram.

5. ENGINEERING DRAWINGS

The following Q-drawings are related to the topics discussed in this volume. They are not included here due to space limitations, but are available from the authors.

Q-2956 (see Table 2, PDP-4)

Q-5036-25 - SEL 810B Multiplexer Isolation, Ground Isolators,
Drivers, and Receivers

Q-5072 (see Table 3, PDP-9)

Q-5187 (see Table 1, SEL 810B)

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