ORELA Data Acquisition System Hardware

Vol. 7: Instruction Manual for the
Multiplexer Channel and Scaler Interface Tester
(Q-5130)

J. W. Reynolds

MASTER

OAK RIDGE NATIONAL LABORATORY

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INSTRUMENTATION AND CONTROLS DIVISION

ORELA DATA ACQUISITION SYSTEM HARDWARE

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for the
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ABSTRACT

This report describes the method of use, operating instructions, theory of operation, and assembly details of the Multiplexer-Scaler Tester.

1. INTRODUCTION

The data input hardware at ORELA, either a Device Controller¹ attached to a Scaler Interface^{2,3} or a multiplexer channel of the Four-Channel Priority Multiplexer (FCPM),^{3,4} can be tested with the ORELA Multiplexer-Scaler Tester, ORNL Instrumentation and Controls Division Drawing Series Q-5130, and its associated computer programs. Three test programs are available for use with the Multiplexer-Scaler Tester. The first program, 8MUP, using data file 8MXP, tests the multiplexer channels. The second program, 8TSC, using data file 8SCD, tests the scaler input. The third program, 7MPX, tests a multiplexer channel while data are being acquired from other experimenters. The operating instructions are contained in the program listing.

The tester generates any one of five test patterns plus a Data Ready control signal. The Data Ready control signal repeats at a switch-selectable fixed or pseudo-random rate. Four of the test patterns contain 32 double words that are used as First Word (FW) and Second Word (SW) in the multiplexer and Scaler Word 1 and 2 in the Scaler Interface. The fifth test pattern, called ALL, has 128 double words obtained by combining the four 32-double-word patterns in the order WALK0, 01/10, WALK1 and 1/0.

The tester is assembled in a four-wide Nuclear Instrument Module using the front and rear panels specified on ORNL I&C Division Dwg. No. Q-5130-3* with assembly per Dwg. No. Q-5036-29. It is connected either to the Scaler Interface, through a 51-pair I/O cable, or to a multiplexer channel, through a 37-pair cable routed through the SEL 810B Multiplexer Ground Isolator (see Dwg. No. Q-5036-25) on that channel. See Dwg. No. Q-2928-11 for the cable assembly.

Data is asynchronously transferred from the tester to the computer under the control of two signals: Data Ready to the computer and Data Accepted from the computer. Each Data Ready pulse sent to the computer sets a busy latch in the tester. The return of the Data Accepted pulse from the computer resets this busy latch, thereby allowing the tester to

* See Sect. 7, Engineering Drawings, for the Q-drawings cited in this volume.

cycle. Since the computer program knows what pattern to expect, it can produce diagnostic information when an incorrect pattern is received. Such a test program can be operated at a low data rate while the other multiplexer channels are being utilized for data acquisition.

2. SWITCHES

The layout of the front panel for the tester is given in Fig. 1. The operation assigned to the three rotary switches and four toggle switches is described below. (The S numbers given are those used on the schematic Dwg. No. Q-5130-1.)

2.1 Mode Switch

The MODE switch is a three-pole, two-position (MPXR-SCALER) toggle switch (S6) that sets the tester to either MPXR (multiplexer) or Scaler Mode. It routes the signal sources of MPXR Control, Data Accepted, and EXTERNAL Clock Period from either the multiplexer or scaler cable to the respective control circuits in the tester.

2.2 Data Accepted Switch

The DATA ACCEPTED routing switch is a single-pole, two-position (EXT-INT) toggle switch (S7) whose normal position is EXTERNAL. Either a program-generated Pulse 11 from the Scaler Interface hardware or a Data Accepted pulse from the FCPM hardware is used in the EXT position. The INTERNAL position, used in either multiplexer or tester trouble diagnosis, uses a pulse (INTDA in Fig. 2) at the end of an internal timing sequence to simulate the Data Accepted signal.

2.3 Clock Period Switch

The CLOCK PERIOD switch is a three-pole, three-position (FIXED-EXTERNAL-RANDOM) rotary switch (S3) that selects a pulse pair period.

Fig. 1. Front panel layout.

ORNL-DWG 76-15940

* NOT PRESENT ON EVERY COUNT

Fig. 2. Timing pulse chain.

The FIXED and RANDOM positions use a nominal frequency selected by the CLOCK FREQUENCY selector switch (see Sect. 2.7). The FIXED position selects a single internal oscillator output to be used to initiate a data transfer. The EXTERNAL position selects an outside source to set the rate of data transfer. In this switch position the Scaler Mode uses a program-generated Pulse 12 from the Scaler Interface as a signal source to initiate data input from the tester. The RANDOM position selects two internal oscillator outputs, nominally set at a CLOCK FREQUENCY, that are ORed together and used to initiate a data transfer. The period between a pair of pulses will vary as a multiple of the difference between the nominal frequencies; therefore, nearly all periods less than the nominal clock period will be present as time progresses.

2.4 System Tag Switch

The SYSTEM TAG switch is a single-pole, two-position (BLOCK-EVENT) toggle switch (S4) whose normal position is BLOCK. The EVENT position is used for trouble shooting in a multiplexer channel. A System Tag bit (FWB2) is generated for the multiplexer test patterns with the first event in a BLOCK of 32 double words (128 for ALL) or at each EVENT. The program must "know" the status of this switch.

The System Tag signal is not used in Scaler Mode.

2.5 Channel Busy Switch

The CHANNEL BUSY switch is a two-pole, two-position (ACTIVE-OFF) toggle switch (S5) whose normal position is ACTIVE. The OFF position is used for either multiplexer or tester trouble diagnosis. The ACTIVE position of the switch inhibits the initiation of another timing sequence until the computer has accepted the previous event. It does this by using the output of a latch set by Data Ready to the computer and reset by Data Accepted from the computer.

2.6 Reset Switch

The RESET switch is a single-pole, single-throw push-button switch (S8) that initializes the Block flip-flop, the Channel Busy latch, the ALT flip-flop, the state counter, and the output register when a test pattern is selected. The test programs have the responsibility for generating printed instructions for resetting and for synchronizing the incoming data with the program, since an arbitrary reset will generate a sequence error in the test pattern.

2.7 Clock Frequency Switch

The CLOCK FREQUENCY selector switch is a two-pole, five-position rotary switch (S1) that is used to select a nominal rate of data transfer when testing a multiplexer channel. The nominal rates are 100, 500, 1000, 2000, and 5000 transfers/sec. In Scaler Mode, the time base signal is generated by the computer program.

2.8 Test Pattern Switch

The TEST PATTERN selector switch is a five-pole, five-position rotary switch (S2) that is used to select one of the five available test patterns for generation. The corresponding pattern must be used by the test program. See 8MXD and 8SCD listings for the multiplexer and scaler test patterns respectively. Note that bits 0 and 1, FWB0 and FWB1, are fixed by the multiplexer hardware, and that bit 2 (FWB2) is controlled by the output signal, System Tag, in the multiplexer first word.

2.8.1 ALL

The ALL test pattern contains 128 double words made up (in sequence) of each of the four patterns described below.

2.8.2 WALK0

The WALKing 0 test pattern has 32 double words. The first word pair in MPXR Mode has all bits on, except for first word bits 0, 1, and 2; the Scaler Mode has all bits on except for bit 15 of the second word, SCW2B15. Each bit is then turned off, and all others are turned on, in sequence from left (bit 0) to right (bit 15) in the first and second words of an event. The last two events in MPXR Mode have all the bits on. See WLK0 in 8MXD and 8SCD.

2.8.3 01/10

The alternating 01/10 test pattern has 32 events. The first event has all the even bits on and the odd bits off in the MPXR Mode, and all the odd bits on and the even bits off in the Scaler Mode. The second event has the opposite pattern of bits. The test data then alternates between these two patterns. See ALTP in 8MXD and 8SCD.

2.8.4 WALK1

The WALKing 1 test pattern has 32 events. In MPXR Mode the pattern starts with all bits off; the Scaler Mode has all bits off except bit 15 of the second word. Each bit is then turned on, and all others are turned off, in sequence from left (bit 0) to right (bit 15) in each of the two words in an event. The last two events in MPXR Mode have all bits off. See WLK1 in 8MXD and 8SCD.

2.8.5 1/0

The alternating 1/0 test pattern has 32 events. The odd events have all bits on; the even events have all bits off. The first event has all bits on. See ALT1 in 8MXD or 8SCD.

3. INDICATORS

See the panel layout of Fig. 1.

3.1 Channel Number

The four channel lights indicate which multiplexer channel is in use by the tester.

3.2 ALT

The ALT indicator displays the status of the ALternate flip-flop, which is used to control the 01/10 and 1/0 test patterns.

3.3 Multiplexer Control

The MPXR CONTROL indicator displays the status of the multiplexer and the computer. The multiplexer is connected and the computer is running when the light is on.

3.4 Channel Busy

The CHANNEL BUSY indicator displays the status of the Channel Busy flip-flop in the multiplexer.

4. CONNECTORS

4.1 Scaler Interface

See Table 1 for the pin assignments. The tester uses the signals Pulse 11, Pulse 12, and all bits of Scaler Words 1 and 2.

Table 1. Connector pin assignments for the Scaler Interface (P3)
to and from the Scaler Ground Isolation (P301)

Pin	Ground	Function	Pin	Ground	Function
101	201	Scaler Word 1, Bit 0	501	601	Scaler Word 2, Bit 0
102	202	Scaler Word 1, Bit 1	502	602	Scaler Word 2, Bit 1
103	203	Scaler Word 1, Bit 2	503	603	Scaler Word 2, Bit 2
104	204	Scaler Word 1, Bit 3	504	604	Scaler Word 2, Bit 3
105	205	Scaler Word 1, Bit 4	505	605	Scaler Word 2, Bit 4
106	206	Scaler Word 1, Bit 5	506	606	Scaler Word 2, Bit 5
107	207	Scaler Word 1, Bit 6	507	607	Scaler Word 2, Bit 6
108	208	Scaler Word 1, Bit 7	508	608	Scaler Word 2, Bit 7
109	209	Scaler Word 1, Bit 8	509	609	Scaler Word 2, Bit 8
110	210	Scaler Word 1, Bit 9	510	610	Scaler Word 2, Bit 9
111	211	Scaler Word 1, Bit 10	511	611	Scaler Word 2, Bit 10
112	212	Scaler Word 1, Bit 11	512	612	Scaler Word 2, Bit 11
113	213	Scaler Word 1, Bit 12	513	613	Scaler Word 2, Bit 12
301	401	Scaler Word 1, Bit 13	701	801	Scaler Pulse 1
302	402	Scaler Word 1, Bit 14	702	802	Scaler Pulse 2
303	403	Scaler Word 1, Bit 15	703	803	Scaler Pulse 3
304	404	Group 0	704	804	Scaler Pulse 4
305	405	Group 1	705	805	Scaler Pulse 5
306	406	Group 2	706	806	Scaler Pulse 6
307	407	Group 3	707	807	Scaler Pulse 7
308	408	Scaler Select 1	708	808	Scaler Pulse 8
309	409	Scaler Select 2	709	809	Scaler Pulse 9
310	410	Scaler Select 4	710	810	Scaler Pulse 10
311	411	Scaler Word 2, Bit 13	711	811	Scaler Pulse 11
312	412	Scaler Word 2, Bit 14	712	812	Scaler Pulse 12
313	413	Scaler Word 2, Bit 15	713	813	Cable Shield

4.2 Multiplexer

See Table 2 for the pin assignments. All signals are used except for MPXR Interrupt.

4.3 Coaxial Test Points

DATA READY, DATA ACCEPTED, BLOCK 0, BLOCK 1, BLOCK 2, and BLOCK 3 are available as trigger sources when diagnosing trouble.

5. TESTER USE

Set either MPXR or Scaler Mode, then set the remaining switches as shown in Table 3. Specific settings may be required by a test program.

The associated test programs, 8MUP and 8TSC, check the data provided by the tester for pickups and dropouts in each of the data bits. One of the multiplexer test programs, 7MPX, has been written to operate with ODAR.⁵ It types the correct data and the error data.

For MPXR Mode, an intermittent error in a Stacking Buffer Memory,⁶ in the ground isolation,⁷ or in a channel of the multiplexer may be isolated and then repaired by repeating test runs after moving the tester logically and physically closer to the multiplexer.

6. THEORY OF OPERATION

The test patterns are controlled by the Block flip-flop [C4],* the TEST PATTERN switch [B4 and B11], the state counter [B10], the counter gates BLOCK 0, 1, 2, and 3 [C10], the ALT flip-flop [E11], and

*Refers to Drawing Series Q-5130, Dwg. No. 1, location C4 as referenced by coordinates on the drawing edges.

Table 2. Multiplexer cable connections

Pin+	Pin-	Function	Pin+	Pin-	Function
101 ^a	201	MPXR Control	308		Channel 3 Indicator
102	202	MPXR Interrupt	408	408	Channel 2 Indicator
103	203	System Tag, Bit 2	309	409	Second Word, Bit 0
104 ^b	204	First Word, Bit 3	310	410	Second Word, Bit 1
105 ^b	205	First Word, Bit 4	311	411	Second Word, Bit 2
106 ^b	206	First Word, Bit 5	312	412	Second Word, Bit 3
107 ^b	207	First Word, Bit 6	313		Channel 1 Indicator
108	208	First Word, Bit 7	501	601	Second Word, Bit 4
109	209	First Word, Bit 8	502	602	Second Word, Bit 5
110	210	First Word, Bit 9	503	603	Second Word, Bit 6
111	211	First Word, Bit 10	504	604	Second Word, Bit 7
112	212	First Word, Bit 11	505	605	Second Word, Bit 8
113		Channel 0 Indicator	506	606	Second Word, Bit 9
301	401	First Word, Bit 12	507	607	Second Word, Bit 10
302	402	First Word, Bit 13	508	608	Second Word, Bit 11
303	403	First Word, Bit 14	509	609	Second Word, Bit 12
304	404	First Word, Bit 15	510	610	Second Word, Bit 13
305	405	Data Ready	511	611	Second Word, Bit 14
306 ^a	406	Data Accepted	512	612	Second Word, Bit 15
307	407	Channel Busy	513	(Shield)	Channel Indicator Gnd

^aOutput from the multiplexer.

^bThese inputs are used for experimenter tags.

Table 3. Switch settings for multiplexer and scaler mode

Switch	Scaler	Multiplexer
Clock Frequency	Not applicable	As desired
Test Pattern ^a	As desired	As desired
Clock Period	EXT	As desired ^b
System Tag	Not applicable	Block
Channel Busy	Active	Active
Data Accepted	EXT	EXT

^a Must be coordinated with a test program.

^b May be determined by test program.

associated gating [E]. The Block flip-flop, the TEST PATTERN switch, and the state counter control which of the four pattern gating signals (BLOCK 0, 1, 2, or 3) are present by generating a RESET signal [C5] for the four 32-event test patterns. The fifth test pattern, ALL, produces the BLOCK 0, 1, 2, and 3 signals in a repeating sequence. Either Load Enable or Shift Enable is generated for a BLOCK at the outputs [E9] of OR gate (A2V1) or AND gate (B5C1). Note that the Shift Load pulse [D8] removes the Shift Enable signal for the pulse duration to allow the initial WALK0 or WALK1 pattern to be set into the output shift register.

Two of the five signals [E9] that control the data to be loaded into the output shift register are the BLOCK 0 and 2 signals. The other three signals depend upon the state of the ALT flip-flop that is enabled during BLOCK 1 or 3 and toggled by the Data Accepted signal returned from the channel under test.

The timing pulses, shown in Fig. 2, are controlled by the signals RESET, MPXR Control, and the output (A2D1) of the Channel Busy latch [C6]. The first two signals control the starting of the internal oscillators by AND gate [B5] output (A6V2) routed through the CLOCK PERIOD switch [B1]. The latch output is routed through the ACTIVE position of the Channel Busy switch [C6] to control the oscillator outputs [B3] from OR gate output (A2J1) in AND gate [C3] whose output (A6K1) triggers the timing pulse chain [D2] and also toggles the state counter [B9].

In normal operation the timing pulse INTDA (Internal Data Accepted, see Fig. 2) is not used. The Reset pulse occurs at the end of each block of data for the WALK0, 01/10, WALK1, and 1/0 test patterns. A Reset is not generated for the ALL test pattern. The Shift Load pulse occurs at the beginning of the WALK0 and WALK1 test patterns to initialize the output shift register. See Fig. 3 for the automatic reset timing. Note that the dotted signals are for the 01/10 or 1/0 test patterns unless noted otherwise.

7. ENGINEERING DRAWINGS

<u>Drawing No.</u>	<u>Page</u>
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Reference Drawings

(The following related drawings are not included here due to space limitations, but are available from the author.)

- Q-2928-11 — ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors
- Q-5036-25 — SEL 810B Multiplexer Isolation, Ground Isolators, Drivers, and Receivers
- Q-5036-29 — SEL 810B Multiplexer-Scaler Isolation, Assy., Four-Wide Nuclear Instrument Module
- Q-5130-3 — ORELA Data Acquisition, Front and Rear Panels

Fig. 3. Automatic reset timing.

ASSY. 4 WIDE NIM		Q-5036-29	
FRONT & REAR PANELS		Q-5130-3	
REFERENCE DRAWINGS			
DESIGN	DATE	REVISION CHECK	DATE
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