MASTER

ORELA Data Acquisition System Hardware

Vol. 4: ORELA Device Controllers
(Q-5098)

J. W. Reynolds
R. E. Wintenberg

OAK RIDGE NATIONAL LABORATORY

OPERATED BY UNION CARBIDE CORPORATION FOR THE ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

Printed in the United States of America. Available from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road, Springfield, Virginia 22161
Price: Printed Copy \$4.50; Microfiche \$3.00

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the Energy Research and Development Administration/United States Nuclear Regulatory Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

Contract No. W-7405-eng-26

INSTRUMENTATION AND CONTROLS DIVISION

ORELA DATA ACQUISITION SYSTEM HARDWARE

Vol. 4: ORELA Device Controllers
(Q-5098)

J. W. Reynolds and R. E. Wintenberg

Date Published: January 1977

NOTICE
This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Energy Research and Development Administration, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

NOTICE This document contains information of a preliminary nature. It is subject to revision or correction and therefore does not represent a final report.

OAK RIDGE NATIONAL LABORATORY
Oak Ridge, Tennessee 37830
operated by
UNION CARBIDE CORPORATION
for the
ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION

Other volumes in this series of reports on *ORELA Data Acquisition System Hardware* are:

ORNL/TM-5638	Introduction
ORNL/TM-5639 (Vol. 2 of ORNL/TM-5638)	Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)
ORNL/TM-5640 (Vol. 3 of ORNL/TM-5638)	Scaler Interfaces (Q-5036-1, -2, -4 through -11, -29, and -30)
ORNL/TM-5642 (Vol. 5 of ORNL/TM-5638)	SEL 810B/PDP-4/PDP-9 Intercomputer Link
ORNL/TM-5643 (Vol. 6 of ORNL/TM-5638)	Eight-Stage Stacking Buffer Memory (Q-5066)
ORNL/TM-5644 (Vol. 7 of ORNL/TM-5638)	Instruction Manual for the Multiplexer Channel and Scaler Interface Tester (Q-5130)
ORNL/TM-5645 (Vol. 8 of ORNL/TM-5638)	Instruction Manual for the Ground Isolation Driver and Receiver Cards on the Quiet Ground System at ORELA

CONTENTS

	<u>Page</u>
ABSTRACT	v
1. INTRODUCTION	1
1.1 Pulse Generation	1
1.2 Input Data Routing	2
1.3 Storing Control Words	2
1.4 System Monitoring	4
1.5 Special Control	4
2. PROGRAMMING	5
3. SCALER INTERFACE-DEVICE CONTROLLER SIGNALS	5
4. OPERATION	11
4.1 Address Decoding	11
4.2 Pulse Definition	11
4.2.1 PX001 Through PX012	11
4.2.2 PX101 Through PX112	12
4.2.3 PX201 Through PX212	15
4.3 Scaler Word Gating	15
4.3.1 Scaler Input Bus	17
4.3.2 Device Word Input	17
4.4 OPERATE Monitor	17
4.5 Control Registers	19
4.6 Special Control Circuits	20
5. ISOLATED PULSE GENERATOR	20
5.1 Operation	20
5.2 Assembly	20
6. MAINTENANCE	21
7. ENGINEERING DRAWINGS	23
APPENDIX A. JAH SPECIAL CONTROL	25
APPENDIX B. RLM SPECIAL CONTROL	33
APPENDIX C. GDS SPECIAL CONTROL	37

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

ABSTRACT

This report describes the programming, word formats, control signals, voltage levels, connector layouts, ground isolation, and a theory of operation with a simplified logic diagram for the ORELA Device Controllers. The ORELA Isolated Pulse Generators (Dwg. No. Q-5109) are also described..

1. INTRODUCTION

The address and pulse generation and read-in capability of the program-controlled input of the Scaler Interfaces^{1,2} are not ready to perform a monitoring task or a control function until they are organized into an operating system of hardware controlled by a computer program. The logic of the Device Controller performs this task for some experimenters at ORELA with the control grouped into five related functions: pulse generation, input data routing, storing of control words, monitoring of the data acquisition system operating conditions, and specific control applications for each experimenter. Address decoding is used by all these functions.

The reader is assumed to have a knowledge of electronics, digital control logic, and machine language programming,³ I/O in particular, for the SEL 810B computer. Further logic and electronic details can be obtained from ORNL Instrumentation and Controls Division Drawing Series Q-5098 as listed in Tables 1 and 2. The cabling and location of equipment at the central data area is shown on Dwg. Nos Q-2928-5* and Q-2928-2 respectively.

1.1 Pulse Generation

The first function, pulse generation, combines the 12 ground isolated pulses from the Scaler Interface with 8 internally decoded addresses to generate a maximum of 96 discrete pulses for use by each of four controllers. The ORELA Isolated Pulse Generator (Drawing Series Q-5109) is a two-wide Nuclear Instrument Module (NIM) that generates a maximum of 12 pulses for those experimenters, using other computers (a PDP-4, a PDP-9, and a HP-2114A) that do not need the capabilities of a Device Controller. The Pulse Generation logic is common to all controllers.

* See Sect. 7, Engineering Drawings, for a list of Q-drawings pertinent to the topics discussed in this volume. These drawings are available from the authors.

Table 1. ORELA Device Controller, common logic
ORNL Drawing Series Q-5098

Number	Title
-1	Select Decode and Pulses X001 thru X312
-2	Select Decode and Pulses X401 thru X712
-3	Data Input Channel 0 to 3, Word 1
-4	Data Input Channel 0 to 3, Word 2
-5	Data Input Channel 4 to 7, Word 1
-6	Data Input Channel 4 to 7, Word 2
-7	Block Diagram
-8	Special Circuit Card Diagrams
-9A	Back Panels and Side Plates
-9B	Front Panel Mounting Rails
-9C	Front Panels
-9D	Metalphoto Nameplates

1.2 Input Data Routing

The input data routing is accomplished with a nine-input gating matrix that routes data from 8 devices and a Scaler Input Bus to the 32 ground-isolated input lines. The Scaler or Device Mode is controlled by pulse selection of routing flip-flops. The routing flip-flops increase the input selection from 8 to 16 input units, 8 devices and 8 "scalars." The "scalars" contain gates that allow their outputs to be transferred onto the Scaler Input Bus. The input data routing is common to all controllers.

1.3 Storing Control Words

Two blocks of 12 pulses are stored in 24 control flip-flops with outputs that are matched to the input requirements of the controlled equipment. These flip-flops are on the drawings assigned to each experimenter.

Table 2a. ORELA Device Controller, experimenter logic

Drawing subset assignment
ORNL Drawing Series Q-5098

Number	Title
-X0	Control Registers
-X1	OPERATE, Scaler Control, Lamp Drivers, and Special Control
-X2	Switch Monitor Receivers
-X4	(to -X8, as required)
-X9	Module Utilization and Cabling Diagram

Table 2b. ORELA Device Controller, experimenter logic

Appendices and drawing subsets
ORNL Drawing Series Q-5098

Drawing Subset	Appendix	For
-10 to -19	A	JAH
-20 to -29	B	RLM
-30 to -39	C	GDS
-40 to -49	D	
-50 to -59	E	
-60 to -69	F	
-70 to -79	G	
-80 to -89	H	
-90 to -99	J	

1.4 System Monitoring

The fourth function, OPERATE, monitors a set of conditions and controls the starting and stopping of the experimenter's scalers. The usual conditions monitored are a check on the start pulses from the linear accelerator, the operating status of the Four-Channel Priority Multiplexer, the RUN condition of the computer, and the state (START or STOP) of the experimenter's computer program. Other inputs can be added. Start and Stop Scaler pulses are produced by the leading and trailing edges of the OPERATE signal. This logic is on the drawings assigned to each experimenter.

1.5 Special Control

The specific control applications and signal conditioning of the signals into and out of the Device Controllers required for each experimenter are contained in an assigned drawing subset (Table 2b). The typical set of drawings in Table 2 are listed in each appendix as Table 2A, 2B, and 2C.

One drawing has the two control registers and specific outputs. A second drawing has the OPERATE monitor, lamp drivers, scaler control lines, and special control circuits. A third drawing has the signal conditioning circuits, and a fourth drawing has a cabling diagram and module utilization layout. Other drawings are added as needed to a maximum of ten.

The control for each experimenter is completed with a specific control program (5GDS, 5JAH, 5RLM)^{*} that operates through an experimenter's dispatch package (7GDS, 7JAH, 7RLM, etc.) under the control of ODAR.⁴ The letters are the experimenter's initials.

^{*}Control and dispatch programs are available from each experimenter.

2. PROGRAMMING

An address is routed to the Device Controller through the Scaler Interface by execution of a CEU instruction with a FORMAT 0 second word while a pulse is generated with a FORMAT 1 second word. The CEU second-word formats are given in Fig. 1. Note that pulse selection is by a unitary code to allow simultaneous generation of all pulses or any combination of them. An address mode instruction will force a delay of 3 μ sec, whereas the pulse mode instructions will force a delay that is equivalent to the length of the pulse (a maximum of 2 μ sec as presently adjusted) before the Scaler Interface will execute another command.

An illustration of the sequence of instructions required to read 32 bits from a scaler through a Device Controller is given in Fig. 2. The program as listed will not run; it requires a value of X (0 to 3) in the GRPX location and the same value of X plus a value of Y (0 to 7) in the SUBY location. Reading 32 bits of data from a device requires only a change of the location MODE to '104200, which will then select the device mode in a Device Controller. The Scaler and Device Modes of the Device Controllers define an eight-input 32-bit parallel bus with gating internal to the equipment attached or in the Device Controller.

A test program, 8SCL, has been written to test the existing and future Device Controllers. Special control circuitry will probably require the addition of another entry into the program. (See Maintenance, Sect. 6.)

3. SCALER INTERFACE-DEVICE CONTROLLER SIGNALS

Pin assignments for the connections between a Device Controller and the Scaler Interface Ground Isolation are listed in Table 3. Connector parts are shown on Dwg. No. Q-5098-3. Figures 3a and 3b show a typical connection to and from the Scaler Interface. The cable distance (see Dwg. No. Q-2928-11 for assembly) ranges from 60 to 150 ft. The function of each of the signals in Table 3 is described below.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
"0"	Not Used										2	1	4	2	1
											Group		Scaler Select		

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
"1"				1	2	3	4	5	6	7	8	9	10	11	12

Pulse Number

Unitary Code

→ LOAD WORD 1 of Program Controlled Input

→ LOAD WORD 2 of Program Controlled Input

→ GATE INPUT for the Scaler Input Bus

Fig. 1. Scaler Interface, CEU second word formats.

ORNL-DWG 76-15916

TO READ 32 BITS FROM A SCALER

REL			
ORG	0		
SYST	NOP		
ME	NOP		
	CEU	'22	SELECT SUBADDRESS 0 ON
GRPX	DATA	'X0	CHANNEL X. WHERE X IS
	BRU	*-2	0, 1, 2, OR 3
	CEU	'22	GENERATE PULSE X002 TO
MODE	DATA	'102200	SET DEVICE CONTROLLER IN
	BRU	*-2	SCALER MODE
	CEU	'22	SELECT SCALER ADDRESS
SUBY	DATA	'XY	Y ON CHANNEL X
	BRU	*-2	
	CEU	'22	GENERATE LOAD WORD 1 PULSE
	DATA	'110000	
	BRU	*-2	
	AIP	'22	
	BRU	*-1	
	STA	SMSB	SCALER MOST SIGNIFICANT BITS
	CEU	'22	GENERATE LOAD WORD 2 PULSE
	DATA	'120000	
	BRU	*-2	
	AIP	'22	
	BRU	*-1	
	STA	SLSB	SCALER LEAST SIGNIFICANT BITS
*	BRU	ME	YOUR PROGRAM HERE
3MSB	ZZZ	**	DMSB WITH MODE = '104200
SLSB	ZZZ	**	DLSB WITH MODE = '104200
	END		

Fig. 2. Instruction Sequence to read 32 bits from
a scaler or a device.

Table 3. Pin assignments for the Scaler Ground Isolation
(P5, P6, P7, and P8) to and from the Device Controller (P409)

Pin	GND	Function	Pin	GND	Function
101	201	Scaler Word 1, Bit 0	501	601	Scaler Word 2, Bit 0
102	202	Scaler Word 1, Bit 1	502	602	Scaler Word 2, Bit 1
103	203	Scaler Word 1, Bit 2	503	603	Scaler Word 2, Bit 2
104	204	Scaler Word 1, Bit 3	504	604	Scaler Word 2, Bit 3
105	205	Scaler Word 1, Bit 4	505	605	Scaler Word 2, Bit 4
106	206	Scaler Word 1, Bit 5	506	606	Scaler Word 2, Bit 5
107	207	Scaler Word 1, Bit 6	507	607	Scaler Word 2, Bit 6
108	208	Scaler Word 1, Bit 7	508	608	Scaler Word 2, Bit 7
109	209	Scaler Word 1, Bit 8	509	609	Scaler Word 2, Bit 8
110	210	Scaler Word 1, Bit 9	510	610	Scaler Word 2, Bit 9
111	211	Scaler Word 1, Bit 10	511	611	Scaler Word 2, Bit 10
112	212	Scaler Word 1, Bit 11	512	612	Scaler Word 2, Bit 11
113	213	Scaler Word 1, Bit 12	513	613	Scaler Word 2, Bit 12
301	401	Scaler Word 1, Bit 13	701	801	Scaler Pulse 1
302	402	Scaler Word 1, Bit 14	702	802	Scaler Pulse 2
303	403	Scaler Word 1, Bit 15	703	803	Scaler Pulse 3
304	404 ^a	Group X	704	804	Scaler Pulse 4
305	405	Group X Interrupt	705	805	Scaler Pulse 5
306	406		706	806	Scaler Pulse 6
307	407		707	807	Scaler Pulse 7
308	408	Scaler Select 1	708	808	Scaler Pulse 8
309	409	Scaler Select 2	709	809	Scaler Pulse 9
310	410	Scaler Select 4	710	810	Scaler Pulse 10
311	411	Scaler Word 2, Bit 13	711	811	Scaler Pulse 11
312	412	Scaler Word 2, Bit 14	712	812	Scaler Pulse 12
313	413	Scaler Word 2, Bit 15	713	813	CABLE SHIELD

^aGroup 0, 1, 2, and 3 in connectors J5, J6, J7, and J8 respectively;
see Dwg. No. Q-5036-30C4.

Fig. 3. Double isolation for signals (a) from the Device Controller to the Scaler Interface, and (b) to the Device Controller from the Scaler Interface.

Scaler Words 1 and 2 are 16-bit parallel inputs to the Scaler Interface that are gated into buffer registers by a program-generated control signal, Load Word 1 and Load Word 2. Each word is transferred from the Scaler Interface buffer register into the computer by execution of either an AIP or MIP instruction. The data on the Scaler Word Bus is gated through the Device Controller by an address from the Scaler Interface.

Group X is the decoded output of the two most significant bits of an address in the Scaler Interface. The group selection is made by the cable connection. It does not define a priority of service by ODAR; however, ODAR requires that the group number be the same as the multiplexer channel number. Each of the four cables (J5, J6, J7, and J8) in the Data Collection Equipment (DCE) Cabinets has its own group signal (GROUP 0, 1, 2, and 3 respectively); hence, they define a subset of scaler addresses (00_8 through 07_8 , 10_8 through 17_8 , 20_8 through 27_8 , and 30_8 through 37_8) that can be used by an experimenter.

Scaler Select 1, 2, and 4 are three of four address selection signals available in the Device Controller that are selected by a control program with a CEU address mode instruction (Fig. 1). A group address is selected simultaneously with the Scaler Select bits. The three select bits are combined with the group line in each Device Controller to generate eight explicit subaddresses, 0 through 7, for use by an experimenter.

Scaler Pulses 1 through 12 are generated in the Scaler Interface by a control program operating in the SEL 810B. Any one of or all the pulses may be generated with a single command instruction. The Scaler Pulses are combined with the Scaler Select and Group levels to generate 96 discrete pulses in each Device Controller. Each of the twelve basic pulses has an adjustable width; however, the width of the pulses has been set at 1 or 2 μsec . The width of pulses 1, 2, and 5 must remain at 2, 2, and 1 μsec , respectively, to allow a gate devices or a gate scalers pulse command (see MODE, Fig. 2) from existing control programs (5GDS, 5JAH, and 5RLM)⁴ to operate three existing Device Controllers.

Group X Interrupt is a line for a priority interrupt that has been reserved for future use.

4. OPERATION

The operation of the Device Controller is presented through a brief description of the major sections of logic. However, the complexities of operation for any device are contained in the control programs that are resident in the SEL 810B computer.

4.1 Address Decoding

The address decoding for the Device Controller (Dwg. No. Q-5098-1) consists of eight four-input M617 AND gates that produce the signals SELX0 through SELX7 (Select group X subaddress 0 through 7). These signals are used in the pulse definition logic and in the Scaler and Device Input Bus gating.

4.2 Pulse Definition

The logic for pulse definition (Dwg. Nos. Q-5098-1 and -2) consists of eight M101 data bus modules (NAND gates) with an address such as SELX0 on a common gating line to produce a set of 12 pulses PX001 through PX012. Three sets of these pulses have been assigned a specific function in the Device Controller; the remaining five sets are assigned as dictated by an experimenter's requirements. PX301 through PX306 in the fourth group are routed to coaxial connectors in one Device Controller (Dwg. No. Q-5098-31).

4.2.1 PX001 through PX012

The first set of pulses are assigned basic control functions in the Device Controllers, as listed in Table 4a, and in the Isolated Pulsed Generators (Sect. 5), as listed in Table 4b.

Table 4a. Pulse Group 0 assignments for a Device Controller

Address	CEU 2nd Word	Pulse	Name	Function
X0	104000	PX001	GDEV	Set Gate Devices flip-flop
X0	102000	PX002	GSCLRBO	Set Gate Scaler Bus 0 flip-flop
X0	101000	PX003	Prog. Start	Set Program On flip-flop
X0	100400	PX004	Prog. Stop	Reset Program On flip-flop
X0	100200	PX005	Gate Clear	Reset GDEV and GSCLRBO flip-flops
X0	100100	PX006		Reset scalers
X0	100040	PX007		Reset register 1A, Bits 11 & 12
X0	100020	PX008		Reset register 2A, Bits 11 & 12
X0	100010	PX009		Reset register 1, Bits 1-5
X0	100004	PX010		Reset register 1, Bits 6-10
X0	100002	PX011		Reset register 2, Bits 1-5
X0	100001	PX012		Reset register 2, Bits 6-10

4.2.2 PX101 through PX112

The second set of pulses set the 12 flip-flops in Control Register 1, as listed in Table 5. The specific use for an experimenter is listed in Tables 5A, 5B, and 5C respectively, in Appendices A, B, and C. The detailed logic, including the connection from the output of Control Register 1 through any special drive logic to a device cable (Table 6), is on Dwg. Nos. Q-5098-10, -20, -30, etc.

Table 4b. Pulse Group 0 assignments for an Isolated Pulse Generator

Address	CEU 2nd word	Pulse	Name	Function
X0	104000	PX001		
X0	102000	PX002		
X0	101000	PX003	Prog. Start	Set Program On flip-flop
X0	100400	PX004	Prog. Stop	Reset Program On flip-flop
X0	100200	PX005	Prog. Clear	Generates a clear pulse
X0	100100	PX006		Reset scalers
X0	100040	PX007		
X0	100020	PX008		
X0	100010	PX009		
X0	100004	PX010		
X0	100002	PX011		
X0	100001	PX012		

Table 5. Pulse Group 1 assignments to set Control Register 1

Address	CEU 2nd word	Pulse	Function
X1	104000	PX101	Set register 1, Bit 1
X1	102000	PX102	Set register 1, Bit 2
X1	101000	PX103	Set register 1, Bit 3
X1	100400	PX104	Set register 1, Bit 4
X1	100200	PX105	Set register 1, Bit 5
X1	100100	PX106	Set register 1, Bit 6
X1	100040	PX107	Set register 1, Bit 7
X1	100020	PX108	Set register 1, Bit 8
X1	100010	PX109	Set register 1, Bit 9
X1	100004	PX110	Set register 1, Bit 10
X1	100002	PX111	Set register 1A, Bit 11
X1	100001	PX112	Set register 1A, Bit 12

Table 6. Device Input (J400 through J407) pin assignments

Pin	Function	Pin	Function
101	Device Word 1, Bit 0	301	Device Word 2, Bit 9
102	Device Word 1, Bit 1	302	Device Word 2, Bit 10
103	Device Word 1, Bit 2	303	Device Word 2, Bit 11
104	Device Word 1, Bit 3	304	Device Word 2, Bit 12
105	Device Word 1, Bit 4	305	Device Word 2, Bit 13
106	Device Word 1, Bit 5	306	Device Word 2, Bit 14
107	Device Word 1, Bit 7	307	Device Word 2, Bit 15
108	Device Word 1, Bit 7	308	
109	Device Word 1, Bit 8	309	
110	Device Word 1, Bit 9	310	
111	Device Word 1, Bit 10	311	
112	Device Word 1, Bit 11	312	
113	Device Word 1, Bit 12	313	
201	Device Word 1, Bit 13	401	1
202	Device Word 1, Bit 14	402	2
203	Device Word 1, Bit 15	403	3
204	Device Word 2, Bit 0	404	4
205	Device Word 2, Bit 1	405	5
206	Device Word 2, Bit 2	406	6
207	Device Word 2, Bit 3	407	7
208	Device Word 2, Bit 4	408	8
209	Device Word 2, Bit 5	409	9
210	Device Word 2, Bit 6	410	10
211	Device Word 2, Bit 7	411	11
212	Device Word 2, Bit 8	412	12

4.2.3 PX201 through PX212

The third set of pulses set the 12 flip-flops in Control Register 2, as listed in Table 7. The specific use for an experimenter is listed in Tables 7A and 7B respectively, in Appendices A and B. The detailed logic, including the connections from the output of Control Register 2 through any special drive logic to a device cable (Table 6), is on Dwg. Nos. Q-5098-10, -20, -30, etc.

Table 7. Pulse Group 2 assignments to set Control Register 2

Address	CEU 2nd word	Pulse	Function
X2	104000	PX201	Set register 2, Bit 1
X2	102000	PX202	Set register 2, Bit 2
X2	101000	PX203	Set register 2, Bit 3
X2	100400	PX204	Set register 2, Bit 4
X2	100200	PX205	Set register 2, Bit 5
X2	100100	PX206	Set register 2, Bit 6
X2	100040	PX207	Set register 2, Bit 7
X2	100020	PX208	Set register 2, Bit 8
X2	100010	PX209	Set register 2, Bit 9
X2	100004	PX210	Set register 2, Bit 10
X2	100002	PX211	Set register 2A, Bit 11
X2	100001	PX212	Set register 2A, Bit 12

4.3 Scaler Word Gating

The scaler word gating logic on Dwg. Nos. Q-5098-1, -2, -3, -4, -5, and -6 is condensed in Fig. 4. The AND gates labeled "S" and "D" are repeated 8 and 16 times respectively in the logic to form the gate scaler (GSCLROY) and the gate device (GDEVY) signals. The two gating flip-flops [1A8]^{*} in the control circuitry allow for expansion of the

^{*}In Dwg. No. Q-5098-1, location A8 referred to the edges of drawing.

Fig. 4. Scaler Word 1 and 2 gating and control.

Scaler Bus (when needed) to 16 inputs by the addition of a few gates on the GSCLRBO line. The GSCLROY signals are in area G on Dwg. Nos. Q-5098-1 and -2. The GDEVY signals are on the left of Dwg. Nos. Q-5098-3, -4, -5, and -6.

4.3.1 Scaler Input Bus

The Scaler Input Bus (Dwg. Nos. Q-5098-5 and -6) is driven by the outputs of a Jorway, Dual Scaler Model 1836 with options. Note that gating diodes are in the scaler on each BCD output line with the cathode tied to the Input Bus. A 1000- Ω resistor (on card B19) completes the diode OR gate. The switching threshold of the M510 I/O Bus Receiver is 1.5 V. The GSCLROY signals are routed over the Scaler Input Bus cable as Gate Scaler 1A, 1B, 2A, etc. [11D11]. Table 8 lists the pin assignments at the Device Controller for the 8421 BCD outputs on the Scaler Input Bus. The connector parts are shown on Dwg. No. Q-5098-5.

4.3.2 Device Word Input

Pin assignments for a device cable are listed in Table 6. The connector parts are shown on Dwg. No. Q-5098-4. A typical input for the existing device words is routed through a switch monitor receiver Dwg. No. (Q-5098-8A) as shown on Dwg. Nos. Q-5098-12, -22, and -32 listed in Appendices A, B, and C. The signals from each experimenter are conditioned by component selection (tabulated for each set on Dwg. No. Q-5098-8A) on the switch monitor receiver card.

The device word bit assignments for devices 0, 1, 2, etc., are listed in Tables 6A, 6B, and 6C in Appendices A, B, and C for JAH, RLM, and GDS Device Controllers.

4.4 OPERATE Monitor

The OPERATE logic which may be modified for a particular experimenter's needs is drawing -X1 in Table 2a; Dwg. No. Q-5098-21 will be used to describe the operation. The output of NAND gate A9 [11A/] is the negative

Table 8. Scaler Input Bus (J408) pin assignments

Pin	Use		Pin	Use	
	Scaler	Drawings		Scaler	Drawings
101	8	(WD1B0)	301	40	(WD2B9)
102	4	(WD1B1)	302	20	(WD2B10)
103	2	(WD1B2)	303	10	(WD2B11)
104	1	(WD1B3)	304	8	(WD2B12)
105	8	(WD1B4)	305	4	(WD2B13)
106	4	(WD1B5)	306	2	(WD2B14)
107	2	(WD1B6)	307	1	(WD2B15)
108	1	(WD1B7)	308		
109	8	(WD1B8)	309		
110	4	(WD1B9)	310		
111	2	(WD1B10)	311		
112	1	(WD1B11)	312		
113	8	(WD1B12)	313		
201	4	(WD1B13)	401	Gate Scaler 1A	(GSCLR00)
202	2	(WD1B14)	402	Gate Scaler 1B	(GSCLR01)
203	1	(WD1B15)	403	Gate Scaler 2A	(GSCLR02)
204	8	(WD2B0)	404	Gate Scaler 2B	(GSCLR03)
205	4	(WD2B1)	405	Gate Scaler 3A	(GSCLR04)
206	2	(WD2B2)	406	Gate Scaler 3B	(GSCLR05)
207	1	(WD2B3)	407	Gate Scaler 4A	(GSCLR06)
208	8	(WD2B4)	408	Gate Scaler 4B	(GSCLR07)
209	4	(WD2B5)	409	Ground	(Ground)
210	2	(WD2B6)	410		
211	1	(WD2B7)	411		
212	80	(WD2B8)	412		

OPERATE signal. It drives a one-shot multivibrator A14 [11A8] whose output generates the four Start Scaler pulses. The negative OPERATE signal is inverted at inverter A13 so that the OFF condition will generate a pulse in a second one-shot multivibrator whose output drives the four Stop Scaler pulse drive circuits.

The three inputs to the OPERATE NAND gate [11A7] are Multiplexer Control, Program On, and a dc level from a switch labeled FAKE LINAC PULSES. The switch allows testing of equipment when the linear accelerator is off. The Multiplexer Control signal supplies the SEL 810B computer RUN signal, a Multiplexer Channel Enabled Status, and the Unit Connected⁵ signal from the Four-Channel Priority Multiplexer. (The logic is shown on multiplexer Dwg. No. Q-5036-12). The Program On flip-flop is controlled by a Program Start pulse (PX003) and a Program Stop pulse (PX004) which supplies the state, Running or Stopped, of the computer program when the computer is in the RUN mode.

A fourth input to the OPERATE NAND gate, which is now tied to the switch input, can be used to supply other monitor inputs.

4.5 Control Registers

The control registers (Dwg. No. Q-5098-X0) have been used to control solenoid valves that supply air to a pneumatically operated linear filter assembly* (paddle sample changer) or sample positioner.[†] Two microswitches on each filter return an IN and an OUT position via device word input (Sect. 4.3.2).

A typical output has either an inverter (M111) or some type of driver (M651 for -3 V output), as required, to isolate the flip-flop (M203) from any external "noise" on the cabling to the solenoid valves.

* See Appendices A, B, and C for drawing reference on a particular flight path.

[†] See Appendix B, Engineering Drawings.

4.6 Special Control Circuits

Special control circuits are described in Appendices A, B, and C, as required.

5. ISOLATED PULSE GENERATOR

The ORELA Isolated Pulse Generator is a two-wide NIM unit that was designed to provide pulse outputs from the SEL 810B Scaler Interface. It is used by those experimenters who do not require scaler or device read-in, but have applications for program-generated monitor pulses.

Four pulses have been assigned the identical functions of subaddress "0" in the Device Controller as listed in Table 4b. All other pulses can be used as the experimenter desires.

5.1 Operation

The logic for the unit is on Dwg. No. Q-5109-1. Each pulse circuit consists of a ground isolating receiver (ISC 142-2), two inverters (M111) in series for restoring the pulse edges, and an AND gate (M101) with subaddress 0, Group X (SELX0) as the gating level. (The circuitry is identical to that in a Device Controller.) The SELX0 level is the output of an AND gate (M617) whose inputs are Group X, SCSEL4, SCSEL2, and SCSEL1. The pulse outputs are +3 V to ground from the M101 gate. Five positive outputs can be provided (two are shown as an option) by using the subaddress inverters.

There are four spare M617 NOR gates. A pair of these gates could be cross-coupled as an R-S flip-flop, which could then be set and reset by two pulses.

5.2 Assembly

The assembly drawing is Dwg. No. Q-5109-4, with a parts list on the drawing; Dwg. No. Q-5109-3 contains the front metalphoto panel and the

rear connector panel. The cabling through the ground isolation chassis (Dwg. No. Q-5036-30) to the Scaler Interface on the SEL 810B computer is shown on Dwg. No. Q-5109-1. Pin assignments for pins 304, 308, 309, 310, and 710 through 713 in Table 3 are used by the Isolated Pulse Generator.

6. MAINTENANCE

A test program, 8SCL Entry 6, is available to test the address selection (Group Number, Device Number) and pulse generation by using the control switches to select pulses. Entries 3 and 4 display 32 bits of data in the A and B registers. Other functions in the three existing Device Controllers are tested by four entries (0, 1, 2, and 5). The instructions from the 8SCL program are given in Fig. 5.

A list of the latest version of the 8SCL program can be obtained by typing the following ODAR⁴ commands:

```
* 7MUP
+ 10, "8SCL"
```

Note the modification date in the second line to see if a later version of the program is being used. The date and time in the first line indicate when the program was assembled.

The calling parameters for 8SCL are Entry Number, Group Number, Device Number, and Time. The time parameter is not used in Entry 6. The device number must be zero for the ORELA Isolated Pulse Generator unless the hardware has another device number wired into it. The ODAR calling sequence is the following:

```
* 8SCL
+ 6, X, 0, 0 where X is Group Number 0, 1, 2, or 3.
```

Set sense switch to return to the system when testing is completed.

```

*8SCL[106,1000] SCALER INTERFACE AND J.W. REYNOLDS BLDG 6010
* 5-23-73 DEVICE CONTROLLER TEST
* SET SNS 15 TO RETURN TO THE SYSTEM, EXCEPT ENTRY 6 USE SNS 1.
*** NOTES
* GROUP NO. = X IN LISTING. IT IS THE MULTIPLEXER CHANNEL NO.
* DECIMAL 42 IS APPROXIMATELY 1 SECOND OF "TIME".
*** ENTRY PARAMETER FUNCTION
* 0. GROUP NO., 2, -TIME (X 25MS) RUN HOT SAMPLE CONTINUOUS
* A SELECTED TIME PERIOD, FORWARD THEN REVERSE.
* 1. GROUP NO., 2, -TIME (X 25MS) RUN HOT SAMPLE STEP FOR
* A SELECTED TIME PERIOD, FORWARD THEN REVERSE.
* 2. GROUP NO., 2, -40 ( 1 SECOND ) MOVE PADDLES, FILTERS, OR
* BEAM STOP AND DISPLAY BY SETTING THE CONTROL SWITCHES.
* JAH BEAM STOP OUT, SET CONTROL SWITCH 0, REGISTER 2, BIT 2.
* JAH-RLM FILTERS ARE SET BY CONTROL SWITCHES 1 THRU 10.
* GES BEAM STOP OUT, SET CONTROL SWITCH 2, REGISTER 1, BIT 2.
* GES LINEAR FILTERS SET BY CONTROL SWITCHES 3 THRU 12.
* 3. GROUP NO., SCALER NO., -TIME SCALER DISPLAY
* 4. GROUP NO., DEVICE NO., -TIME DEVICE DISPLAY
* 5. GROUP NO., TIME (MINUTES), 2 PERIODIC PRINT OF SCALERS
* SET SNS 0 TO STOP PRINTING.
* SET SNS 1 FOR NO RESET OF SCALERS
* TIME = XXX FOR MINUTES
* TIME = '10XXXX FOR 60/SEC. ('100341 = .5 MIN.)
* 6. GROUP NO., DEVICE NO., 0 CONTROL SW. PULSE PATTERN

```

Fig. 5. 8SCL instructions.

7. ENGINEERING DRAWINGS

The following drawings are related to the topics discussed in this volume. They are not included here due to space limitations, but are available from the authors.

- Q-2928-2 — ORELA Data Acquisition, Bldg. 6010, Central Data Area, Computer Equipment Layout
- Q-2928-5 — ORELA Data Acquisition, Experimenters Equipment Layout
- Q-2928-11 — ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors
- Q-5098 — (see Tables 1 and 2)
- Q-5109-1 — ORELA Isolated Pulse Generator, Select Code X0 and Pulse X01 through X12
- Q-5109-3 — ORELA Isolated Pulse Generator, Front and Rear Panels
- Q-5109-4 — ORELA Isolated Pulse Generator, Module Assembly
- ISC 142-1 — Isolated Digital Line Driver/Coupler/Level Shift Card
- ISC 142-2 — Isolated Digital Line Receiver/Coupler/Level Shift Card

REFERENCES

1. J. W. Reynolds, *ORELA Data Acquisition System Hardware, Volume 3, Scaler Interfaces*, ORNL/TM-5640, Oak Ridge National Laboratory, Oak Ridge, Tenn., 1976.
2. Systems Engineering Laboratories, Inc., *Technical Manual Data Acquisition System*, June 1969, vol. 1, pp. 3-1 to 3-7.
3. Systems Engineering Laboratories, Inc., *Reference Manual, SEL 810B General Purpose Computer*, November 1968.
4. N. A. Betz, J. G. Craven, and D. R. Winkler, *The ORELA Data Acquisition Monitor System*, unpublished internal report (available from J. G. Craven, ORNL).
5. Systems Engineering Laboratories, Inc., *Design Manual, Input/Output Interface, SEL 810B Computer*, August 1968, Sect. IV.

APPENDIX A

JAH Special Control

	<u>Page</u>
4.6A* Hot-Sample Changer Motor Drive	26
4.6.1A Step Mode	26
4.6.2A Continuous Mode	26
 Table 2A.* ORELA Device Controller, JAH logic	 28
Table 5A. JAH Pulse Group 1 assignments to set Control Register 1	29
Table 6A0. JAH Device 0 data bit assignments	30
Table 6A1. JAH Device 1 data bit assignments	31
Table 6A2. JAH Device 2 data bit assignments	31
Table 7A. JAH Pulse Group 2 assignments to set Control Register 2	32

Engineering Drawings[†]

M-11300-EK-105-E ORELA Flight Path One, Linear Filter Assembly
 Q-5115-1 Flight Path One Sample Changer, Wiring Diagram

* Section numbers and table numbers in the appendix refer to related sections and tables in the text. For example, Sect. 4.6A is an addition to Sect. 4.6, Table 2A is related to Table 2.

[†] These drawings are not included here, but are available from the authors.

4.6A Hot-Sample Changer* Motor Drive

The motor drive for the Hot-Sample Changer has two modes of operation: Step and Continuous.

4.6.1A Step Mode

The Step Mode is selected by pulse PX008 (Table 4a) to the Step-Continuous flip-flop (Control Register 2, bit 11) on Dwg. No. Q-5098-10E9. The computer program then generates the Hot Forward (PX111) or Hot Reverse (PX112) pulses (Table 5A) as required to set a particular position and angle through computer program monitoring of the Device 2 input signals (Table 6A2).

If the reference position is detected while seeking a position, the computer program reverses the direction of motion. It is necessary to clear the Hot Forward and Hot Reverse flip-flops using pulse PX007 (reset Control Register 1A, bits 11 and 12) before setting the other direction of motion.

The desired sample positions and angles are: position 1 and 73.4°, 2 and 116.7°, 3 and 165.4°, and 4 and 210.3°.

4.6.2A Continuous Mode

Continuous Mode is selected by producing pulse PX211 (Table 7A) to set Control Register 2, bit 11 followed by a pulse to set either Hot Forward (PX111) or Hot Reverse (PX112). The direction pulse triggers the same one-shot used in Step Mode. The trailing edge of the drive pulse triggers a delay (8 msec) one-shot whose trailing edge retriggers the drive one-shot. Continuous Mode is terminated when the desired coarse position is detected during a periodic check by the computer program. The fine positioning (angle) is accomplished with the Step Mode.

* Idaho Nuclear Corporation, ORELA Sample Changer.

The Slo-Syn Translator (Model ST1800) supplied as part of the Hot-Sample Changer uses the 125 pulse/sec pulse train to drive a Slo-Syn motor which positions the sample changer. The position readings are produced by microswitches. The angle reading is produced and visually indicated by a shaft encoder.* The pin assignments for the sample changer, connector pair P402/J402, are listed on Dwg. No. Q-5098-12.

*Computer Control Corporation, Model DS70.

Table 2A. ORELA Device Controller, JAH logic
ORNL I&C Division Drawing Series Q-5098

Number	Title
-10	Control Registers (JAH), 5 & 10 Meter Paddles, Beam Stop, and Hot Sample Changer Motor Control Status
-11	OPERATE, Scaler Control, Lamp Drivers, and Hot Sample Motor Control Pulses (JAH)
-12	Monitor Switch Receivers (JAH)
-19	Module Utilization (JAH) and Cabling Diagram

Table 5A. JAH Pulse Group 1 assignments to set Control Register 1

Address	CEU 2nd word	Pulse and center pulse	Function
X1	104000	PX101	Set register 1, Bit 1 5-m paddle 1 in
X1	102000	PX102	Set register 1, Bit 2 5-m paddle 2 in
X1	101000	PX103	Set register 1, Bit 3 5-m paddle 3 in
X1	100400	PX104	Set register 1, Bit 4 5-m paddle 4 in
X1	100200	PX105	Set register 1, Bit 5 5-m paddle 5 in
X1	100100	PX106	Set register 1, Bit 6 10-m paddle 6 in
X1	100040	PX107	Set register 1, Bit 7 10-m paddle 7 in
X1	100020	PX108	Set register 1, Bit 8 10-m paddle 8 in
X1	100010	PX109	Set register 1, Bit 9 10-m paddle 9 in
X1	100004	PX110	Set register 1, Bit 10 10-m paddle 10 in
X1	100002	PX111	Set register 1A, Bit 11 Hot Forward
X1	100001	PX112	Set register 1A, Bit 12 Hot Reverse

Table 6A0. JAH Device 0 data bit assignments

Bit	Word 1	Word 2	Function
0	In	Out	Beam stop
1	In	Out	5-m paddle 1
2	In	Out	5-m paddle 2
3	In	Out	5-m paddle 3
4	In	Out	5-m paddle 4
5	In	Out	5-m paddle 5
6	In	Out	10-m paddle 6
7	In	Out	10-m paddle 7
8	In	Out	10-m paddle 8
9	In	Out	10-m paddle 9
10	In	Out	10-m paddle 10

The following bits are temporarily wired open
at the device control:

11	Closed	Open	5-m vacuum valve
12	Closed	Open	10-m vacuum valve
13	Closed	Open	78-m shutter
14	Closed	Open	82-m shutter
15	Closed	Open	200-m shutter

Table 6A1. JAH Device 1 data bit assignments

Bit	Word 1 function	Word 2 function
0	Geneva mech. operate.	
1	Geneva position 1	
2	Geneva position 2	
3	Geneva position 3	
4	Geneva position 4	Spare
5	Spare	Spare
6	210-m shutter closed	210-m shutter open
7	400-m shutter closed	400-m shutter open
8		
9		
10		
11		
12		
13		
14		
15		

Table 6A2. JAH Device 2 data bit assignments

Bit	Word 1 function	Word 2 function
0	Hot reference position	
1		200 degrees
3		100 degrees
4		80 degrees
5		40 degrees
6		20 degrees
7		10 degrees
8		8 degrees
9		4 degrees
10		2 degrees
11		1 degree
12		0.8 degree
13	Hot position 4	0.4 degree
14	Hot position 2 (2 and 3)	0.2 degree
15	Hot position 1 (1 and 3)	0.1 degree

Table 7A. JAH Pulse Group 2 assignments to set Control Register 2

Address	CEU 2nd word	Pulse and center pulse	Function
X2	104000	PX201	Set register 2, Bit 1 Spare
X2	102000	PX202	Set register 2, Bit 2 Beam stop out
X2	101000	PX203	Set register 2, Bit 3 Spare
X2	100400	PX204	Set register 2, Bit 4 Spare
			Bits 5 through 10 are not used
X2	100002	PX211	Set register 2A, Bit 11 Hot Continuous Mode
X2	100001	PX212	Set register 2A, Bit 12 not used

APPENDIX B

RLM Special Control

Signal conditioning on drawings. No special functions.

	<u>Page</u>
Table 2B.* ORELA Device Controller, RLM logic	34
Table 5B. RLM Pulse Group 1 assignments to set Control Register 1	35
Table 6B0. RLM Device 0 data bit assignments	36
Table 7B. RLM Pulse Group 2 assignments to set Control Register 2	36

Engineering Drawings[†]

M11282-EK-037-E ORELA Flight Path 7, Linear Filter Assembly
I-11282-QJ-001 ORELA Flight Path 7, Sample Positioner Assembly

* Table numbers in the appendix are correlated with related tables in the text. For example, Table 2B is associated with Table 2.

[†] These drawings are not included here, but are available from the authors.

Table 2B. ORELA Device Controller, RLM logic
ORNL I&C Division Drawing Series Q-5098

Number	Title
-20	Control Registers (RLM), 5 Meter Filters and 40 Meter Sample Changer
-21	OPERATE, Scaler Control, and Lamp Drivers (RLM)
-22	Switch Receivers and 40 Meter Interface (RLM)
-28	40 Meter Control (RLM)
-29	Module Utilization (RLM) and Cabling Diagram

Table 5B. FLM Pulse Group 1 assignments to set Control Register 1

Address	CEU 2nd word	Pulse and center pulse	Function
X1	104000	PX101	Set register 1, Bit 1 5-m filter 1 in
X1	102000	PX102	Set register 1, Bit 2 5-m filter 2 in
X1	101000	PX103	Set register 1, Bit 3 5-m filter 3 in
X1	100400	PX104	Set register 1, Bit 4 5-m filter 4 in
X1	100200	PX105	Set register 1, Bit 5 5-m filter 5 in
X1	100100	PX106	Set register 1, Bit 6 40-m sample 1 in
X1	100040	PX107	Set register 1, Bit 7 40-m sample 2 in
X1	100020	PX108	Set register 1, Bit 8 40-m sample 3 in
X1	100010	PX109	Set register 1, Bit 9 40-m sample 4 in
X1	100004	PX110	Set register 1, Bit 10 Spare
X1	100002	PX111	Set register 1A, Bit 11 Spare
X1	100001	PX112	Set register 1A, Bit 12 Spare

Table 6B0. RLM Device 0 data bit assignments

Bit	Word 1	Word 2	Function
0	In	Out	Beam stop
1	In	Out	5-m filter 1
2	In	Out	5-m filter 2
3	In	Out	5-m filter 3
4	In	Out	5-m filter 4
5	In	Out	5-m filter 5
6	Closed	Open	5-m vacuum valve
7	In	Out	40-m sample 1
8	In	Out	40-m sample 2
9	In	Out	40-m sample 3
10	In	Out	40-m sample 4
11	"Zero"	"One"	Spare wired
12	Closed	Open	40-m vacuum valve
13	"Zero"	"One"	Wired
14	"Zero"	"One"	Wired
15	"Zero"	"One"	Wired

Table 7B. RLM Pulse Group 2 assignments to set Control Register 2

Address	CEU 2nd word	Pulse and center pulse	Function
X2	104000	PX201	Set register 2, Bit 1 Spare
X2	102000	PX202	Set register 2, Bit 2 Spare
Bits 3 through 12 are not used			

APPENDIX C

GDS Special Control

Signal conditioning on drawings. No special functions.

	<u>Page</u>
Table 2C.* ORELA Device Controller, GDS logic	38
Table 5C. GDS Pulse Group 1 assignments to set Control Register 1	39
Table 6C0. GDS Device 0 data bit assignments	40

Engineering Drawings[†]

M11297-EK-515-E ORELA Flight Path 5, Linear Filter Assembly
Q-2956-40 thru 47 Linear Filter Control

* Table numbers in the appendix are correlated with related tables in the text. For example, Table 2C is associated with Table 2.

[†] These drawings are not included here, but are available from the authors.

Table 2C. ORELA Device Controller, GDS logic
ORNL I&C Division Drawing Series Q-5098

Number	Title
-30	Control Register (GDS), Beam Stop, and Linear Filters 1 to 10
-31	OPERATE, Scaler Control, Lamp Drivers, and Positive Pulses PX301 thru PX306 (GDS)
-32	Monitor Switch Receivers (GDS)
-39	Module Utilization (GDS) and Cabling Diagram

Table 5C. GDS Pulse Group 1 assignments to set Control Register 1

Address	CEU 2nd word	Pulse and center pulse	Function
X1	104000	PX101	Set register 1A, Bit 12 Spare
X1	102000	PX102	Set register 1A, Bit 11 Beam stop out
X1	101000	PX103	Set register 1, Bit 1 Linear filter 10
X1	100400	PX104	Set register 1, Bit 2 Linear filter 9
X1	100200	PX105	Set register 1, Bit 3 Linear filter 8
X1	100100	PX106	Set register 1, Bit 4 Linear filter 7
X1	100040	PX107	Set register 1, Bit 5 Linear filter 6
X1	100020	PX108	Set register 1, Bit 6 Linear filter 5
X1	100010	PX109	Set register 1, Bit 7 Linear filter 4
X1	100004	PX110	Set register 1, Bit 8 Linear filter 3
X1	100002	PX111	Set register 1, Bit 9 Linear filter 2
X1	100001	PX112	Set register 1, Bit 10 Linear filter 1

Table 6C0. GDS Device 0 data bit assignments

Bit	Word 1	Word 2	Function
0	In	Out	
1	In	Out	
2	In	Out	
3	In	Out	
4	In	Out	
5	In	Out	Beam stop
6	In	Out	Linear filter 10
7	In	Out	Linear filter 9
8	In	Out	Linear filter 8
9	In	Out	Linear filter 7
10	In	Out	Linear filter 6
11	In	Out	Linear filter 5
12	In	Out	Linear filter 4
13	In	Out	Linear filter 3
14	In	Out	Linear filter 2
15	In	Out	Linear filter 1

ORNL/TM-5641
(Vol. 4 of ORNL/TM-5638)

Internal Distribution

1. C. J. Borkowski	17. R. P. Rosenbaum
2. J. G. Craven	18. J. H. Todd
3. J. A. Harvey	19. H. A. Todd
4. N. W. Hill	20. R. E. Wintenberg
5. R. W. Ingle	21. J. W. Woody
6. J. A. Keathley	22-39. ORELA Computer System File,
Bldg. 6010
7. F. C. Maienschein	40-41. Central Research Library
8. F. W. Manning	42-44. Laboratory Records Department
9. J. W. McConnel	45. Laboratory Records - ORNL R.C.
10. E. McDaniel	46. ORNL Document Reference Section
11. R. W. Peele	47. ORNL Patent Office
12-16. J. W. Reynolds	

External Distribution

48. Director, Research and Technical Support Division ERDA-ORO
49-75. Technical Information Center, P.O. Box 62, Oak Ridge,
Tennessee 37830