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DIP COATING PROCESS

Silicon Sheet Growth Development for the
Large-Area Silicon Sheet Task of the
Low-Cost Silicon Solar Array Project

Quarterly Report No. 6

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Work Performed Under Contract No. NAS-7-100-954356

Honeywell Corporate Material Sciences Center
Bloomington, Minnesota

ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

During this quarter, significant progress was made in silicon on ceramic (SOC) solar cell performance. SOC cells having 1 cm^2 active areas demonstrated measured conversion efficiencies as high as 7.2 percent. Typical open circuit voltages (V_{oc}) and short circuit current densities (J_{sc}) were 0.51 volt and 20 mA/cm^2 respectively. Since the active surface of these solar cells is a highly reflective "as-grown" surface, one can expect improvement in J_{sc} after an anti-reflection (AR) coating is applied. It is significant that single-crystal comparison cells, also measured without benefit of an AR coating, had efficiencies in the 8.5 percent range with typical V_{oc} 's and J_{sc} 's of 0.54 volt and 23 mA/cm^2 , respectively. Therefore, improvement in cell design and junction diffusion techniques should increase the efficiency of both the SOC and single-crystal cells.

During this quarter the dip coating facility was inadvertently contaminated, but has since been restored to a purity level exceeding its original state. With this facility, silicon coatings were grown with a single-crystal seed attached to the substrate. Single-crystal silicon was not forthcoming, but the results were nonetheless encouraging. Several of the carbon coating types tried appear promising, including one which has high purity and can be applied uniformly by swab or airbrush.

To date chemical analysis techniques have not revealed any impurity segregation at grain boundaries, either before or after diffusion. It is also encouraging to note that even when the melt is given a significant exposure to mullite, SOC solar cells can be made from the resulting silicon with V_{oc} 's and J_{sc} 's that are within 9 percent of those obtained in single-crystal comparison cells.

A scanning light beam (LBIC) was used this quarter to identify regions of low minority carrier diffusion length and poor solar cell efficiency. The photodiode short circuit current decay (PSCCD) technique was also evaluated and does not seem to be a simple method of measuring minority carrier lifetime.

The design of the continuous coating facility has been completed and the construction of this facility is proceeding on schedule.

Latest figures from our economic analysis stress the fact that SOC growth rates should be greater than 0.3 cm/sec.

INTRODUCTION

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon, which offers an outstanding cost-effective way to manufacture inexpensive, large-area solar cells.

This SOC approach has excellent scale-up potential. With the dip coating method it is possible to coat several wide, large-area substrates in one dipping. Another method we are pursuing is to silicon coat, in a continuous manner, large-area substrates. The investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

Since the inception of this program, an experimental dip coating facility was designed and constructed. In this facility a variety of ceramic materials have been dip coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25cm^2 in area have been achieved with single-crystal grains as large as 4mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this (SOC) sheet silicon is promising. To date 1cm^2 solar cells have been fabricated, without the benefit of an antireflection coating (AR) and minimized series resistance, that have conversion efficiencies in the 7 percent region.

Such cells typically have open circuit voltages and a short circuit current densities of 0.51 volt and 20 mA/cm² respectively. Application of an AR coating to these cells would improve their efficiency in the direction of the program's ultimate 12 percent goal.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The aluminum and other impurities of the substrate are believed to adversely affect solar cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar cell performance should be forthcoming. An alternate method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, as previously mentioned, a silicon coating facility is being constructed which is designed to coat large (10 cm x 100 cm) substrates in a continuous manner. It is expected that this new facility will not only improve the growth rate, but also minimize the silicon melt's contact with the substrate. This should reduce the rate at which the melt becomes contaminated. Further, this new facility will permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

The balance of this document will report the progress achieved during the past quarter year of effort.

TECHNICAL DISCUSSION

SILICON FILM GROWTH MECHANISM (R. B. Maciolek, D. Sauve, S. Marquardt, and K. Wuori)

Apparatus and Procedure

During the second quarter of 1977 the dip coating apparatus was dismantled, cleaned and reassembled. It is once again operating satisfactorily. A total of 16 runs (numbers 52-67) have been made during this quarter, including three "wiping experiments" to determine conditions for horizontal coating. The first few runs were made to reestablish growth conditions and understandably gave low yields. Subsequent runs went as planned and were productive. One of the runs was a dummy during which the melt was held at a typical growth temperature for six hours, but no substrates were dipped. This was done to check the cleanliness of the apparatus. Resistivity measurements made at the conclusion of the run were high, 100-1,000 ohm cm, n-type, indicating the melt had not been contaminated.

Starting with run number 55, He has been used as the atmosphere in the apparatus rather than Ar. The use of He suppresses the collection of Si vapor on the viewports and chamber walls.

One substrate was dipped that had been etched for 30 minutes in HF prior to carbon coating. This was done to clean the surface and increase the surface porosity to promote adherence of the Si. The dipped substrate cracked and broke upon cooling and the Si film spalled off. The increased porosity apparently acted to notch the substrate and at the same time hold too much graphite on the surface which promoted spalling.

Four substrates were dipped with single-crystal Si seeds attached. Thin wafers of single-crystal Si were simply clamped to the substrate at the top edge of the carbon coating. The results can be seen in Figure 1, which shows the interface between the single crystal seed and the ensuing silicon film. Although the desired result, single-crystal film growth, did not occur, the procedure shows promise. The seed-film junction is continuous, indicating that with a suitably oriented seed, large grain growth may be induced.

A new numbering system which has been initiated to identify the samples incorporates certain information about the ceramic substrate and graphite coating. For example,

Figure 1. Seeded Si sheet growth. The seed is the trapezoidal shape at the top of the photo (Wright etch, 2.5X).

59-10M6H means the 59th run, 10th substrate dipped in that run; M is for McDanel, 6 is the Ceramic Center's batch identification, and H is for hand-rubbed graphite. The meaning of other letters which may appear is explained in the key at the bottom of the data sheet.

The substrates coated during this quarter are listed in the Appendix along with a summary of the coating conditions.

Substrate Carbonization

Work continued on the evaluation of the Dylon carbon coatings (graphite-water suspensions from Dylon Industries, Cleveland, Ohio), and two other methods of carbon coating substrates were investigated during this report period. A total of 22 substrates were dipped that had been coated with the various Dylon compounds. It was found necessary to oven dry these coatings, as residual moisture caused them to blister or "boil" off when dipped in the molten silicon, as shown in Figure 2. It was also noted that the granular nature of most of these coatings promoted nucleation which decreased the grain size (see Figure 3), and that carbides formed throughout the Si layer (see Figure 4). However, in cases where the granular surface was smoothed by wiping off the excess graphite and the coating was oven dried, the Dylon coatings gave large grain size similar to the hand-rubbed graphite coatings. Unfortunately our chemical analysis of these coatings has revealed that they contain from 1 to 2 percent impurities--a fact the vendor would not reveal--and are probably unsuited for our application.

Three substrates coated with 'dag' dispersion number 154, an alcohol-colloidal carbon suspension obtained from Acheson Colloids Co., Port Huron, Michigan, looked very promising. Drying poses no problems, and thickness is easier to control than the Dylon coatings. The growth morphology of the Si did not seem to be influenced by the coating either. The 'dag' was applied with either a swab or an airbrush. Preliminary analysis also indicates that the carbon used in the product is quite pure and should be suitable for solar cell application.

A third and somewhat novel method of carbon coating by plasma decomposition of propane gas in an RF sputtering apparatus was also investigated. The carbon is deposited uniformly and its purity should reflect that of the gas used. The morphology and grain size of the silicon film formed on such substrates is comparable to those on hand-rubbed graphite coatings.

Figure 2. Blistered and spotty Si film formation as the result of incomplete drying of Dylon Carbon Coatings (1.7X).

Figure 3. Photomicrograph of an etched "as-grown" surface of a Si film formed on a Dylon coating showing the decrease in grain size caused by the granular carbon coating. (Wright etch, 82.5X)

Figure 4. Carbides formed throughout Si layer grown on Dylon-coated substrate (unetched, 500X).

Chemical Characterization

During this quarter we performed further leaching experiments in an attempt to decrease the metallic impurities at the surface of the ceramic. This would permit us to evaluate the effect of impurities on solar cell performance, and would perhaps permit the use of ceramics with a high degree of impurity content.

The chemical analysis of the leached samples of MV-20 ceramic has been completed, using emission spectroscopy. As discussed in the previous quarterly report, HF leaching dramatically whitened the ceramic by dissolving the glassy phase, but did not change the metal impurity content. HCl or H₂SO₄ leaching had no detectable effect on either color or impurities. However, if the HF leach is followed by an HCl or H₂SO₄ leach, there is some reduction of impurities as shown in Table 1.

Table 1. Chemical Analysis of Leached Mullite

	<u>HCl only *</u>	<u>HF/HCl</u>	<u>HF/H₂SO₄</u>
Fe	0.73%	0.25%	0.34%
Mn	0.64	<0.03	0.035
Mg	0.31	<0.15	0.19
Ca	0.09	<0.03	0.059
Na	0.18	0.09	0.014
Ti	0.39	0.16	0.13
V	0.03	0.03	0.03

* The unleached and H₂SO₄ only were essentially identical to the HCl only results.

Generally the HCl was more effective as a second step than H₂SO₄, except in the case of Ti, the oxide of which is more soluble in H₂SO₄.

Future activity will involve looking at the performance of solar cells made on the above types of substrates to compare the effect of impurities on cell performance.

Two days were spent at Applied Research Laboratories analyzing impurities in SOC samples and comparing them with single crystal results. Both the IMMA system and the QMAS systems were used. The IMMA system was used to look for evidence of impurity segregation and preferential phosphorus diffusion at grain boundaries. Sample MR47 was selected as being likely to have a large amount of metal impurities since it was grown in a melt which had been exposed to silicon for over an hour. Photodiodes made on this substrate showed rather poor characteristics.

Several diode areas were examined in the imaging mode. One region was selected as having a fairly large angle grain boundary and a region of irregular surface texture, indicating small crystal size. This area was sputtered to a depth such that most of the n^+ phosphorus diffused layer had been removed. After profiling, the area still showed some mass 27 (Al), 31 (P), 48 (Ti), and 54 (Fe). Images taken with a 10 μm ion beam showed no preferential distribution of any of these impurities.

In general, all the searching for segregation at grain boundaries by this technique gave negative results. The only images which showed nonuniform distribution of impurities were on surfaces that had not been sputtered. Sample MR105 showed clustering of masses 23 (Na), 27 (Al), 48 (Ti), and 54 (Fe7). These did not appear to correlate with structural features.

The QMAS machine was used to look for impurities in the SOC samples. Comparison with a silicon standard from JPL containing 2 ppma aluminum gave 26 ppma using the standard calibration program. The numbers depend on the presputtering (preburn) time, with lower concentrations after longer times. Thus surface cleanliness is clearly important for good results. All the samples were grown from melts which had been exposed to mullite for long times. The only independent check is the Al content, which should correlate with resistivity measurements. This correlation was quite poor. Sample MR78TC should have had considerably less Al than MR47, whereas they both showed the same amount, both higher than the values indicated from resistivity. The Al content indicated for sample MR105 was beyond the solubility limit. The discrepancy could well be due to residual Al from the surface.

We basically believe in the capability of the QMAS system, but need a consistent procedure for cleaning samples to avoid "driving in" of impurities.

Analysis of Silicon - Carbon Interface

A number of interesting observations have been made regarding the silicon-carbon interface. In the last quarterly report we presented evidence that the electrical contact between the silicon and vitreous carbon can be low in resistance, though it tends to be nonuniform. The same samples were mounted in a metallurgical mount, and have been cut and polished to show the cross section. The microscope showed that there was an interface layer that was harder than either the carbon or the silicon - a strong suggestion of silicon carbide formation.

These samples were then removed from the potting compound and the cross section was examined using scanning Auger microscopy (SAM) at Physical Electronics, Inc. Some of the results are shown in Figure 5. A complete Auger spectrum of the interfacial material showed only silicon and carbon, and no impurities (at the 0.1 percent level). It is interesting, however, that the shape of the carbon peak and the silicon to carbon stoichiometry varied from that of a polycrystalline silicon carbide standard. It is not known whether these discrepancies are significant, but they suggest that the form of silicon carbide is different from the usual form.

At any rate, several comments on the silicon-carbon interface are in order. The SiC appeared thickest at the top of sample MR78 which had been in the melt for an hour. Since it was much thicker than the carbon coating, the SiC must be formed from carbon particles which float to the top of the melt. There was no detectible SiC at the top of sample MR106 which had been in the melt a minimum amount of time. Away from the surface the SiC thickness appeared about the same in the two samples varying from 2 to 10 μm . Typically, the SiC was somewhat thinner than the vitreous carbon coating remaining.

The samples were etched in Sirtyl etch after polishing, which revealed the presence of cracks. The region shown in Figure 5 was selected because the SiC was of maximum thickness and because it showed some cracks in the silicon and at the silicon-SiC interface. These cracks may be responsible for the nonuniformity of the electrical contact, or it may be due to variations in SiC thickness.

EBIC Measurements

Additional EBIC measurements of diode uniformity were made during this quarter. In order to quantify the uniformity of the EBIC response, it is useful to use a line scan.

Figure 5. Scanning Auger micrographs of the silicon-vitreous graphite interface at 2500X. The picture at left is a secondary electron image, the center picture is the carbon image, and at right is the silicon image of a section of sample MR 106. Silicon is at the top, carbon is at the bottom, and the silicon carbide is in between.

Figure 6 shows some diode uniformity results obtained on diode R78D-42-6. The diodes show fairly uniform EBIC response in spite of poor structure. This diode had an actual efficiency of 6.5 percent, and a short circuit current of 22 ma/cm^2 , so it appears that reasonably good performance can be obtained in spite of poor crystallinity.

In general we have had trouble obtaining consistent measurements of minority carrier diffusion length using EBIC. The problems previously described relating to surface inversion and long-term drift have been significantly reduced with our current diode fabrication procedure. The mesa is defined as the last step in the process so that there is less oxide formation on the base region, and therefore less chance for surface inversion.

We have found that the offset current (EBIC current with the e-beam striking the base region) is significantly larger for larger diodes. This, together with amplifier problems, has prevented us from obtaining many point-by-point measurements of diffusion length (L_D). Although we expect to correct these problems, we plan to expand our efforts to measure diode uniformity and L_D by spectral response measurements with a focused light.

Spectral Response Measurements

During this quarter we also improved the system for spectral response measurements. The system contains a variable size aperture that is imaged onto the diode with an $F/2.8$ reflective objective. The diode surface can be viewed using an eyepiece and a beam splitter. Figure 7 shows a point-by-point scan on diode R107C-50-3a with two different wavelengths. The response at the short wavelength was quite uniform indicating that the light was collected within a diffusion length of the junction. The response at the longer wavelength indicates considerable variation in minority carrier diffusion length. The absorption coefficient at this wavelength should be about $29 \mu\text{m}$. Therefore, parts of the material had diffusion lengths less than this and parts of the material may have had diffusion lengths approaching $30 \mu\text{m}$.

(A) EBIC image of silicon-on-ceramic photodiode. R78D-42-6

(C) Same as (A) showing detail of grain structure

(B) EBIC line scan of bright line in (A) showing zero current level where beam crosses wire and particles.

(D) Line scan of (C) showing quantitative loss of EBIC signal at grain boundaries.

Figure 6. EBIC measurements of diode uniformity

Figure 7. LBIC scan of diode R107C-50-3a at two wavelengths. The vertical scale is in units of 10^{-9} amp at 910 mμ and 10^{-10} amp at 550 mμ. The horizontal scale is distance on the diode in units of 10 mμ.

The implications of this study are that the minority carrier diffusion lengths are quite nonuniform, and measurements of diffusion length such as SPV measurements should be interpreted in light of such variations.

Future activities will be aimed at quantum efficiency measurements as a function of wavelength at particular spots where the response appears to be spatially uniform. If the LBIC (Light Beam Induced Currents) method can be made to produce images with high resolution, it should be more useful than EBIC, because of the possibility of varying wavelength, and the lack of problems with e-beam charging.

Minority Carrier Lifetime Measurements

We have begun to set up a method for measuring minority carrier lifetime by looking at the decay of the photo current with time. A pulsed GaAs laser was used in a circuit that generated a 20-nsec pulse with a few-nsec rise and fall time. An advantage of this technique is that it can be used with fabricated diodes and so does not require any new fabrication steps. A weakness of the approach is that the absorption length of the 900-nm laser wavelength is about 25-30 μm, and so the technique may not be valid for material with diffusion lengths longer than this.

Various measurement techniques have been tried, and the results frequently depend on the measurement technique. The short circuit photodiode current was measured by shorting the diodes and using a clamp-on Tetrax current probe. Generally, shunting the diode with 5 ohms or less and impedance matching to a 50-ohm cable produced cleaner and more consistent signals. Photoconductive decay measurements could also be made using the two ohmic contacts in our photodiode pattern.

A number of measurements were taken, but the results did not give a unique, well-defined lifetime. The observations can be roughly summarized as follows:

- Photodiode short circuit current decay (PSCCD) measurements could be made independent of RC time constant affects by going to low values of R by shunting, or by applying sufficient reverse bias to decrease the capacitance.
- On single crystal samples, the PSCCD followed a rapid drop at first, presumably due to sweepout of carrier in the space charge region. The second part of the decay appeared to be exponential, but close examination revealed that it actually contained a number of time constants ranging from 150 nsec to more than 500 nsec.
- On SOC samples, the PSCCD followed the same behavior as above with roughly the same time constants. The initial decay was not as much, or as fast, presumably due to the narrower space charge region of the SOC diodes which had a more heavily doped base region.
- The photoconductive decay (PCD) measurements consisted of two parts: (1) a photovoltaic contribution, which could be of either sign, presumably associated with the preferential illumination of one contact; and (2) a true PCD contribution that was proportional to the bias current. This signal peaks about 200 nsec after the 20-nsec pulse is turned off.
- The PCD for the single-crystal samples indicated a fairly consistent exponential decay with a time constant of about 1 μ sec.
- The PCD for the SOC samples was very nonexponential with time constants at least 50 μ sec or longer. This must be due to majority carrier trapping, possibly at grain boundaries in the SOC material.

We conclude that these results are very interesting, but that a fair amount of analysis would be required to sort out the lifetime or lifetimes of minority carriers. The photovoltaic effect that occurs with the contacts may have an effect on the open circuit voltage of solar cells made with a base contact on the top surface.

Solar Cell Fabrication

The fabrication procedure outlined in the previous quarterly report has been implemented. Sputtered Pt is put down for the base contact, then sintered at 600°C. Sputtered Ni is used on top of the PtSi and as a contact to the n^+ region. The final mask is used to define the edge of the p-n junction using a plasma etch. Difficulties with mask registration have been eased by going to contact masks on glass plates with Fe_2O_3 patterns. The glass plates do not shrink during development and the Fe_2O_3 is semitransparent to darkroom light, but opaque as far as the photoresist is concerned. This procedure was found to be essential in going to a $10cm^2$ pattern, and sufficiently eased problems with the smaller patterns. The $10cm^2$ masks are completed and a single-crystal cell has been fabricated, but no $10cm^2$ SOC cells have yet been made.

Two types of patterns are being used at present, as illustrated in Figure 8. The photodiode pattern in Figure 8a is convenient for evaluating uniformity of the material and for EBIC, LBIC, PSCCD, and PCD measurements. The $1cm^2$ cell pattern was designed to have wide line widths and large tolerances on mask alignment for ease of fabrication. In laying out the pattern for the $10cm^2$ we were forced to use narrower line widths and 50 percent greater width between lines, so tolerances are smaller and the effect of spreading resistance may be more detrimental.

Photodiode and Solar Cell Performance

The results of measurements on small (few mm^2) photodiodes and on $1cm^2$ solar cells are summarized in Table 2. In taking averages, cells that were atypically poor were not included. Usually these were a small fraction of the total number.

Substrates 78 and 106 had vitreous carbon (Vitregraph) instead of rubbed graphite as the coating on the ceramic. There appear to be enough variations in processing that it is difficult to attribute any significant difference to the Vitregraph.

A number of diodes were made on Substrate R107A that had been diffused once, lightly etched to remove the diffused layer, then rediffused and processed. Although some of the diodes were the best to date, the statistical scatter is large enough that it is not clear if the gettering had any effect. The diffusion at 870°C should have given a sheet resistance higher than the observed $\rho_s = 18$ ohms/sq.

We developed the $1cm^2$ solar cell patterns (shown in Figure 8b) during this quarter and, after initial runs that were not successful because of obvious problems like misregistration, produced the results shown for substrates R172D and R169A in Table 2 and in Figures 9 and 10.

(a)

(b)

Figure 8. SOC solar cells, Magnification, 6X. (a) An array of 7 photodiodes. The central square is a base contact, as well as the outer region. (b) A solar cell with 1cm^2 active area.

Table 2. Summary of SOC Solar Cell Performance

Substrate	No. of Diodes	Avg. Area cm ²	ρ Ohm- cm	ρ_s Ohms / $\square$	Avg. V_{oc} Volts	Avg. J_{sc} ma/cm ²	Avg. FF	Avg. η %	Max. η %
R78A-33*	8	0.02	2.3	10	0.45	15	0.69	4.6	5.9
R78D-42*	5	0.03	2.3	21	0.46	20	0.65	6.1	6.5
R107D-47	9	0.07	5.0	--	0.48	18	0.59	5.1	6.25
R103J-46*	4	0.01	--	17	0.45	14	0.68	4.3	4.9
R103A-45*	5	0.05	--	--	0.45	14	0.66	4.3	4.5
R107C-50	6	0.07	5.0	23	0.50	21	0.67	7.0	7.5
R107A-51**	9	0.05	5.0	18	0.49	20	0.69	6.9	7.8
R172D-59	1	1.0	1.4	53	0.51	21	0.68	7.2	7.2
R169A-61	1	1.0	--	--	0.50	20	0.68	6.9	6.9
Single-Crystal Comparison Cells									
CF50-4	6	0.07	--	23	0.55	25	0.73	10.0	10.7
SC61a-b	1	1.0	5.7	--	0.54	23	0.68	8.6	8.6

-- Not Measured

* Vitreous Carbon

** "Gettered" Substrate

Note: 1) All cells have no Oxide or AR Coating

2) The areas, current densities and efficiencies refer to the active area of the device

Figure 9. IV characteristics of an SOC solar cell

Figure 10. IV characteristics of an SOC solar cell.

We consider these first results for 1 cm^2 cells to be highly significant for the following reasons:

- A number of small photodiodes made from the same substrates show nearly the same results. They have not been fully evaluated, however, and therefore were not included.
- The performance of the SOC cells is almost as good as that of the single-crystal comparison cells (Figure 11): the V_{oc} and J_{sc} values were within 9 percent of the single-crystal values. Thus some improvement might result from improved processing. In particular, we expect to change from using a P_2O_5 source to a phosphene source during the next quarter.
- Substrate MR172, which shows the 7.2 percent efficiency, was the seventh substrate dipped in the series. Thus, of all the substrates shown in Table 2, it was grown from silicon exposed to the most impurities from the mullite.
- After correcting for reflectivity losses (assumed to be 35 percent) and series resistance, the calculated inherent efficiency of both cells was 12 percent, compared to 15 percent for the single crystal.
- If one allows a reasonable value for series resistance, AR coating, and electrode area, the efficiency of these cells would have been about 10 percent.
- These samples were among the first to be processed into diodes since the dip coating facility had been put back into operation after being contaminated. The results demonstrate the system is fully operational.

We are therefore very encouraged by these results and believe that they demonstrate that the SOC process can produce solar cell quality material. Of course, other significant hurdles remain: production of high quality material at fast growth rates and demonstration of a suitable base contact method.

SUBSTRATE CHARACTERIZATION (B. G. Koepke, R. B. Maciolek, S. J. Marquardt, and M. Smeltzly)

Characterization

During the past quarter activities in this area have been limited to the determination of the microstructures and densities of a number of McDanel MV-20 rolled, dried, and fired mullite substrates dipped in previous runs. To date, data have been taken on 55

Figure 11. IV characteristics of a single-crystal comparison cell.

substrates with numbers in the range MR1 to MR35 and MR70 to MR105. The densities were determined at 25°C by weighing samples first in distilled water, drying at 150°C, and then weighing in air. The densities ranged from 2.43 to 2.54 with an average of about 2.50 gm/cm³. Optical micrographs have been taken of the microstructures of 20 of the substrates. These were all similar and closely resembled the micrograph included in the last quarterly report. No noticeable differences in the relative amounts of glass matrix, mullite crystallites or porosity were noted. On the basis of these comparisons (which are continuing) we conclude that, from a microstructural standpoint, the McDanel substrates are quite uniform in character. During the past quarter we did not continue efforts to confirm that the etch pits observed on polished and etched cross sections of silicon were associated with dislocations, but we anticipate some activity in the area in the next quarter.

Following discussions with JPL it was mutually decided not to conduct thermal shock resistance tests on mullite substrates. The dipping operation itself is considered a satisfactory test.

Efforts to measure the adhesion of the silicon layer to the mullite substrate using fracture mechanics techniques were not carried out during the past quarter but will be pursued during the next reporting period.

Experimental Substrate Compositions

A number of substrates with differing compositions have been ordered from the Honeywell Ceramics Center and from Coors Porcelain Co. The purpose of these experimental compositions is to better define how the microstructural constituents and properties of the substrate relate to the output of the solar cell.

Examples of some of the experimental variables that will be examined in this phase of the study are given below.

- Relative amounts of glassy and crystalline phases
- Porosity
- Purity (particularly with respect to transition metal ions)
- Glassy phase doped with B

A number of substrates will also be produced with carbon or carbon containing coatings applied during the primary processing of the substrates. Some of the techniques employed in this phase of the study will be:

- Mix graphite powder with clay and fire body in reducing atmosphere
- Roll SiC powder into surface of green mullite body and fire in reducing atmosphere
- Coat green body with suitable organic and fire in reducing atmosphere

CONTINUOUS COATING FACILITY (J. D. Heaps, C. D. Butter, L. D. Nelson, and H. A. Wolner)

Construction of the continuous coating facility is progressing on schedule. Its present state of completion is partially shown in Figure 12. Not visible in this photograph are the chain conveyor mechanisms, a water-cooled copper heat shield which will surround three individual furnaces, and cooling-water distribution manifolds, all of which are completed. The three furnaces and their associated heat shields were designed and have been constructed by Ultra Carbon Corporation of Bay City, Michigan. Two of the three high current power supplies needed have been ordered and the third one is in-house. All other miscellaneous parts, including the required quartz tubing and silicon stock, are also on order.

The facility's design was for the most part finalized during this reporting period. The facility is designed to allow a 100 cm x 10 cm graphite-coated ceramic substrate to pass (coated face down) over a silicon-filled quartz side arm of a crucible containing molten silicon (see Figure 13). The level of the molten silicon will be adjusted so that the surface of the liquid bulges up above the walls of this quartz side arm. As molten silicon is used up, it will be automatically replenished by a quartz plunger which displaces the silicon in the main crucible (see Figures 14 and 15). Initially we plan to control the position of this plunger by imaging the radiation emitted from the silicon meniscus onto a linear array of light sensitive elements. The outputs from this array will be processed as needed to perform the above function. Should this method of controlling liquid level prove unsatisfactory, an alternative plan is to utilize a small laser beam in such a way that it is interrupted by the meniscus when the level condition is satisfied.

Figure 12. Photograph showing construction status of continuous coating facility.

Figure 13. Exposed top view of continuous coating facility (Top covers are removed and upper substrate furnace and carbon felt insulation are not shown).

Figure 14. Cross-sectional view of three-zone furnace in growth chamber.

Figure 15. Top and side view of continuous coating facility.

The growth chamber of the facility is surrounded by a water-cooled copper box (see Figure 13). Three separately controlled graphite furnaces will provide temperature zones to perform the following functions:

1. Gradually heat the substrate to the coating temperature.
2. Control the temperature of the molten silicon in the main crucible and side arm.
3. Provide, as needed, the temperature profile required for desirable crystalline solidification and minimum thermal stress.

The first and second zones will be individually powered by SCR-regulated 0-30 volt, 0-1500 amp, D. C. power supplies. Their temperatures will also be individually controlled by Honeywell three-mode controllers. The third zone will be powered and temperature controlled by a Honeywell Electrodyne-controlled power supply. Each of these furnaces is surrounded by insulating blocks of graphite and carbon felt. Viewing ports will be provided for observation of the main crucible during melt-down and for viewing the silicon meniscus in contact with the substrate (see Figure 15).

The inert gas-filled enclosure which houses the growth chamber also includes fore and after compartments for handling uncoated and coated substrates. These compartments contain stainless steel chain conveyors which carry the substrates to, through, and from the growth chamber. The chain conveyors will be driven by a "Digilok" controlled variable-speed drive system which will be adjustable for growth velocities of tenths of mm/sec to many cm/sec. Given an ideally flat substrate, the fore and after chain conveyors are spaced to allow the substrate's center of gravity to carry it from one conveyor to the other. For substrates that are less than flat, spring or weight loaded rollers will assist in positioning the substrate. Until the growth parameters are established for producing acceptable crystalline silicon coatings, several substrates to be silicon coated will be loaded into the facility's fore compartment (see Figures 13 and 15) via the top opening. They will subsequently be placed on and removed from the chain conveyors using "dry box" type rubber gloves which will be installed. Once proper growth parameters have been established, the end plates on the fore and after compartments will be replaced with plates that permit substrates to pass through with a minimum of inert gas leakage.

While the facility was primarily designed to horizontally coat substrates, provision has been made for tilting the entire facility through about ± 30 degrees. With minor modifications the facility can be adapted to vertically coat substrates. Vertical coating does, however, place a more severe requirement on substrate flatness.

During this past quarter experimental attempts were made to examine the feasibility of the horizontal coating method used by the continuous coating facility. While for different reasons all experimental runs failed, insight was nevertheless gained on problems that are likely to be encountered with this coating technique. Initially, a large diameter quartz melt displacer was to be used. By doing so, sufficient molten silicon could be displaced to coat 10 or 11 substrates before melt replenishment would be needed. One of our experimental attempts at melt displacement demonstrated that a large displacer extracts enormous amounts of energy from the melt, making the surface temperature difficult to control. The physical position of a large displacer is also difficult to control since the slightest displacement causes a large change in the melt's liquid level. The diameter of the displacer will therefore be reduced to accomodate the coating of only three substrates before melt replenishment is required. Several methods for replenishing the melt are under consideration, but a final determination of the one best suited will be made after a few successful silicon coatings have been placed on the larger substrates.

ECONOMIC ANALYSIS (S. Schuldt)

The economic model for a large-scale coating facility was first described in the Quarterly Report No. 5. An estimated price of \$12.20 per square meter was reported, assuming a pulling rate of 1.0 cm/sec. The details of this estimate are presented in the accompanying computer printout (Figure 16). All amounts are in terms of 1977 dollars.

Iterations of the model under varying input conditions show that the pulling rate becomes a cost-critical factor below 0.2 cm/sec. At 0.1 cm/sec the price is \$25.37/m² (1977 dollars). The price decreases rapidly as the pulling rate increases, reaching \$17.80/m² at 0.2 cm/sec. At higher pulling rates, the price begins to level off.

Since the model was developed prior to receiving the Solar Cell Manufacturing Industry Costing Standards (SAMICS) Workbook, the methods and assumptions for the allocation of expenses do not totally conform with SAMICS standards. The procedures used, however, were identical to those used by Honeywell costing experts for comparably-sized factory operations. The basic ground rules for the model are outlined next.

Because many costs do not scale exactly with the factory size as measured by the number of production units, a separate detailed cost analysis was performed by Honeywell experts for two factories representing supposed opposite ends of the spectrum. In each case, the total annual production was assumed to be five million square meters per year, but the linear pulling rates were respectively 1.0 and 0.1 cm/sec, representing the most optimistic and most pessimistic conditions. Production units required to meet the

JUNE 14, 1977

HONEYWELL CORPORATE RESEARCH CENTER COST ANALYSIS FOR COATING
SILICON ON CERAMIC. LATEST REVISION APRIL 7, 1977.

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION
SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE
FOLLOWING INPUT DATA:

OCTUPLE COATING UNITS	100000. \$ EACH
POLY SI	10.00 \$/KGM
CERAMIC	2.00 \$/SQ M
ARGON	4.00 \$/100 CU FT
PULLING RATE	1.00 CM/SEC
SHEET WIDTH	30.00 CM
SI THICKNESS	100. MICRONS
SUBSTRATE THICKNESS	0.50 CM
ELECTRIC RATE	4.00 CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 9
COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.011	
PRODUCTION EQUIPMENT	0.066	
PLANT EQUIPMENT	0.004	0.081
DIRECT LABOR		
PRODUCTION	1.106	
PRODUCTION ENGINEERING	0.028	
INSPECTION	0.025	1.160
BURDEN OVERHEAD		1.433
DIRECT MATERIALS		
SILICON	2.912	
CERAMIC	2.500	
CARBON	0.264	
ARGON	0.392	6.069
ELECTRIC POWER		0.253
FACTORY COST (SUBTOTAL)		8.995
GEN. & ADM.		1.619
TOTAL COST		10.614
PROFIT		1.592
PRICE		12.206
ADDED VALUE		9.294

FIGURES LISTED BELOW GIVE THE PERCENT INCREASE (DECREASE)
IN PRICE AND ADDED VALUE, WHICH WOULD BE THE RESULT OF
INCREASING EACH OF THE INPUT VALUES 1% WHILE MAINTAINING
ALL THE OTHER VALUES FIXED. FIRST COLUMN GIVES THE %
CHANGE IN PRICE AND SECOND COLUMN GIVES THE % CHANGE IN
ADDED VALUE.

OCTUPLE COATING UNIT PRICE	0.003	0.004
POLY SI PRICE	0.324	0.112
CERAMIC PRICE	0.278	0.365
ARGON PRICE	0.044	0.057
PULLING RATE	-0.110	-0.145
SHEET WIDTH	-0.065	-0.086
SILICON THICKNESS	0.325	0.113
SUBSTRATE THICKNESS	0.026	0.034
ELECTRIC RATE	0.028	0.037

Figure 16. Economic analysis for growth rate of 1.0 cm/sec.

annual quota were respectively nine and 92. Detailed estimates of direct and indirect labor were itemized for each factory, as well as burden allocations, materials, and capital expenditures.

Since the economic model is supposed to be valid for any pulling rate between these extremes, a linear interpretation in terms of production units is employed. For example, let A_0 be the required factory floor area assuming a pulling rate of 1.0 cm/sec (9 machines), and A_1 the area required for 0.1 cm/sec (92 machines). The area computation for an intermediate speed r , $0.1 - r - 1.0$, proceeds as follows:

$$\text{No. of machines } M = 9.2/r$$

$$\text{Area } A = A_0 + \frac{M-9}{92-9} (A_1 - A_0)$$

The second computer printout (Figure 17) represents the slow pulling rate, with the other parameters unchanged. A comparison of the two printouts summarizes the cost analyses for the two extreme cases, where the figures have been reduced to dollars per square meter.

JUNE 14, 1977

HONEYWELL CORPORATE RESEARCH CENTER COST ANALYSIS FOR COATING
SILICON ON CERAMIC. LATEST REVISION APRIL 7, 1977.

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION
SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE
FOLLOWING INPUT DATA:

OCTUPLE COATING UNITS	100000. \$ EACH
POLY SI	10.00 \$/KGM
CERAMIC	2.00 \$/SQ M
ARGON	4.00 \$/100 CU FT
PULLING RATE	0.10 CM/SEC
SHEET WIDTH	30.00 CM
SI THICKNESS	100. MICRONS
SUBSTRATE THICKNESS	0.50 CM
ELECTRIC RATE	4.00 CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 92
COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.066	
PRODUCTION EQUIPMENT	0.350	
PLANT EQUIPMENT	0.034	0.451
DIRECT LABOR		
PRODUCTION	3.042	
PRODUCTION ENGINEERING	0.061	
INSPECTION	0.053	3.155
BURDEN OVERHEAD		5.138
DIRECT MATERIALS		
SILICON	2.912	
CERAMIC	2.500	
CARBON	0.264	
ARGON	3.924	9.600
ELECTRIC POWER	0.353	
FACTORY COST (SUBTOTAL)	18.698	
GEN. & ADM.	3.366	
TOTAL COST	22.063	
PROFIT	3.309	
PRICE	25.373	
ADDED VALUE	22.460	

FIGURES LISTED BELOW GIVE THE PERCENT INCREASE (DECREASE)
IN PRICE AND ADDED VALUE, WHICH WOULD BE THE RESULT OF
INCREASING EACH OF THE INPUT VALUES 1% WHILE MAINTAINING
ALL THE OTHER VALUES FIXED. FIRST COLUMN GIVES THE %
CHANGE IN PRICE AND SECOND COLUMN GIVES THE % CHANGE IN
ADDED VALUE.

OCTUPLE COATING UNIT PRICE	0.015	0.017
POLY SI PRICE	0.156	0.046
CERAMIC PRICE	0.134	0.151
ARGON PRICE	0.210	0.237
PULLING RATE	-0.623	-0.704
SHEET WIDTH	-0.407	-0.460
SILICON THICKNESS	0.156	0.047
SUBSTRATE THICKNESS	0.012	0.014
ELECTRIC RATE	0.019	0.021

Figure 17. Economic analysis for growth rate of 0.1 cm/sec.

CONCLUSIONS

From the past quarter's research activities the following can be concluded:

- The SOC process is capable of producing solar cell quality sheet silicon.
- Even a significant amount of exposure of the melt to mullite can lead to solar cells with J_{sc} and V_{oc} within 9 percent of those obtained in single-crystal comparison cells.
- Single-crystal seeding experiments show promise for promoting improved grain growth.
- Dylon Industries carbon coatings can produce good silicon coating, but are not suitable because of their high 1 to 2 percent impurity content.
- "Dag" dispersion no. 154 looks very promising as a carbon coating material. It is quite pure and can be applied by a swab or airbrush.
- To date, chemical analysis techniques have not revealed any impurity segregation at grain boundaries.
- SiC has been identified at the silicon-vitreous carbon interface using scanning Auger microscopy.
- Surface inversion is not a serious problem in EBIC measurements on p-type silicon if the surface is free of oxide.
- A scanning light beam (LBIC) can be used to identify regions of low minority carrier diffusion length and poor cell efficiency.
- Photodiode short circuit current decay (PSCCD) is not a simple method of measuring minority carrier lifetime.
- The least reliable process in our present fabrication procedure is the diffusion using P_2O_5 . We plan to change to a PH_3 process.
- No noticeable differences in porosity or relative amounts of glassy and crystalline phases have been found in the mullite substrates examined to date.
- Our economic analysis stresses the fact that the pulling rates should be greater than 0.3 cm/sec.

RECOMMENDATIONS

It is recommended that the use of boron-doped vitreous carbon coatings be pursued. The vitreous carbon would prevent dissolution so that the melt does not become excessively boron-doped. However, the boron doping would promote ohmic contact between the silicon and the silicon carbide. Tylan Corp. has given us a quotation for experiments to demonstrate feasibility.

NEW TECHNOLOGY

There have been no reportable "New Technology" items uncovered during this reporting period.

PROJECTED ACTIVITIES FOR NEXT QUARTER

In the dip coating experiments planned for the next quarter, additional SOC seeding experiments will be tried using properly oriented ribbon-type seeds. Considerable emphasis will also be placed on measuring and controlling the temperature gradient above the melt in an effort to achieve acceptable crystalline coatings at faster growth rates. Tests will be made measuring the adhesion of the silicon to the substrate and residual stresses in the silicon coatings will be measured using X-ray techniques.

Substrate characterizations will continue on all incoming substrates from Honeywell's Ceramics Center and Coors Porcelain Co. Numerous types of substrates are expected to arrive during the coming quarter.

In the area of solar cell fabrication and evaluation, large area (10cm^2) solar cells will be made on SOC coatings which have slotted substrates. Such cells will improve the active-to-total-area ratio and demonstrate the technical feasibility of electrically contacting the base layer via the silicon-filled substrate slots. Emphasis will continue on fabricating several additional 1cm^2 - and 10cm^2 - area solar cells using PH_3 rather than P_2O_5 as a diffusant. The potentials of boron-doped carbon coatings will be explored in an effort to minimize back contact series resistance. LBIC and other techniques for measuring the minority carrier diffusion length of the base region will continue.

The back contact modeling study will begin and will include: (1) comparing the distributed resistance with lumped series resistance; (2) calculating the resistance-lowering effect of vitreous carbon substrate coatings; and (3) calculating the exact contact resistance.

Also, during the next quarter it is anticipated that the continuous coating facility will be completed and made operational and a Standard Operation Procedure Manual will be prepared and presented to JPL.

Lastly, the economic evaluation computer program will be exercised as required.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 18, 19, and 20.

Figure 18. Updated program plan

Figure 19. Updated program labor summary

Figure 20. Updated program cost summary

APPENDIX A DIP COATED SAMPLE LIST

This appendix contains a list of the samples that were dip coated during this quarter, along with a summary of the coating parameters for each sample.

Sample	Temp°C/ Thermocouple mV (Pt + 13% Rh)	Soak (sec)	Withdraw (cm/sec)	Carbon
MR133	(a)	30	0.04	Ultra carbon
MR134	16.60mV	30	0.04	Ultra carbon
MR135	16.49	30	0.04	Ultra carbon
MR136	16.35	30	0.04	Ultra carbon
MR137		Substrate broke		
MR138	16.35	45	(b)	Ultra carbon
MR139	16.37	30	0.04	Ultra carbon
MR140	16.32	20	0.04	Ultra carbon
MR141	16.29	20	0.04	Ultra carbon
MR142	16.29	20	0.04	Ultra carbon
MR143	16.29	20	0.04	Dylon AE
MR144		Pull rod broke		
MR145	16.22	30	0.04	Ultra carbon
MR146	16.22	30	0.04	Ultra carbon
MR147	16.22	30	0.04	Dylon AE
MR148	16.18	30	0.04	Ultra carbon
MR149	16.13	30	0.04	Ultra carbon
MR150	16.13	30	0.02	Ultra carbon
MR151	16.13	30	0.02	Ultra carbon
MR152	16.08	20	0.1	Ultra carbon
MR153	16.08	20	0.04	Ultra carbon
MR154	16.08	20	0.04	Dylon AG
MR155	16.08	20	0.04	Dylon AG
MR156	16.08	20	0.04	Dylon SA
MR157	16.08	20	0.04	Dylon DS
MR158	16.06	20	0.04	Dylon DS
MR159		Froze into melt		
MR160	(c)	20	0.04	Ultra carbon
MR161	(c)	20	0.04	Ultra carbon
MR162	(c)	20	0.04	Ultra carbon
MR163	(c)	20	0.04	Dylon AG
MR164	(c)	20	0.04	Ultra carbon
MR165		Froze into melt		
58-1M6H	1432°C	20	0.03	Ultra carbon
58-2M6H	1432	20	0.03	Ultra carbon
58-3M6H	1432	20	0.03	Ultra carbon

Sample	Temp°C/ Thermocouple mV (Pt + 13% Rh)	Soak (sec)	Withdraw (cm/ sec)	Carbon
58-4M6H	1432°C	20	0.03	Ultra carbon
58-5M6H	1432	20	0.03	Ultra carbon
58-6M6H	1432	20	0.03	Ultra carbon
58-7M6H	1432	20	0.03	Ultra carbon
58-8M6H	1432	20	0.03	Ultra carbon
58-9M6D	1432	20	0.03	Dylon SA
58-10M6H	1432	20	0.03	Ultra carbon
59-1MT	1432	20	0.02	Tylan
59-2M6H	1432	20	0.02	Ultra carbon
59-3M6H	1432	20	0.02	Ultra carbon
59-4CH	1432	20	0.02	Ultra carbon
59-5M6H	1432	20	0.02	Ultra carbon
59-6CH	1432	20	0.02	Ultra carbon
59-7M6H	1432	20	0.02	Ultra carbon
59-8M6H	1432	20	0.02	Ultra carbon
59-9M6H	1432	20	0.02	Ultra carbon
59-10M6H	1432	20	0.02	Ultra carbon
61-1MT	1438	120	0.03	Tylan
61-2MT	1438	30	0.02	Tylan
61-3M6H	1438	20	0.02	Ultra carbon
61-4M6X	1438	20	0.05	dag # 154
61-5M6X	1438	20	0.03	dag # 154
61-6M6D	1438	20	0.05	Dylon SA
61-7M6D	1438	60	0.05	Dylon SA
61-8M6D	1438	20	0.10	Dylon SA
61-9M6D	1438	20	0.10	Dylon SA
61-10M6D	1438	20	0.03	Dylon SE
63-1M7H	15.00 mV	30	0.04	Ultra carbon
63-2M7H	15.00	30	0.03	Ultra carbon
63-3M7D	15.00	30	0.03	Dylon DS
63-4M7D	15.00	20	0.05	Dylon AG
63-5M6D	15.00	15	0.05	Dylon AE
63-6M6D	14.90	15	0.10	Dylon AE
63-7M7X	14.90	15	0.10	Grafoil
63-8M6D	14.90	30	0.02	Dylon DS

Sample	Temp°C/ Thermocouple mV (Pt + 13% Rh)	Soak (sec)	Withdraw (cm/sec)	Carbon
63-9M6D	14.90mV	30	0.03	Dylon AG
63-10M6D	14.90	30	0.03	Dylon DS
63-11M6D	14.90	30	0.03	Dylon AE
65-1M7H	1430°C	(d)	0.02	Ultra carbon
65-2M7H	1442	30	0.03	Ultra carbon
65-3M7H	1442	30	0.03	Ultra carbon
65-4M7H	1442	30	0.03	Ultra carbon
65-5M7H	1442	30	0.02	Ultra carbon
65-6M7H	1442	30	0.03	Ultra carbon
65-7M7X	1442	60	0.02	dag # 154
66-1M7X	1455	30	0.03	dag # 154
66-2M7X	1440	30	0.03	dag # 154
66-3M7X	1434	30	0.03	dag # 154
66-4M7X	1434	30	0.03	dag # 154
66-5M7H	1430	30	0.03	Hand-rubbed
66-6M7X	Substrate broke			dag # 154
66-7M7X	Substrate broke			dag # 154
67-1M7S	Substrate broke			Propane
67-2M7S	1475	20	0.02	Propane
67-3M7S	1475	20	0.02	Propane
67-4M7S	1475	10	0.02	Propane

- (a) Temperature controller failed
- (b) Pull mechanism failure
- (c) Thermocouple sheath cracked, thermocouple inaccurate
- (d) Froze into melt, soak time ~ 8 min