DIGITIZING HIGH FREQUENCY SIGNALS USING SERIAL ANALOG MEMORIES*

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ABSTRACT

An online computer system has been developed as a replacement for oscilloscopes and cameras on the Tormac project. Up to 32 simultaneous waveforms are recorded at up to 2 MHz in analog shift registers, then digitized sequentially after the event into a small PDP-11 computer. Data and functions of data may be displayed or plotted locally, and then forwarded for storage at a larger, remote computer via a network arrangement. Advantages over scopes have been lower incremental cost ($\sim$ \$200/channel), less noise pickup, better resolution ($< 1\%$), and immediate presentation of data.

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Introduction

The Tormac project consists of experiments on pulsed magnetically-confined plasma devices. During an event, it is necessary to record the time evolution of signals from such diagnostics as polychrometers, laser interferometers and magnetic probes so that plasma parameters may be calculated. Since such calculations must be performed in a computer, it is advantageous to acquire the data directly in digital form. However, to maintain submicrosecond resolution on many signals is beyond a computer's bandwidth.

The only commercially available solution has been individually buffered high speed Analog to Digital Converters (ADC), such as those made by Biomation, and similar devices built into CAMAC modules.¹⁻⁶ Direct digitizing is very expensive at high speed, and so it would be economical to record data in a way which could exploit the long delay between events to digitize the data.

Such a system has recently become feasible by the development of Serial Analog Memory (SAM) integrated circuits.⁷ A SAM permits an analog signal to be recorded in an array of sampling capacitors at one clock rate, held for some brief time, and then read out at another clock rate. Presently these circuits are made by Reticon Corporation and Fairchild Semiconductor.⁸

Organization

The system for Tormac uses the Reticon SAM128V. (Fig. 1). Each SAM contains 128 sample and hold circuits and gating circuitry from common analog input and outputs. Two independent 128 stage shift

registers control the sequencing of the input gates and output buffers. The sequence is shifted at each edge of a complementary clock signal running at half the sample rate.

A complete system is assembled from 32 SAMs, a control circuit, and a single medium speed ADC (Fig. 2). When an event occurs, all 32 inputs are clocked in parallel to record the signals, after which the computer is notified. The computer then commands the control board to read and digitize the signals from each SAM in series until 128 time samples times 32 SAMs equals 4096 signals are recorded. In its present configuration, the input sampling rate is 2 Mhz, for a total input bandwidth of 64 Mhz. The readout is performed at the program loop time of 7 μ sec per sample, hence this method has reduced the necessary digital bandwidth by 500.

Two such systems have been built and installed on Tormac IV and V (Fig. 3). Each unit is contained in a heavily shielded box adjacent to the experiment. It communicates over high speed serial lines to a PDP 11/10 computer across the room. As the computer operates only after the event, it did not require additional shielding. The PDP 11 buffers the data from both experiments, after reading them at separate times via a simple mechanical switch. It displays the data on an xy scope or plotter and performs various simple analyses.

No storage peripherals are included in the system. Instead, data is forwarded via a 9600 baud phone line to a larger central PDP 11/45 to be stored on disc and tape. The tapes are then analyzed more extensively on the laboratory CDC 7600. The 11/10 to 11/45 networking arrangement has worked well in several locations at Lawrence

Berkeley Laboratory, and allows an experiment to invest in a minimum of computer equipment. A minimum of hardware also enhances reliability and permits shared software effort.

Properties of the SAM128V

SAMs are quite adequate for use in precision, quantitative instruments, however they were not intended for this purpose. As a result, they exhibit certain peculiarities which must be dealt with by a computer.

Most of these peculiarities appear as degradations in signal to noise ratio, to 30 or 40 db. One principle source is clock noise pickup caused by careless grounding or paths. The clock signals rise from -10 to +5 volts in < 30 ns, which can cause a systematic noise pattern at the clock frequency. This was partially reduced by locally buffering the clock signals on the SAM card and running the digital lines away from the high impedance analog lines. In the computer it is further reduced by base line subtraction and two-sample time filtering.

A further problem is that each SAM is physically 128 independent circuits, each with possibly different gain, offset, and nonlinearity due to chip geometry, etc. The bulk of this variation lies in offset, so that after baseline correction the ratio improves to 55 db, or the equivalent of a 9 bit digital device.

The devices have an input range of ± 4 V, however they are nonlinear near these limits. When used at a reduced range of ± 3 V, the linearity is better than 1%. The only remaining calibration is the relative gain between SAMs, and this is simple within the computer.

It was noted that this too can occasionally be avoided when SAMs are selected from a single production batch.

Information stored in a SAM degrades exponentially, approximately 5% in 40 ms, hence the computer must be able to read it quickly. The remaining degradation can be considered relative gain if the read out sequence remains the same as the calibration sequence, thus maintaining a repeatable delay.

Circuit Design

The unit contains 8 SAM boards of 4 channels each, a digital control board, an ADC board, and power supplies (Fig. 2).

Each SAM board contains CMOS digital logic to drive the clock signals and to decode the readout select. The analog output of each channel is high impedance and hence is connected by a Darlington emitter follower to a low impedance common analog bus. The analog input is diode protected, and shielded by a generous ground plane.

The ADC board (Fig. 4) contains a high speed Datel 10 bit ADC, which digitizes the voltage on the analog bus on command from the computer. It converts via successive approximation in 4 μ sec, and provides the 10 bit word serially. This, and other signals, are buffered to the computer on differential drivers and receivers over shielded twisted pairs.

The control board (Fig. 5) handles timing. It detects the event trigger, and provides a lock-out to avoid retriggering. Next, it enables a 2 MHz clock to sequence the read into the SAMs, and a start pulse. After 256 pulses (128 for reading, 128 to allow noise to settle), it stops the clock and provides a ready signal to

the computer. The computer sends a serialized address to this board to select which channel to read, and then sends 128 read commands, repeating this process for each channel. The select address is decoded into a board select (1 of 8) and chip select (1 of 4) which are then combined at the SAM board.

Readout occurs in 7 microsecond cycles, the time it takes the computer to perform a loop to store the data in an array. The analog to digital conversion, and subsequent serial transmission, requires 4 μ sec, leaving 3 μ sec for switching and line settling.

Within the computer, the interface consists of an input shifter to receive the ADC serial data, an output shifter to transmit the select address, and line buffers. These are mounted on a DEC supplied interface foundation card. Mounted on the same card are two digital-to-analog converters to drive a scope display and xy plotter (Fig. 6).

There are a total of 5 signals between the SAM box and the computer: a ready signal to tell the computer an event has been read in, a read signal from the computer to initiate an ADC cycle, a 4 MHz clock generated by the ADC, the 4 MHz ADC data shifted by that clock, and the 4 MHz serial select signal from the computer also shifted by that clock. The timing relations of these and other internal signals are shown in Figure 7.

The computer system used in our experiment is a PDP-11/10 with 16K core, a VT50 terminal, and a 9600 baud serial link to a PDP 11/45 at the bevatron. Such a system costs \$8,000, and could be accomplished for even less with a newer 11/03. If storage

peripherals were required, the cost would be much higher. The base SAM assembly is on the order of \$1,000, and each SAM chip is \$85.

Software

Data taking software for the experiment is written in a specially modified version of BASIC/PTS. The modifications consist of short assembly language routines to cycle the SAM unit, display or plot curves and labels, and transfer information over the serial link to the 11/45.^{9,10}

BASIC is an interactive high level language. It seems nearly ideal for experimental data taking as it allows the experimenter to modify programs as they run, examine data in the arrays, and re-enter programs at any point. New or modified programs may be saved and recalled.

The bevatron 11/45 is a medium scale machine for bio-medical experiments. It runs RSX-11M, a multi programming, real time operating system, to which our computer appears as a terminal. Our programs and data reside on the 11/45 disc.

Our computer is thus used in two distinct modes. In one mode our terminal interacts directly with the RSX system so that we may manipulate our files, modify the BASIC service routines, run Fortran programs there, or download BASIC into our 11/10. Once BASIC is downloaded, our computer can operate more or less independently. That is, BASIC programs can be written and run without communicating with the 11/45. However, when we wish to store data or programs onto disc, BASIC internally initiates a service task on the 11/45 to do so. This service task is written in FORTRAN, and stores our

data in FORTRAN accessible formats. BASIC calls can switch our terminal between BASIC and RSX mode without disturbing contents of memory, and in certain circumstances both modes may operate simultaneously.

An archetypal data taking program is as follows:

```
10 REM SAMPLE DATA TAKING PROGRAM
20 DIM D(1023), S(16), R(128)
30 FOR I = 0 to 16
40 S(I) = 31 - I*2\NEXT I
50 PRINT 'READY TO TAKE DATA'\INPUT A$
60 IF A$ = 'NO' THEN 50
70 CALL 'ADC' (D,S)
80 FOR I = 0 to 63
90 CALL 'UPK2' (D(I), R(I*2), R(I*2 + 1))
100 NEXT I
110 B$ = 'DATA FROM SAM #31'
120 CALL 'SCOP' (R, 128, B$)
130 ONNET\FILE 'DATA1\DA:20:200'
140 FOR I = 1 to 16
150 OUTREC (I, 128, D((I - 1)*64))
160 NEXT I
170 OFFNET\STOP
```

This program reads every other SAM channel in reverse order, displays the wave form of the first one read on the xy scope with a label, then stores all the data on a disc file.

Numbers in BASIC are 32 bit reals, and arrays are indexed from zero. We pack ADC data into 16 bit half words. Thus D is the data array, and can hold 16 channels times 128 cells.

S is a select array, and is a list of which channels are to be read and in what order. The service routine 'ADC' keeps reading channels pointed to by S until it hits a negative entry.

The loop 80-100 unpacks the first 64 elements of D into an array of 128 real numbers BASIC can operate on. R then is an array of voltage measurements recorded by SAM channel 31.

B\$ is a character string label which appears on the oscilloscope with a plot of R when 'SCOP' is called.

The section 140-170 communicates our data to an 11/45 file named DATA1:

ONNET initiates the service task.

FILE specifies the octal number and size of file records.

OUTREC transmits data to each record.

OFFNET terminates the service task.

After many files of data accumulate at the 11/45, they are spooled onto mag tape and analyzed at the 7600. Disc files may also be read back into BASIC programs and analyzed locally, or accessed at the bevatron by FORTRAN programs.

Expansion

There is essentially no limit to the number of SAMs which could be joined; our choice of 32 was arbitrary. The operating frequency of 2 MHz could be increased slightly, however the SAM128 limit of

5 MHz can not be reached by CMOS control circuitry.

Newer SAM chips have been developed with longer retention, more samples, or higher speeds. Some of these are 'bucket brigade' types where the sampled change itself physically propagates through the channels. Such devices have the advantage that each time sample has seen the same electronics, reducing 'pattern noise'.

Any new implementation of this scheme should consider building the circuitry into computer accessible CAMAC modules. This would make it easier to include SAMs with other types of pre-existing hardware and software, however it might make shielding more difficult.

Conclusion

Serial analog memories may be readily adapted to computerized handling of transient data. Their peculiarities may be compensated for by the computer. They offer advantages of convenience, low cost, and high resolution over oscilloscope/camera banks, and are much less expensive than direct digitizing techniques.

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Figure 1. Internal Organization of SAM128V

Figure 2. SAM System Organization

Figure 3. Laboratory Implementation

Figure 4. Analog to Digital Converter and Line Drivers

Figure 6. Interface to PDP-11 Using M1710 Unibus Foundation Module

FOUNDATION MODULE CIRCUITRY

Figure 7. Read Out Cycle Timing

Figure 8. Component Side of Boards