ORELA Data Acquisition System Hardware

Vol. 3: Scaler Interfaces
(Q-5036-1, -2, -4 through -11, -29, and -30)

J. W. Reynolds

OAK RIDGE NATIONAL LABORATORY

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INSTRUMENTATION AND CONTROLS DIVISION

ORELA DATA ACQUISITION SYSTEM HARDWARE

Vol. 3: Scaler Interfaces
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ORNL/TM-5638	Introduction
ORNL/TM-5639 (Vol. 2 of ORNL/TM 5638)	Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)
ORNL/TM-5641 (Vol. 4 of ORNL/TM-5638)	ORELA Device Controllers (Q-5098)
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ORNL/TM-5645 (Vol. 8 of ORNL/TM-5638)	Instruction Manual for the Ground Isolation Driver and Receiver Cards on the Quiet Ground System at ORELA

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ABSTRACT

This report describes programming, word formats, control signals, voltage levels, connector layouts, ground isolation, and a theory of operation with simplified logic diagrams for the Scaler Interface on the SEL 810B data acquisition computers at ORELA.

1. INTRODUCTION

The Scaler Interface¹ is the part of the data collection equipment on the Data Acquisition System² at Oak Ridge Electron Linear Accelerator (ORELA) that provides for external control through pulse and address generation and read-in of information from scalers and other devices. There are two read-in paths in the interface — the 16-bit Scaler Input Bus and the 32-bit program-controlled input called Scaler Word 1 and 2.

The reader is assumed to have a knowledge of electronics, digital control logic, and machine language programming³ for the SEL 810B computer. Further details can be obtained from ORNL Instrumentation and Controls Division Drawing Series Q-5036 as listed in Table 1 and Systems Engineering Laboratories, Inc. (SEL) *Technical Manual, Data Acquisition System*, vol. 1, Publication No. 315-219100-000, pp. 3-1 through 3-7. Note that the SEL TM does not contain control revisions for either the Scaler Input Bus or Scaler Word 1 and 2. The SEL sheet numbers above sheet 4 correspond to the Drawing Series Q-5036 dash numbers. Below sheet 4 they correspond to the next lower digit.

The Scaler Interface is located in the Data Collection Equipment (DCE) Cabinet for each Data Acquisition Computer (DAC). See Dwg. No. Q-2928-2* for a floor plan of the equipment.

1.1 Scaler Input Bus

The Scaler Input Bus is a 16-bit parallel input with bit 0 as the most significant bit. The bus is controlled by the Scaler Ready interrupt and a CEU pulse instruction to enable the transfer of the input bus data into the computer by an AIP or MIP instruction. Address generation is not required. The Scaler Input Bus on one DAC has been reserved for data from the Pulse Shape Analyzer located at the ORELA control panel.

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* See Sect. 6, Engineering Drawings, for a list of Q-drawings pertinent to the topics discussed in this volume. These drawings are available from the author.

Table 1. SEL 810B Scaler Interface drawing list

ORNL Drawing Series Q-5036
 SEL Dwg. Series 53320 with revisions
 Logic Diagram, unit 1R2

Number	Subtitle
-1	Decode Unit 22
-2	I/O Sync Logic
-4	Scaler Interrupt Control
-5	Scaler Address Control
-6	Scaler Input Data Register, Word #1, Part #1 (bits 0-7)
-7	Scaler Input Data Register, Word #1, Part #2 (bits 8-15)
-8	Scaler Input Data Register, Word #2, Part #1 (bits 0-7)
-9	Scaler Input Data Register, Word #2, Part #2 (bits 8-15)
-10	Scaler Pulse Output, Part 1 (Pulse 1 to 6)
-11	Scaler Pulse Output, Part 2 (Pulse 7 to 12)
-21	I/O Bus Bits 0-3
-22	I/O Bus Bits 4-7
-23	I/O Bus Bits 8-11
-24	I/O Bus Bits 12-15
	SEL 810B Multiplexer-Scaler Isolation
-29	Assembly, Four-Wide Nuclear Instrument Module for DEC A, K, R & M Series Logic Cards
	SEL 810B Scaler Isolation
-30	Master Receivers and Drivers
-31	Master Receivers and Drivers Panels

1.2 Program-Controlled Input

The program-controlled input consisting of Scaler Word 1 and 2 (16 bits each) uses bit 0 of Scaler Word 1 as the most significant bit in a device that requires a maximum of 32 bits. Bit 15 of Scaler Word 2 is the least significant bit. Either word can be transferred under

program control to the computer without the other word, or Word 2 can be transferred before Word 1. The program-controlled input is used with a Device Controller⁴ for monitoring such things as beam stop, vacuum valve, and filter or sample changer positions; for reading scalers and other devices associated with an experiment; and for controlling the filter and sample changers via address and pulse generation. The program-controlled input requires the execution of a program that uses both the address and pulse generation features of the interface. The five address bits select an experimenter (two bits) and one of the devices or scalers (three bits) connected to the interface. The selected device is then controlled by using the pulses to perform a specific control function that has been designed into the Device Controller; for instance, in scaler control these pulses are used to clear, start, and stop the scalers, and the count read in from a scaler may be used as a monitor count to indicate when a sample changer should operate.

1.3 Addressing

The two address bits that select an experimenter route a group signal to a fixed location in one of four cables connected to the ground isolation module attached to the Scaler Interface. The remaining three address bits are then decoded for a specific use in the attached Device Controller. See Dwg. No. Q-2928-5 for the cabling.

1.4 Pulses

The twelve output pulses used for control are generated in the Scaler Interface and routed to all four cables attached to the ground isolation module. The pulses will be present on all cables whenever any program generates them; therefore, it is absolutely essential that all equipment designed to use these pulses use the group signal in the cable as an enable before the pulses are used for a specific control function.

2. PROGRAMMING

The Scaler Interface unit number is '22. An address is set in the Scaler Interface by execution of a CEU instruction with a FORMAT 0 second word while a pulse is generated with a FORMAT 1 second word. The CEU second word formats are given in Fig. 1. Note that pulse selection is by a unitary code to allow simultaneous generation of all pulses or any combination of them. An address mode instruction will force a delay of 3 μ sec, whereas the pulse mode instructions will force a delay that is equivalent to the length of the pulse (a maximum of 2 μ sec as presently adjusted) (see Scaler Pulses, Sect. 3.1) before the Scaler Interface will execute another command.

An illustration of the sequence of instructions required to read 32 bits from a scaler through a Device Controller is given in Fig. 2. The program as listed will not run. It requires a value of X (0 to 3) in the GRPX location and the same value of X with a value of Y (0 to 7) in the SUBY location. To read 32 bits of data from a device, it is necessary only to change the location MODE to '104200, which will then select the device mode in a Device Controller. The Scaler and Device Modes of the Device Controllers define an eight-input bus, with gating that is internal to the equipment attached or that is in the Device Controller.

3. SIGNALS

The signal levels to and from the Scaler Interface are +3 V for the true condition and 0 V for the false condition. The input and output circuits to and from the Scaler Interface are shown in Figs. 3a and 3b respectively. These circuits are connected to ground isolating⁵ receivers and drivers (Dwg. Nos. Q-5072-9C and -11A) for the program-controlled input on cable assembly.

A typical ground isolated connection between the Scaler Interface and an experimenter for each direction of transfer is given in Fig. 4.

ORNL-DWG 76-15915

FORMAT 0, Address Mode

FORMAT 1, Pulse Mode

Fig. 1. Scaler Interface, CEU second word formats.

ORNL-DWG 76-15916

TO READ 32 BITS FROM A SCALER

REL		
ORG	0	
SYST	NOP	
ME	NOP	
	CEU '22	SELECT SUBADDRESS 0 ON
GRPX	DATA 'X0	CHANNEL X. WHERE X IS
	BRU *-2	0, 1, 2, OR 3
	CEU '22	GENERATE PULSE X002 TO
MODE	DATA '102200	SET DEVICE CONTROLLER IN
	BRU *-2	SCALER MODE
	CEU '22	SELECT SCALER ADDRESS
SUBY	DATA 'XY	Y ON CHANNEL X
	BRU *-2	
	CEU '22	GENERATE LOAD WORD 1 PULSE
	DATA '110000	
	BRU *-2	
	AIP '22	
	BRU *-1	
	STA SMSB	SCALER MOST SIGNIFICANT BITS
	CEU '22	GENERATE LOAD WORD 2 PULSE
	DATA '120000	
	BRU *-2	
	AIP '22	
	BRU *-1	
	STA SLSB	SCALER LEAST SIGNIFICANT BITS
*	BRU ME	YOUR PROGRAM HERE
SMSB	ZZZ **	DMSB WITH MODE = '104200
SLSB	ZZZ **	DLSB WITH MODE = '104200
	END	

Fig. 2. Instruction Sequence to read 32 bits from
a scaler or a device.

INPUT SIGNALS

DATA READY
 SYSTEM TAG, BIT 2
 FIRST WORD, BIT 3 TO 15
 SECOND WORD, BIT 0 TO 15

OUTPUT SIGNALS

DATA ACCEPTED
 CHANNEL BUSY
 MPXR CONTROL

Fig. 3. Scaler Interface circuits: (a) input, (b) output.

∞

Fig. 4. Double isolation for signals (a) to and (b) from the Scaler Interface.

Note that fan-out and fan-in for the various experimenters are part of the isolation system. The receiver and driver circuit cards (Dwg. Nos. Q-5072-9C and -11A) use a Model 1513 Iso-switch rated at $10^{10} \Omega$ resistive isolation. Other parameters for these Iso-switches are contained in Data Sheets 869 and 870. See Iso-switch Data Sheet Z-1341A and Z-1346A for ISC 142-1 and ISC 142-2 used at the Device Controller (Dwg. No. Q-5098) or Isolated Pulse Generator (Dwg. No. Q-5109).

3.1 Program-Controlled Input Connector

Pin assignments for the connections to the program-controlled input of the Scaler Interface are given in Tables 2 and 3. Table 2 gives the pin assignments for signals between the Scaler Interface and the computer side of the Scaler Interface Ground Isolation (Dwg. No. Q-5036-30), and Table 3 gives the pin assignments for the signals between the experimenter side of the Scaler Interface Isolation and the Device Controllers. Note that the only differences between Tables 2 and 3 are in the group signals at pins 304, 305, 306, and 307. The cable distance between the Scaler Ground Isolation and the experimenter's Device Controllers is 60 to 150 ft. The function of each of the signals for the program-controlled input in Tables 2 and 3 is described below.

Scaler Words 1 and 2 are 16-bit parallel inputs that are gated into buffer registers by the program-generated control signals, Load Word 1 and Load Word 2. Each word is transferred from the Scaler Interface buffer register into the computer by execution of either an AIP or MIP '22 instruction. Data are gated to the Scaler Word Input Bus through the Device Controller by an address from the Scaler Interface.

Group 0, 1, 2, and 3 are the decoded outputs (Fig. 5) of the two most significant bits of the address mode (Fig. 1) CEU '22 instruction. The group selection is made by the cable connection. It does not define a priority of service by ODAR;⁶ however, ODAR requires that the group number is the same as the multiplexer channel number. Each of the four cables (J5, J6, J7, and J8) has its own group signal (GROUP 0, 1, 2, and 3 respectively); hence, they define a subset of scaler addresses (00_8 through 07_8 , 10_8 through 17_8 , 20_8 through 27_8 , and 30_8 through 37_8) that can be used by an experimenter.

Table 2. Pin assignments for the Scaler Interface (P3)
to and from the Scaler Ground Isolation (P301)

Pin	GND	Function	Pin	GND	Function
101	201	Scaler Word 1, Bit 0	501	601	Scaler Word 2, Bit 0
102	202	Scaler Word 1, Bit 1	502	602	Scaler Word 2, Bit 1
103	203	Scaler Word 1, Bit 2	503	603	Scaler Word 2, Bit 2
104	204	Scaler Word 1, Bit 3	504	604	Scaler Word 2, Bit 3
105	205	Scaler Word 1, Bit 4	505	605	Scaler Word 2, Bit 4
106	206	Scaler Word 1, Bit 5	506	606	Scaler Word 2, Bit 5
107	207	Scaler Word 1, Bit 6	507	607	Scaler Word 2, Bit 6
108	208	Scaler Word 1, Bit 7	508	608	Scaler Word 2, Bit 7
109	209	Scaler Word 1, Bit 8	509	609	Scaler Word 2, Bit 8
110	210	Scaler Word 1, Bit 9	510	610	Scaler Word 2, Bit 9
111	211	Scaler Word 1, Bit 10	511	611	Scaler Word 2, Bit 10
112	212	Scaler Word 1, Bit 11	512	612	Scaler Word 2, Bit 11
113	213	Scaler Word 1, Bit 12	513	613	Scaler Word 2, Bit 12
301	401	Scaler Word 1, Bit 13	701	801	Scaler Pulse 1
302	402	Scaler Word 1, Bit 14	702	802	Scaler Pulse 2
303	403	Scaler Word 1, Bit 15	703	803	Scaler Pulse 3
304	404	Group 0	704	804	Scaler Pulse 4
305	405	Group 1	705	805	Scaler Pulse 5
306	406	Group 2	706	806	Scaler Pulse 6
307	407	Group 3	707	807	Scaler Pulse 7
308	408	Scaler Select 1	708	808	Scaler Pulse 8
309	409	Scaler Select 2	709	809	Scaler Pulse 9
310	410	Scaler Select 4	710	810	Scaler Pulse 10
311	411	Scaler Word 2, Bit 13	711	811	Scaler Pulse 11
312	412	Scaler Word 2, Bit 14	712	812	Scaler Pulse 12
313	413	Scaler Word 2, Bit 15	713	813	CABLE SHIELD

Table 3. Pin assignments for the Scaler Ground Isolation (P302)
to and from the Device Controllers (J5, J7, and J8)

Pin	GND	Function	Pin	GND	Function
101	201	Scaler Word 1, Bit 0	501	601	Scaler Word 2, Bit 0
102	202	Scaler Word 1, Bit 1	502	602	Scaler Word 2, Bit 1
103	203	Scaler Word 1, Bit 2	503	603	Scaler Word 2, Bit 2
104	204	Scaler Word 1, Bit 3	504	604	Scaler Word 2, Bit 3
105	205	Scaler Word 1, Bit 4	505	605	Scaler Word 2, Bit 4
106	206	Scaler Word 1, Bit 5	506	606	Scaler Word 2, Bit 5
107	207	Scaler Word 1, Bit 6	507	607	Scaler Word 2, Bit 6
108	208	Scaler Word 1, Bit 7	508	608	Scaler Word 2, Bit 7
109	209	Scaler Word 1, Bit 8	509	609	Scaler Word 2, Bit 8
110	210	Scaler Word 1, Bit 9	510	610	Scaler Word 2, Bit 9
111	211	Scaler Word 1, Bit 10	511	611	Scaler Word 2, Bit 10
112	212	Scaler Word 2, Bit 11	512	612	Scaler Word 2, Bit 11
113	213	Scaler Word 1, Bit 12	513	613	Scaler Word 2, Bit 12
301	401	Scaler Word 1, Bit 13	701	801	Scaler Pulse 1
302	402	Scaler Word 1, Bit 14	702	802	Scaler Pulse 2
303	403	Scaler Word 1, Bit 15	703	803	Scaler Pulse 3
304	404 ^a	Group X	704	804	Scaler Pulse 4
305	405	Group X Interrupt	705	805	Scaler Pulse 5
306	406		706	806	Scaler Pulse 6
307	407		707	807	Scaler Pulse 7
308	408	Scaler Select 1	708	808	Scaler Pulse 8
309	409	Scaler Select 2	709	809	Scaler Pulse 9
310	410	Scaler Select 4	710	810	Scaler Pulse 10
311	411	Scaler Word 2, Bit 13	711	811	Scaler Pulse 11
312	412	Scaler Word 2, Bit 14	712	812	Scaler Pulse 12
313	413	Scaler Word 2, Bit 15	713	813	CABLE SHIELD

^aGroups 0, 1, 2, and 3 are in connectors J5, J6, J7, and J8 respectively;
see Dwg. No. Q-5036-30C4.

Scaler Select 1, 2, and 4 are the three least significant bits of the CEU address mode instruction (Fig. 1). A group address, see above, is selected simultaneously with the Scaler Select bits. The three select bits are combined with the single group line which is available to each remote Device Controller to generate explicit subaddresses, 0 through 7, for use by an experimenter. (See group signal above.)

Scaler Pulses 1 through 12 are a means of generating control signals to external equipment -- for instance, to move a sample into or out of the beam. Each pulse is controlled by a bit in a CEU pulse mode instruction (Fig. 1); therefore, any one of or all the pulses may be generated with a single instruction. The twelve Scaler Pulses may be externally combined with the Scaler Select and Group levels to generate a total of 384 pulses (96 per group).

Each of the twelve basic pulses has an adjustable width; however, the width of the pulses has been set at 1 or 2 μ sec. The widths of pulses 1, 2, and 5 must remain at 2, 2, and 1 μ sec, respectively, to allow a gate-devices or a gate-scalers pulse command (see MODE in Fig. 2) from existing control programs (5GDS, 5JAH, and 5RLM)⁶ to operate three existing Device Controllers.

Group X Interrupt is a line for generating a priority interrupt in the SEL 810B computer. Its use and the function it performs is determined by experimenter requirements. Existing experiment control has not required the use of this feature; however, an application for its use is pending.

Two additional control pulses, Load Words 1 and 2, are generated internally to the Scaler Interface by a FORMAT 1 instruction (Fig. 1) to load a 16-bit Scaler Word. The Load signals are interlocked in the hardware so that only one pulse at a time may be generated. An attempt to generate both pulses will result in neither pulse being generated.

3.2 Scaler Input Bus Connector

The pin assignments for the connections to the Scaler Input Bus (P4) are given in Table 4. The function of each of the signals in the Scaler Input Bus connector is described below.

Table 4. Pin assignments, Scaler Input Bus, connector P4

Pin	GND	Function	Pin	GND	Function
101	201	Scaler Input Bit 0	301	401	Scaler Input Bit 12
102	202	Scaler Input Bit 1	302	402	Scaler Input Bit 13
103	203	Scaler Input Bit 2	303	403	Scaler Input Bit 14
104	204	Scaler Input Bit 3	304	404	Scaler Input Bit 15
105	205	Scaler Input Bit 4	305	405	Scaler Ready Interrupt
106	206	Scaler Input Bit 5	306	406	Scaler Data Accepted
107	207	Scaler Input Bit 6	307	407	Scaler Overflow Interrupt
108	208	Scaler Input Bit 7	308	408	
109	209	Scaler Input Bit 8	309	409	
110	210	Scaler Input Bit 9	310	410	
111	211	Scaler Input Bit 10	311	411	
112	212	Scaler Input Bit 11	312	412	
113		Not used	313		Paired with 113

Scaler Ready Interrupt, a pulse input to the Scaler Interface, sets a flip-flop and generates a priority interrupt to the SEL 810B computer. A second interrupt cannot be received for at least 6 μ sec because of hardware restrictions.

Scaler Input, bit 0 through 15, is a 16-bit parallel input enabled by a Scaler Ready interrupt from the equipment attached and a program-generated signal, Gate Input Bus, for each word transferred.

Scaler Data Accepted, a pulse output from the interface, occurs when an AIP or MIP '22 instruction is executed, as a result of a Scaler Ready interrupt, after executing a pulse mode instruction to generate the Gate Input Bus signal. It signals the interrupting unit that the data word on the Scaler Input Bus has been gated into the computer.

Scaler Overflow Interrupt, a pulse input to the Scaler Interface, sets a flip-flop that causes a priority interrupt to be generated to the SEL 810B computer. The response of the computer to the interrupt is determined by its associated control program. A second interrupt cannot be received for at least 6 μ sec because of hardware restrictions.

One other pulse, Gate Input Bus, for controlling the Scaler Input Bus is generated within the Scaler Interface chassis by a pulse mode instruction (Fig. 1), with a second word equal to '140000. Data will not be transferred with an AIP or MIP instruction unless this pulse is generated prior to the input data transfer instruction.

4. OPERATION

The Scaler Interface can be logically divided into six parts: (1) I/O decoding,⁷ (2) I/O synchronization,⁷ (3) program-controlled generation of an address using a CEU instruction with FORMAT 0 second words, (4) program-controlled generation of pulses using a CEU instruction with FORMAT 1 second words, (5) program-controlled input of 16 or 32 bits of data from a device or a scaler, and (6) transfer of 16 bits to the computer on the Scaler Input Bus. All six parts are covered in detail in the *SEL Technical Manual, Data Acquisition System*; however, changes have been made to the address generation logic, the pulse generation logic, and the control of both Scaler Words 1 and 2 and the Scaler Input Bus. The original SEL Drawing Series 53320 has been redrawn with the modifications on ORNL Drawing Series Q-5036. Brief explanations of the last four parts, using two brief logic diagrams (Figs. 5 and 6), are included in the following four sections; the first two parts are explained in the *Reference Manual*.³

4.1 Scaler Address Selection

Scaler address selection (Fig. 5) is accomplished by execution of a CEU instruction with bit 0 off (FORMAT 0, address mode). Bits 11 through 15 of the CEU second word are stored in five flip-flops. The outputs of the two most significant flip-flops, 2^4 and 2^3 , are decoded in four two-input AND gates to generate four Group (0, 1, 2, 3) or channel levels. The three least significant flip-flops are designated Scaler Select lines 1, 2, 4. The four Group levels and the three Scaler Select

Fig. 5. Scaler Interface pulse and address generation.

Fig. 6. Scaler Interface data input.

levels are output to the Device Controllers via the Scaler Ground Isolation (Tables 2 and 3). The detailed drawing for the address logic is Dwg. No. Q-5036-5. The group decoding is not on the original SEL drawings.

4.2 Scaler Pulse Generation

The left quarter of Fig. 5 represents the logic for pulse generation. The logic for a single pulse is shown with Z representing the specific bit required to generate a pulse (see Pulse Mode in Fig. 1). The bits of the second word when bit 0 is on (FORMAT 1, Pulse Mode) are individually strobed through AND gates to trigger twelve one-shots in any combination. The width of these pulses are adjustable in four ranges from 0.3 μ sec to 6.0 μ sec. At present, pulses 1 and 2 are adjusted for 2 μ sec, whereas the others are adjusted for 1 μ sec (see Scaler Pulses in Sect. 3.2). Care should be exercised before the width of a pulse is changed. The twelve output pulses can be output in parallel for use as a 12-bit control word. The Ready signal returned to the I/O synchronization logic prevents execution of another CEU while a long pulse, greater than the CEU execution time of 3 μ sec is in progress. The detailed logic drawings are Dwg. Nos. Q-5036-10 and -11. The Load Word 1 and 2 and Gate Input Bus pulses have been added to the original SEL logic. The output pulses have been routed to twisted pairs (originally on coax connectors) in the 51-pair scaler cable (See Tables 2 and 3 for pin assignments and Dwg. No. Q-2928-11 for color coding and assembly details).

4.3 Scaler Input Bus Data Transfers

The Scaler Input Bus on the left of Fig. 6 is controlled by the Scaler Ready interrupt and a signal (Gate Input Bus) from the computer program. The Ready interrupt sets a flip-flop, which in turn generates the priority interrupt to the computer. The computer program that is executed as a result of the interrupt generates a Gate Input Bus pulse by use of a CEU instruction with the second word equal to '140000. The

Gate Input Bus signal sets the Interrupt Word Ready flip-flop. An AIP or MIP instruction then gates the data through AND gate 4 and OR gate 3 onto the I/O Bus of the SEL 810B. At the completion of the data transfer into the 810B, a Computer Data Accepted pulse is generated; this resets the two control flip-flops, Ready interrupt and Interrupt Word Ready. Note that the zero output of the Interrupt Word Ready flip-flop inhibits the transfer of data through AND gates 1 and 2 and the reset of the Word 1 and 2 Ready flip-flops. The detailed logic for the Scaler Input Bus data transfers is on Dwg. No. Q-5036-4. Changes from the original logic were made to the bus gating control and to the resets of both the Scaler Ready interrupt and Interrupt Word Ready flip-flops. Table 4 contains the pin assignments for the Scaler Input Bus (P4).

4.4 Scaler Word 1 and 2 Data Transfers

The 32-bit program-controlled input is transferred to the computer as two 16-bit words. Each 16-bit word (Scaler Word 1 or 2 on the right half of Fig. 6) is jam transferred into a buffer register by a CEU instruction with a FORMAT 1 second word equal to '110000 (Load Word 1) or '120000 (Load Word 2). The Load Word pulse also sets its corresponding Word Ready flip-flops while the hardware prevents simultaneous generation of Load Words 1 and 2. When an AIP or MIP instruction is executed, the word in the buffer register is then gated through AND gates 1 or 2 and OR gate 3 to the I/O Bus of the computer. Completion of the input instruction at the SEL 810B generates a Computer Data Accepted (CDA) pulse, which then resets the Word Ready flip-flop to complete the read-in. Note that the signal Interrupt Word Ready will inhibit the CDA pulse from resetting Word 1 and 2 Ready flip-flops. See Fig. 2 for the instruction sequence.

The OR gates at the top of Fig. 6 labeled GND ISU are a wired OR (a cable pair, Fig. 4) in the Scaler Ground Isolation (Dwg. No. Q-5036-30). Pin assignments for the cable forming the wired OR are listed in Table 3. The detailed logic for Scaler Word 1 and 2 Input is on Dwg. Nos. Q 5036-6, -7, -8, and -9. Changes from the original logic were made to the control for the buffer register output gates and to the buffer register strobe signal.

5. MAINTENANCE

A test program, 8SCL entry 6, is available to test address selection (Group No., Device No.) and pulse generation by using the control switches to select pulses. Figure 7 gives the instructions for this program. Entries 3 and 4 display 32 bits of data in the A and B registers. Other functions in three existing Device Controllers* can be tested by using the other entries of 8SCL. It is recommended that 8SCL operate with exclusive use of the SEL 810B for the display of scalers or devices (Entries 3 and 4) and with exclusive use of the Scaler Interface for address selection and pulse generation (Entry 6).

Another test program, 8TSC, uses the Multiplexer-Scaler Tester⁸ to provide any one of five selected data patterns for checking data flow through the Device Controllers and Scaler Interfaces.

The programs are available from the author.

6. ENGINEERING DRAWINGS

The following Q-drawings are related to the topics discussed in this volume. They are not included here due to space limitations, but are available from the author.

- Q-2928-2 - ORELA Data Acquisition, Bldg. 6010, Central Data Area, Computer Equipment Layout
- Q-2928-11 - ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors
- Q-5036 - (see Table 1)
- Q-5072-9C - Ground Isolating Receiver, Dual Isolator 0 to +3 Out
- Q-5072-11A - Ground Isolating Driver, Double Isolator 0 to +3 Input
- ISC 142-1 - Isolated Digital Line Driver/Coupler/Level Shift Card
- ISC 142-2 - Isolated Digital Line Receiver/Coupler/Level Shift Card

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* Dwg. Nos. Q-5098-10 to -19 for 7JAI, -20 to -29 for 7RLM, -30 to -39 for 7 GDS.

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*8SCL [136,1000] SCALER INTERFACE AND J.W. REYNOLDS BLDG 6010
* 5-23-73 DEVICE CONTROLLER TEST
* SET SNS 15 TO RETURN TO THE SYSTEM, EXCEPT ENTRY 6 USE SNS 1.
*** NOTES
* GROUP NO. = X IN LISTING, IT IS THE MULTIPLEXER CHANNEL NO.
* DECIMAL 40 IS APPROXIMATELY 1 SECOND OF "TIME".
*** ENTRY PARAMETER FUNCTION
* 0. GROUP NO., 2, -TIME (X 25MS) RUN HOT SAMPLE CONTINUOUS
* A SELECTED TIME PERIOD, FORWARD THEN REVERSE.
* 1. GROUP NO., 2, -TIME (X 25MS) RUN HOT SAMPLE STEP FOR
* A SELECTED TIME PERIOD, FORWARD THEN REVERSE.
* 2. GROUP NO., 2, -40 ( 1 SECOND ) MOVE PADDLES, FILTERS, OR
* BEAM STOP AND DISPLAY BY SETTING THE CONTROL SWITCHES,
* JAH BEAM STOP OUT, SET CONTROL SWITCH 0, REGISTER 2, BIT 2.
* JAH-RLM FILTERS ARE SET BY CONTROL SWITCHES 1 THRU 10.
* GDS BEAM STOP OUT, SET CONTROL SWITCH 2, REGISTER 1, BIT 2.
* GDS LINEAR FILTERS SET BY CONTROL SWITCHES 3 THRU 12.
* 3. GROUP NO., SCALER NO., -TIME SCALER DISPLAY
* 4. GROUP NO., DEVICE NO., -TIME DEVICE DISPLAY
* 5. GROUP NO., TIME (MINUTES), 2 PERIODIC PRINT OF SCALERS
* SET SNS 0 TO STOP PRINTING.
* SET SNS 1 FOR NO RESET OF SCALERS
* TIME = XXX FOR MINUTES
* TIME = '10XXXX FOR 60/SEC. ('100341 = .5 MIN.)
* 6. GROUP NO., DEVICE NO., 0 CONTROL SW. PULSE PATTERN

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Fig. 7. 8SCL instructions.

REFERENCES

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