CONF - 774702

LA-UR -77-199

TITLE: SOME ELECTRICAL CHARACTERISTICS OF A DC SUPERCONDUCTING
CABLE

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SUBMITTED TO: IEEE Summer Power Meeting
July 1977
Mexico City

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SOME ELECTRICAL CHARACTERISTICS OF A DC SUPERCONDUCTING CABLE*

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ABSTRACT

A large amount of power (5 GW or more) can be transmitted through a dc superconducting power transmission line (SPTL) which has the highest power density and efficiency of any known transmission line. Although the SPTL has zero resistance to pure dc, it experiences hysteresis and resistive losses under ac and ripple. Under faults, the current may be driven out of the superconductor into the cryostabilizer which causes additional resistive losses. A well-designed SPTL should have minimum steady-state ac losses. It should also be able to recover from a transient fault quickly and reliably. The paper discusses the performance of three dc SPTL's, rated at 2.5 GW, 5 GW, and 7.5 GW, and shows that the operating conditions can be successfully met.

INTRODUCTION

The dc superconducting power transmission line (SPTL) has the highest power capability of any transmission line — existing or under development. This fact, together with its low loss and freedom from system constraints, such as electrical stability, reactive compensation and short circuit current level, make it extremely attractive for bulk power transmission. Figure 1 shows the conceptual design of the dc SPTL which is now under development at the Los Alamos Scientific Laboratory (LASL). One single coaxial cable carries both the go and return current of a monopolar transmission line. The parameters of three similar dc SPTL's of different power ratings are given in Table I. Operating voltages and currents for each cable were selected from an economic analysis of the required transmitted power (Fig. 2). The methodology used in this analysis has been described elsewhere [1], [2].

The fundamental difference between a dc SPTL and all other forms of power transmission is that there is no power dissipation within the line that is directly related to the transmitted power, such as the usual I²R losses. Consequently, there are no thermal limitations to the amount of power that can be transmitted by a single line, nor are there any physical limitations to carrying large currents at relatively low voltages. Conversely, a dc SPTL has no short-term excess power capability. Any "excess" capability built into a system can be maintained 24 hours a day. On the other hand, the current density in the superconductor itself is limited by its temperature and magnetic flux density (Fig. 3). These three parameters define a critical surface. Superconductivity can

Fig. 1. Conceptual design of the Los Alamos dc SPTL.

TABLE I

Parameters of Three DC SPTL's

Design	A	B	C
Rated Power, GW	2.5	5.0	7.5
Rated Voltage, kV	100.	200.	300.
Rated Current, kA	25.	25.	25.
Current Density, A/mm ²			
in superconductor	15000.	15000.	15000.
overall	90.	90.	90.
Max. Electrical Stress, kV/mm	10.	15.	20.
Inductance, nH/m	119.	158.	178.
Capacitance, pF/m	234.	175.	156.
Surge Impedance, Ω	22.5	30.1	33.8
Diam of Central Channel, mm	25.	25.	25.
ID of Dielectric, mm	33.7	33.7	33.7
OD of Dielectric, mm	61.0	74.3	82.1
OD of Cable, mm	73.4	87.7	96.0
ID of Enclosure, mm	82.7	96.1	103.8
OD of Enclosure, mm	248.	288.	312.
No. of Subcables			
Inner Conductor	20.	20.	20.
Outer Conductor	90.	90.	90.

only exist inside the volume defined by that surface, which is different for each superconducting alloy or compound. The critical temperature of Nb₃Sn, the material selected in our work, is 17 to 18 K. If properly prepared and arranged, Nb₃Sn can support a critical dc current density of 15 000 A/mm² at 14 K and 0.5 T (5 kG). Within the 1 to 10 GW range, line ratings become totally a matter of economics and reliability. The hardware cost per GW of installed transmission decreases markedly as the power level is increased.

*Work performed under the auspices of U.S.E.R.D.A.

Fig. 2. Hardware cost per meter of line vs voltage for three dc SPTL's of different power levels. Cost includes cable and cryogenic envelope but not installation or converters. A = 2.5 GW; B = 5 GW; C = 7.5 GW.

Although a superconductor offers zero resistance (i.e., no power dissipation) to dc, it experiences power dissipation under ac and electrical and mechanical transients because of magnetic flux movement inside the superconductor. These losses cause localized heating in the superconductor; if not contained, the critical temperature limit for the operating condition will be exceeded, driving the superconductor "normal." This event would then be followed by destructive localized power dissipation because the normal state resistivity of most superconducting alloys is around $4 \times 10^{-7} \Omega\text{-m}$ (20 times the resistivity of copper at room temperature). A superconductor is stabilized by controlling all temperature excursions and by adding closely coupled parallel normal conductor (cryoconductor or cryostabilizer), such as copper with a low-temperature resistivity of $10^{-10} \Omega\text{-m}$ (100 times lower than copper at room temperature), so that the composite can continue to carry the required currents, at least temporarily [3]. Figure 4 shows the cross section of a stabilized composite superconducting wire to be used in the dc SPTL [4]. Under transient conditions, the current can easily transfer from the superconductor to the copper matrix. However, the result of this method of stabilization is a reduction of the effective current density (referred to the total wire cross section) to about 90 A/mm².

In the application of the stabilized superconductor in a dc SPTL, energy losses are incurred because of the ripple current present in dc transmission of electric power and because of transient faults. Either will produce hysteresis losses in the superconductor and ac resistive losses in its copper matrix. The extent to which such currents will divide between the copper matrix and the superconductor will depend on the geometry of the wire and cable and on the wave shape and magnitude of the transient. Once the fault is removed, steady-state current can continue to flow through the superconductor, provided the energy losses in the cryostabilizer during the transient condition have not raised the temperature of the superconductor beyond its critical

Fig. 3. The phase diagram for the superconducting state.

Fig. 4. Cross section of a stabilized multifilamentary superconducting wire. Bronze (BRZ) containing niobium (Nb) tubes are located within copper (Cu) matrix. Nb₃Sn superconductor is formed by diffusion reaction on the inside of the niobium tubes.

temperature. The dc SPTL system should, therefore, be designed so that neither the steady-state losses caused by the ripple current nor the transient losses due to fault currents exceed the permissible limits. This paper discusses some of the electrical characteristics of the Los Alamos dc SPTL, their rationale, and their relation to the safe and reliable operation of a stabilized superconducting cable.

RIPPLE LOSSES

Harmonic currents on the dc SPTL produced both by the normal and the abnormal harmonic voltage sources have been computed for a 100-km long dc SPTL under various operating conditions. The computations of the normal harmonics are based on the standing-wave theory of long transmission lines. The computations of the abnormal current harmonics were performed by representing the dc SPTL as an equivalent π -network because the line length at these frequencies is less than the quarter-wavelength. It was assumed during the entire analysis that the dc SPTL is terminated at either end by a smoothing reactor. No other filter network is connected to the dc SPTL.

Long DC SPTL

The source of harmonics is obviously the inverter. It is considered to be a voltage source for the dc-side harmonics. The equivalent circuit of the dc SPTL with the converter stations at either end is shown in Fig. 5. The voltages V_1 and V_2 are the harmonic voltage sources and L_T is the dc smoothing reactor.

The harmonic voltages generated at either end will be attenuated by the dc smoothing reactors and will travel along the dc SPTL in opposite directions with almost no attenuation but changing phase. They will be reflected by the reactors repeatedly as they travel back and forth along the dc SPTL. The magnitude of a harmonic at any point along the dc SPTL will be the sum of these two components. As a result, the harmonic voltage or current level will exhibit standing wave patterns with successive maxima and minima. The maxima occur when these two components are in phase, minima when they are out of phase by π radians.

The analysis is made by a step-by-step process [5]. During the first step, the current distribution $I_1(x)$ caused by one voltage source (V_1) is obtained, assuming the other voltage source (V_2) short-circuited. During the second step, the current distribution $I_2(x)$ caused by the other voltage source (V_2) is obtained, assuming the first voltage source (V_1) short-circuited. During the final step, the two current distributions are superimposed to obtain the resultant current distribution.

The magnitudes and phase angles of the generated harmonic voltages, V_1 and V_2 , will generally be different. As the ac systems on either side of the dc SPTL are asynchronously connected, the phase angles will vary at random. The general solution for the harmonic current along the dc SPTL is given in Appendix I. The maxima of the harmonic current for the special cases when the two generated harmonic voltages, V_1 and V_2 , are equal in magnitude, V_n , but differ in phase angle, θ , by 0, $\pi/2$ and π are shown below.

For $V_1 = V_2 = V_n$ and $\theta = 0$,

$$I_{\max} = V_n / [2\pi f_n L_T \sin(\beta L/2)]; \quad (1)$$

for $V_1 = V_2 = V_n$ and $\theta = \pi/2$,

$$I_{\max} = V_n / [2\sqrt{2}\pi f_n L_T \sin(\beta L/2)]; \quad (2)$$

for $V_1 = V_2 = V_n$ and $\theta = \pi$

$$I_{\max} = V_n / [2\pi f_n L_T \cos(\beta L/2)]; \quad (3)$$

where

- V_n = generated harmonic voltage, V
- f_n = harmonic frequency, Hz
- L_T = inductance of smoothing reactor, H
- $\beta = 2\pi f_n / L_T C$, rad/m
- L = inductance of SPTL, H/m
- C = capacitance of SPTL, F/m
- l = length of SPTL, m.

Short DC SPTL

For short transmission lines ($L < \lambda/4$), the line can be represented by its lumped constants, either as a π - or as a T-network. A π -network was selected for this analysis (Fig. 6).

Fig. 5. Schematic representation of a long transmission line

With this method, the current (I_3) through Z_L can be assumed to be the harmonic current in the dc SPTL. Filter capacitances can be incorporated into the admittances ($Y_L/2$), if necessary. The current through the dc SPTL is given by

$$I_3 = (V_1 - V_2) / [4\pi f_n L_T \cos(\beta L/2) + Z_c \sin \beta L], \quad (4)$$

where

V_1, V_2 = generated harmonic voltages at either end of SPTL, V

Z_c = surge impedance of SPTL, Ω .

The detailed computations are shown in Appendix II. It should be noticed in Eq. (4) that if $V_1 = V_2$, no harmonic current will exist in the dc SPTL. Computations were made with the assumption that $V_1 = -V_2$.

Computation of Harmonic Currents and Losses

The dc SPTL characteristics (L_T, L, C) and the converter characteristics (V_n, f_n) are required to compute the harmonic currents along the dc SPTL.

The harmonic characteristics of the dc SPTL for one application are shown in Table II. Three values for the dc smoothing reactor (L_T) were chosen — 1, 2 and 4 p.u.

A 12-pulse converter was assumed. It means that the normal dc-side harmonics will be the 12th and its multiples. However, abnormal harmonics do exist in actual systems because of imbalances and mismatch in the ac systems and the converter bridges. The normal harmonic voltages generated on the dc side were obtained from [6] and [7], the abnormal harmonic voltages from [8]. Computations for the abnormal harmonic currents showed that the resulting heating of the conductor is insignificant.

Fig. 6. Schematic representation of a short transmission line.

TABLE II

Harmonic Current Maxima and Conductor Losses
Twelve-Pulse Operation; 100-kV, 2.5-GW dc SPTL
Line Length = 100 km
Firing Angle = 15°
Overlap Angle = 22.6°

Smoothing Reactor p.u.	Frequency Hz	Max. Harmonic Current A(rms)	Conductor Losses W/km
1.0	720.	248.	49.
	1440.	14.	0.2
2.0	720.	124.	12.
	1440.	7.	0.05
4.0	720.	62.	3.
	1440.	3.5	0.01

The ripple current produces two types of losses in the conductor — hysteresis losses in the superconductor and ac resistive losses in the copper matrix. The hysteresis losses caused by the ripple current superimposed on dc are given by the Bean-London Equation [9],[10]:

$$P_s = 2\mu_0 f_n \sigma_p^2 / 3J_c \quad (5)$$

where

P_s = hysteresis losses, W/m²
 μ_0 = $4\pi \times 10^{-7}$, H/m
 f_n = harmonic frequency, Hz
 σ_p = peak induced current, A/m
 J_c = critical current density of superconductor, A/m².

LOSSES CAUSED BY FAULT CURRENT

During an overcurrent condition caused by a fault, the total current may divide between the superconductor and the copper cryostabilizer or it may transfer entirely into the cryostabilizer. This will produce resistive losses in the copper, and hence temperatures rise. As long as the critical temperature conditions of the conductor are not exceeded, power can continue to be transmitted as soon as the fault is removed. However, if the critical temperature is exceeded, power has to be interrupted until the conductor is recooled. Therefore, it is essential to know the fault-current capability of the dc SPTL.

The most severe fault current through the dc SPTL will occur if the line-end bushing of the inverter-side smoothing reactor flashes over (Fig. 7). The fault current will consist of two components. The first component will be a traveling wave caused by the discharge of the cable. The second component will be driven by the voltage source on the ac side of the rectifier.

Fig. 7. Flashover of line-end bushing of inverter-side smoothing reactor.

The magnitude and duration of the cable discharge current cannot be controlled by any external means, such as valve control of the converter or a dc circuit breaker. The second component of fault current can be controlled by these external means, and the fault current profile will be dependent upon the means of interruption.

DC SPTL Discharge Current

The analysis for the cable discharge current was made as follows [11]:

- (1) apply cancellation voltage at the point of flashover,
- (2) short circuit all other voltage sources, and
- (3) open circuit all current sources.

Traveling waves (V_r, I_r) will be created at the instant of short circuit, given by the relationship

$$I_r = V_r / Z_c \quad (6)$$

where

V_r = cancellation voltage
 = system voltage, V_{ac} .

These waves will travel along the dc SPTL, will be reflected (V_r, I_r) by the smoothing reactor near the rectifier, and will partially penetrate into the reactor (V_r, I_r). The reflected and the transmitted current waves are given by

$$I_r = (V_r / Z_c) [2 \exp(-Z_c t / L_T) - 1] \quad (7)$$

and

$$I_t = (2V_r / Z_c) [1 - \exp(-Z_c t / L_T)] \quad (8)$$

If L_T / Z_c is large compared with the travel time along the dc SPTL, then Eqs. (7) and (8) can be simplified to the following

$$I_r = -V_r / Z_c = -V_{ac} / Z_c \quad (9)$$

and

$$I_t = 0 \quad (10)$$

Physically, a rectangular current wave ($I_r = V_{ac} / Z_c$) will be generated at the flashover point at the instant of flashover. This wave will travel along the dc SPTL and be reflected at the rectifier-end smoothing reactor. A reflected current wave ($I_r = -I_r$) will travel back, canceling the forward current wave (I_r). The duration (τ) of the discharge current at the point of flashover is given by

$$\tau = 2L/v \quad (11)$$

where

L = length of dc SPTL
 v = velocity of propagation in dc SPTL
 = $1/\sqrt{LC}$.

The duration of the discharge current diminishes monotonically along the dc SPTL and is zero at the rectifier end. Table III shows the magnitude and duration of the discharge current for the three dc SPTL's considered.

TABLE III

DC SPTL Discharge Current at Fault
Line Length = 100 km

DC SPTL Design	I kA	τ ms	Conductor Temp. Rise K
A	4.43	1.05	0.24
B	6.65	1.05	0.28
C	8.87	1.05	0.32

DC SPTL Fault Current With Valve Control

The second component of the fault current will be maintained by the voltage sources on the ac side of the rectifier. Therefore, the ac-side reactances, the smoothing reactor and the dc SPTL reactance will limit this component of the fault current. The following assumptions were made:

1. Fault is initiated at the beginning of commutation.
2. There is no commutation overlap.
3. Fault current is interrupted by blocking the firing of the subsequent valves.
4. Firing angle delay is zero.
5. Converters operate in 12-pulse mode.
6. AC network reactance beyond the rectifier transformer is negligible.

The 12-pulse system, with its equivalent circuit for the computation of the fault current, is shown in Fig. 8. If the fault starts at $\theta_a = \pi/3$ when the reference valve comes into conduction (Fig. 9), the fault current will continue to increase even if the sensing system is fast enough to block the next valve which would have started conducting at $\theta_1 = \pi/2$. The fault current will continue to increase until the ac voltage in the loop reaches zero. The fault current will then decrease until it is zero when $\text{fvdt} = 0$. If the next valve is not blocked, then the fault current will continue to rise until the new voltage around the loop is zero. Similarly, as the subsequent valves are not blocked, the fault current level will increase.

Fig. 8. Representation of a 12-pulse rectifier bridge with fault at inverter end.

Fig. 9. Voltage across 12-pulse rectifier bridge and current profile under fault condition.

Details of the analysis are shown in Appendix III. A similar analysis has been performed neglecting the transformer reactance [12].

The temperature rise of the conductor was calculated on the conservative assumption that as soon as the fault starts, both the fault component of the current and the pre-fault steady-state current flow through the copper matrix. Table IV shows the limiting fault component of current which is permissible before the superconductor goes normal. The entry n_{max} in Table IV denotes the maximum number of subsequent valves which may be permitted to conduct after the initiation of the fault. The total current is obtained by adding the steady-state current to the fault component of current, shown in the Table. The conductor temperature rise includes the contribution from the rectangular discharge current wave of the cable. Figure 10 shows the profiles for the fault current and conductor temperature rise for $n = 2$.

DC SPTL Fault Current With DC Circuit Breaker

DC power circuit breakers are not commercially available, but three types are being developed [13]-[16]. Although the modes of operation of these three types of circuit breakers are significantly different, they are similar in two basic principles:

1. the fault current is not limited during the initial period of sensing and contact opening; and
2. the total current is diverted to a nonlinear resistor during the final period of interruption.

The time required from the initiation of contact opening to the current transfer into the nonlinear resistor is 3-4 ms for the first two types of breakers [13]-[15]. The third type of breaker requires 40-60 ms [16]. The initial delay period (t_d) of uncontrolled fault current is the sum of the relaying time, the contact opening time and the time required to transfer current from the main circuit breaker to the nonlinear resistor.

TABLE IV

Maximum Allowable Fault Component of Current
in DC SPTL with Converter Control
Commutating Reactance, $L_c = 0.18$ p.u.

DC SPTL Design	Switching Reactance p.u.	n_{max}	Peak Fault Component of Current p.u.	Duration ms	Conductor Temperature Rise K
A	1	1	0.71	12.5	2.2
	2	2	0.64	15.3	2.4
	4	3	0.50	18.0	2.5
B	1	1	0.82	12.5	2.4
	2	2	0.72	15.3	2.6
	4	3	0.53	18.0	2.6
C	1	1	0.90	12.5	2.5
	2	1	0.79	12.5	2.1
	4	3	0.55	18.0	2.6

Fig. 10. Profiles of fault current, critical current and conductor temperature rise. Fault cleared by valve control at $n = 2$, i.e., two subsequent valves are fired after fault is initiated; $L_c = 0.18$ p.u.; $L_T = 2$ p.u. Solid line is total current; dashed line is temperature rise of conductor; dotted line is superconductor critical current at the increased temperature.

Computations of the fault current were made for two values of $t_d = 5$ ms and 10 ms. The characteristics of the nonlinear resistor were assumed to be [17],[18]:

$$v_a = ki^b; \quad (12)$$

where $k, b = \text{constants}$.

Computation of the current profile for the initial period (t_d) were made by the procedure shown in Appendix III. The current at the end of that period is the peak of the total current (i_{mt}), including the prefault load current. The current starts to decay once it is transferred to the nonlinear resistor, according to the following relation:

$$L(di/dt) + ki^b = 0. \quad (13)$$

The solution of this equation is given by

$$i^{1+b} = i_{mt}^{1+b} - (k/L) (1+b) t. \quad (14)$$

The constant k was derived on the assumption that $v_a = 1.7$ V_{dc} at i_{mt} . In actual applications, k can be adjusted to the desired value by series-parallel combination of the nonlinear resistor bank. A value of 0.05 was used for b in agreement with [17] and [18]. Table V shows the fault component of the current and the conductor temperature rise for the three dc SPTL designs. The thermal recovery times are also shown in the Table. The thermal recovery time is defined as the time required by the conductor to cool down to the temperature at which the critical current is 1 p.u. In other words, full power can be switched on to the dc SPTL after the lapse of the thermal recovery time. Figures 11 and 12 show the fault-current profile for the 100-kV, 2.5-GW dc SPTL and the conductor temperature rise for two values of circuit breaker delay. The fault current profiles for the other two cables are almost coincidental with that for the 100-kV cable.

Fig. 11. Profiles of fault current, critical current and conductor temperature rise. Fault cleared by dc circuit breaker at $t_d = 5$ ms; $L_c = 0.18$ p.u.; $L_T = 2$ p.u.

TABLE V

Fault Component of Current in DC SFTL
with DC Circuit Breaker
Commutating Reactance, $L_c = 0.18$ p.u.

DC SFTL Design	Smoothing Reactor p.u.	Delay Time ms	Peak Fault Component of Current p.u.	Duration ms	Conductor Temperature Rise K	Thermal Recovery Time ms
A	1	5	0.72	12.5	1.6	0
	1	10	1.43	21.0	3.6	70
	2	5	0.50	14.5	1.5	0
	2	10	1.01	22.5	3.0	30
	4	5	0.32	18.0	1.4	0
	4	10	0.64	26.0	2.6	0
B	1	5	0.83	12.0	1.7	0
	1	10	1.67	20.0	4.0	100
	2	5	0.56	14.0	1.5	0
	2	10	1.12	22.0	3.2	40
	4	5	0.34	17.5	1.4	0
	4	10	0.68	25.5	2.6	3
C	1	5	0.91	12.0	1.8	0
	1	10	1.82	20.0	4.3	100
	2	5	0.59	13.5	1.6	0
	2	10	1.19	21.5	3.3	50
	4	5	0.35	17.0	1.5	0
	4	10	0.70	25.5	2.7	6

DISCUSSION

Thermal Response Model

The long-term (minutes and hours) thermal performance of the cable depends strongly on the specific wire and cable design and on the cryogenic heat transfer conditions. However, faults will take place essentially adiabatically. Therefore, the conservative assumption is that all energy is initially taken up in the enthalpy of the metallic conductors. Under normal operating conditions the temperature of the line will vary by 2 K along its length (between the refrigeration stations) so that the thermal safety margin will be different at different points. Again the conservative assumption is that all excursions start from the normal maximum temperature of 12 K. Finally, it is assumed (pessimistically) that all major disturbances will cause the superconductor to be driven into the normal state, since the associated rates of change of the magnetic field are between 20 and 50 T/s. As a result both the fault component of the current and the normal pre-fault line current are assumed to be in the copper and heating it. The criterion for safe operation is that at the end of the disturbance the temperature has risen to a lower value than that at which the superconductor critical current is at least 1 p.u. For our model this temperature is 14.6 K.

For the heating calculations in the copper we take the previously mentioned dc resistivity of 1×10^{-10} Ω -m, which also includes magneto-resistivity. A magnetic field diffusion "time constant" of about 0.3 ms can be used to characterize the penetration through a radius of 0.2 mm of such cryoconductor. From this we can estimate the frequency-dependent enhancement of the ac resistivity (including the proximity effect) at 2x for a 1-ms square wave, 1.5x for 720-Hz ripple and 1.3x for slower disturbances with half-periods of 10 to 50 ms. For steady-state heat losses due to all causes, a limit of 50 W/km has been used, which means that maximum ripple losses of 20 to 30 W/km are acceptable.

The thermal capacity per unit length of the helium refrigerant in the line is about 2 orders of magnitude larger than that of the metallic conductor. The conductor will therefore recoil to the helium temperature with a time constant given by

$$\tau_r = mc_p/hA \quad (15)$$

where

- m = mass per unit length, kg/m
- c_p = heat capacity per unit mass, J/kg/K
- h = heat transfer coefficient, W/m²/K
- A = heat transfer area, m².

Fig. 12. Profiles of fault current, critical current, conductor temperature rise and thermal recovery. Fault cleared by dc circuit breaker at $t_d = 10$ ms; $L_c = 0.18$ p.u.; $L_T = 2$ p.u.

The only uncertain quantity in the above equation is the value of the heat transfer coefficient which depends on flow parameters including velocity and turbulence. For a conservative h value of $5 \text{ W/m}^2/\text{K}$, τ_r becomes about 170 ms.

Ripple Losses

The harmonic currents were computed with no dc-side harmonic filters in the system. The hysteresis losses in the superconductor were negligible, most of the losses being incurred in the copper cryostabilizer. As shown in Table II, the conductor losses are well within the design goal of 50 W/km , except at 720 Hz and $L_T = 1 \text{ p.u.}$ The losses in the cryostabilizer can be further reduced either by installing a 12th harmonic filter, or by increasing L_T , or by redesigning the conductor with more copper. It appears at the present time that a higher L_T will be the best solution. This will also improve the performance of the dc SPTL under faults.

Fault Current

Analysis of the fault current was performed under assumptions which produced conservative results. Nonzero firing angle delay and overlap angle will decrease the fault current level. Only the commutating reactance of the converter transformer was considered in the analysis. Inclusion of the ac system impedance would further reduce the fault current level. Modern control schemes for 12-pulse hvdc systems would not allow more than one commutation after a line-to-ground fault [19]. Therefore, fault currents beyond $n = 1$ need not be considered. Nevertheless, the present analysis considered up to $n = 10$, the primary objective being to provide a simplified method in the understanding of the dc SPTL performance. Figure 10 shows that even with $n = 2$, the critical current (I_c) at the end of fault interruption is greater than 1 p.u., meaning that the dc SPTL will be able to carry full power immediately after the fault.

Although no hvdc circuit breakers are commercially available, it is expected that in the future dc breakers will play a major role in the hvdc transmission of power. Analysis was performed with two assumed delay times of the breaker — 5 ms and 10 ms. A breaker with delay time less than 5 ms may not be practical. Similarly, a breaker with a delay time longer than 10 ms will not be very useful without assistance from valve control. Figure 11 shows that I_c is nearly 1.5 p.u. when the fault is interrupted by a breaker with $t_{br} = 5 \text{ ms}$. Full power can be turned on the dc SPTL immediately after the fault is cleared. However, if $t_{br} = 10 \text{ ms}$ (Fig. 12), partial power may be restored to the dc SPTL. If it is required that full power be restored immediately after a fault is cleared by a 10-ms breaker, then the dc SPTL could be redesigned with more cryostabilizer. Engineering compromises can also be made where partial power is immediately switched on and full power is gradually attained as the conductor is cooled by helium.

It is evident from Table V that the recovery time for the dc SPTL is very short — less than 100 ms for the assumptions made in this study. For transient faults, at least this time interval will be required for the deionization of the arc at the fault.

CONCLUSIONS

A well-designed dc SPTL can successfully withstand the expected ripple losses and meet the fault-current requirements while transmitting large blocks of power with high efficiency and with virtually no systems constraints.

ACKNOWLEDGMENTS

The authors would like to thank their colleagues Martin P. Maley for a discussion of hysteresis losses and John W. Dean for a discussion of cryogenic heat transfer.

APPENDIX I

Ripple Current for Long DC SPTL

For a long single-source transmission line, the voltage and the current along the line are given by [20]

$$V(x) = V_r \cosh(\gamma x) + I_r Z_c \sinh(\gamma x) \quad (16)$$

$$I(x) = I_r \cosh(\gamma x) + \frac{V_r}{Z_c} \sinh(\gamma x) \quad (17)$$

where, V_r = receiving-end voltage, V

I_r = receiving-end current, A

γ = propagation constant of the line

$= \alpha + j\beta$, nepers/m and radians/m

x = distance of the measurement point from the receiving end, m

Z_c = characteristic impedance of the line, Ω

The voltage and current distributions along the dc SPTL (Fig. 5) when $V_2 = 0$ or $V_1 = 0$ are then derived separately. The resultant voltage at a point x from V_2 is obtained by adding the two separate solutions. The resultant voltage along the dc SPTL is then given by

$$V(x) = \frac{Z_c}{(Z_T + Z_c)(e^{\gamma l} - K^2 e^{-\gamma l})} [V_1(e^{\gamma x} + K e^{-\gamma x}) + V_2(e^{\gamma(l-x)} + K e^{-\gamma(l-x)})] \quad (18)$$

where, Z_T = dc smoothing reactor

$$K = \frac{Z_T - Z_c}{Z_T + Z_c}$$

As the currents are flowing in opposite directions for $V_2 = 0$ and $V_1 = 0$, the resultant current along the dc SPTL is obtained by subtracting the individual solutions for current.

Thus,

$$I(x) = \frac{1}{(Z_T + Z_c)(e^{\gamma l} - k e^{-\gamma l})} [V_1(e^{\gamma x} - k e^{-\gamma x}) - V_2(e^{\gamma(l-x)} - k e^{-\gamma(l-x)})] \quad (19)$$

The same result for the resultant current $I(x)$ is obtained by considering $V(x)$ of Eq. (18) as composed of a forward component and a reflected component, e.g.,

$$V(x) = V^+(x) + V^-(x) \quad (20)$$

$$\text{Then, } I(x) = \frac{V^+(x)}{Z_c} - \frac{V^-(x)}{Z_c} \quad (21)$$

For the dc SPTL,

$$Z_T = j2\pi f_n L_T \gg Z_c \quad (22)$$

$$\gamma = \alpha + j\beta = j2\pi f_n \sqrt{LC} \quad (23)$$

$$k = 1 \quad (24)$$

where,

f_n = harmonic frequency, Hz

L = dc SPTL inductance, H/m

C = dc SPTL capacitance, F/m

The Eqs. (18) and (19) are thus simplified to

$$V(x) = \frac{Z_c}{2\pi f_n L_T \sin \beta l} [V_1 \cos \beta x + V_2 \cos \beta(l-x)] \quad (25)$$

$$I(x) = \frac{1}{2\pi f_n L_T \sin \beta l} [V_1 \sin \beta x - V_2 \sin \beta(l-x)] \quad (26)$$

Assuming V_1 as the reference phasor,

$$V_1 = V_1 \angle 0 \quad (27)$$

$$V_2 = k_0 V_1 \angle \theta \quad (28)$$

The Eq. (26) is reduced to

$$I(x) = \frac{jV_1}{\omega L_T \sin \beta l} [\sin \beta x - k_0 \sin \beta(l-x) \angle^\theta] \quad (29)$$

The harmonic current minima can be found by putting $I(x) = 0$.

This means,

$$\sin \beta x - k_0 \sin \beta(l-x) \angle^\theta = 0 \quad (30)$$

Solution of Eq. (30) leads to

$$x_{\min} = \frac{n\pi + \phi}{\beta} \quad (31)$$

$$x_{\max} = \frac{(2n+1)\pi + 2\phi}{\beta} \quad (32)$$

where,

$$\phi = \arctan \left(\frac{k_0 \cos \theta \sin \beta l}{1 + k_0 \cos \theta \cos \beta l} \right) \quad (33)$$

APPENDIX II

Ripple Current for Short DC SPTL

The components of the equivalent π -network (Fig. 6) can be determined as follows [20]

$$Z_k = Z_c \sinh(\gamma l) \quad (34)$$

$$\frac{Y_l}{2} = \frac{\tanh(\gamma l/2)}{Z_c} \quad (35)$$

The solution of the circuit of Fig. 6 is given in matrix form as,

$$[I] = [Z]^{-1}[V] \quad (36)$$

where,

$$[I] = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad (37)$$

$$[V] = \begin{bmatrix} V_1 \\ 0 \\ V_2 \end{bmatrix} \quad (38)$$

$$[Z] = \begin{bmatrix} (Z_T + 2/Y_k) & 0 & -2/Y_k \\ -2/Y_k & -2/Y_k & (Z_T + 4/Y_k) \\ 0 & -(Z_T + 2/Y_k) & 2/Y_k \end{bmatrix} \quad (39)$$

Solving Eq. (36),

$$I_3 = \frac{(V_1 - V_2)}{Z_T Z_L Y_k / 2 + 2Z_T + Z_k} \quad (40)$$

APPENDIX III

Fault Current Profile with Converter Valve Control

From Fig. 8, the loop equation for the fault current is

$$v(t) = L di/dt \quad (41)$$

where, $v(t) = v_1(t) + v_2(t)$

$v_1(t)$ = voltage across bridge 1

$$= \sqrt{2} V_{LL} \sin(\omega t + \theta)$$

$v_2(t)$ = voltage across bridge 2

$$= \sqrt{2} V_{LL} \sin(\omega t + \theta + \pi/6)$$

V_{LL} = line-to-line rms voltage across each

bridge

θ = angle of bridge 1 voltage when fault occurs

$\alpha = \pi/3$ when fault occurs at commutation of a valve

t = time measured from the instant the fault occurs

$$L = 4L_c + L_T + L_2$$

From Eq. (41)

$$i(t) = \frac{\int_0^t v_1(t)dt + \int_0^t v_2(t)dt}{L} \quad (42)$$

The peak of the fault current (i_m) will be reached when the resultant voltage is zero, i.e., $v(t) = 0$ at a time $t = t_m$.

$$\begin{aligned} \text{Then, } i_m &= \frac{\int_0^{t_1} v_1(t)dt + \int_{t_1}^{t_m} v_1(t)dt + \int_0^{t_1} v_2(t)dt + \int_{t_1}^{t_m} v_2(t)dt}{L} \\ &= \frac{A_{11} + A_{12} + A_{21} + A_{22}}{L} \end{aligned} \quad (43)$$

where, t_1 = time when the first valve in bridge 2 is commutated after the initiation of fault

When the firing delay angle (α) is zero, $t_1 = \pi/6\omega$ and $t_m = 7\pi/12\omega$. Because of delay in sensing, if the next n valves are fired, the peak of the fault current is given by

$$i_m = \frac{(n+1)(A_{11} + A_{21}) + A_{12} + A_{22}}{L} \quad (44)$$

The time (t_m) to reach the peak of the fault current is given by

$$t_m = \frac{n\pi}{6\omega} + \frac{7\pi}{12\omega} \quad (45)$$

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