DIP COATING PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon
Sheet Task of the Low-Cost Silicon Solar Array Project.
Quarterly Report No. 4, September 17, 1976–December 17, 1976

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December 28, 1976

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Honeywell Corporate Research Center
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ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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by

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ABSTRACT

The objective of this research program is to investigate the technical and economic feasibility of producing solar cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

With the present dip coating facility, pulling rates of 5 to 7 cm/min are most likely to produce layers of the crystalline quality from which high efficiency solar cells can be fabricated. At a pulling rate of 6 cm/min, it is possible to achieve smooth 50- μ m to 100- μ m thick layers, with grains as large as 2.5-mm wide, generally extending the entire length of the substrate. At pulling rates less than 6 cm/min, single grains as large as 4 mm in width have been observed. Substrates held at an angle of 45° to the surface of the melt during dipping produced layers qualitatively similar to the vertical dipped layers, but they show some potential for improved coating uniformity.

Diffraction measurements on several samples showed that the strongest diffraction peak was from the silicon 220 plane which is about 10° from the sample surface. The {110} surfaces have been found to be dominant in the EFG and dendritic material, and it appears this is a general characteristic of sheet-grown silicon.

Mullite substrates containing an excess of SiO_2 have been shown to match the thermal expansion coefficient of silicon. Mullite, however, dissolves slightly in the silicon melt, adding aluminum impurities to the silicon layers. A preliminary Ion Beam Microprobe analysis revealed that the aluminum concentration measured in three samples of typical dip-coated silicon layers correlated correctly with the measured resistivities.

The extent to which substrate dissolution in the melt affects the electrical properties of the silicon layers and melts is under investigation.

Different compositions of mullite have been found to dissolve at approximately the same rate. Impurities from the mullite appear to be detrimental to solar cell performance, and methods are being investigated to inhibit or retard substrate dissolution. Reducing the contact time and area between the substrate and the melt is one approach that will be investigated. An alternative solution is to coat the substrate with vitreous graphite, thereby isolating it from the molten silicon. Tylan Corporation's Vitre-Graf coatings have been tried, and they possess good silicon wettability and considerably inhibit dissolution of mullite.

Photodiodes were made on a number of silicon on ceramic (SOC) layers. The diode performance improved as the amount of mullite dissolved by the silicon decreased. The best performance to date is 5 percent energy conversion efficiency and 9.5 percent inherent efficiency at 100-mw illumination.

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

During this reporting period, the effect of pulling rate and melt temperature on silicon layer thickness has been further characterized. In the present dip coating facility, pulling rates of 5 to 7 cm/min are most likely to produce layers of the crystalline quality from which high efficiency solar cells can be fabricated. At a pulling rate of 6 cm/min, it is possible to achieve smooth 50- μ m to 100- μ m thick layers, with grains as large as 2.5-mm wide, generally extending the entire length of the substrate. At pulling rates less than 6 cm/min, single grains as large as 4 mm in width have been observed. Substrates held at an angle of 45° to the surface of the melt during dipping produced layers qualitatively similar to the vertically dipped layers, but they show some potential for improved coating uniformity.

Mullite substrates containing an excess of SiO_2 have been shown to match the thermal expansion coefficient of silicon. Slip cast mullite bodies, in which the Al_2O_3 content is as high as 60 weight percent, have shown compatibility with the dip coating process.

The extent to which substrate dissolution in the melt affects the electrical conductivity of the silicon layers and melts has been investigated. It was determined that higher purity mullite dissolves in approximately the same proportion as the rolled, dried and fired mullite more commonly used in the program. The rubbed-on graphite substrate coatings offer little protection to the dissolution rate. On the other hand, Tylan Corporation's

Vitre-Graf substrate coatings have good silicon wettability and considerably inhibit the dissolution of mullite in molten silicon.

A preliminary Ion Beam Microprobe analysis revealed that the aluminum concentration measured in three samples of typical dip-coated silicon layers was approximately related to their measured resistivities.

Diffraction measurements on several samples showed that the strongest diffraction peak was from the silicon 220 plane which is about 10° from the sample surface. The {110} surfaces have been found to be dominant in the EFG and dendritic material, and this appears to be a general characteristic of sheet-grown silicon.

Photodiodes have been made on a number of silicon on ceramic (SOC) layers. The diode performance improved as the amount of mullite dissolved by the silicon decreased. The best performance to date is 5 percent energy conversion efficiency and 9.5 percent inherent efficiency at 100-mw illumination.

A computer program has been written which fits diode I-V data to equivalent circuit models. The fit is useful in calculating inherent efficiencies of photodiodes, and the variation of model parameters should be helpful in identifying ways of improving energy conversion efficiency.

For comparison purposes, control photodiodes were made using single crystal silicon. The control photodiodes made with conventional geometry normally have uncorrected conversion efficiencies of 8-9 percent. The control photodiodes made in the same way as the SOC diodes, namely with front surface contact to the base, have lower efficiencies, essentially the same as those of the SOC photodiodes.

A possible reason for the differences in efficiencies is the contacts

and methods of evaluating contact resistance developed. Nickel contacts to p-type silicon can have low contact resistance but have an unusual nonlinear behavior. Other possible reasons for the performance differences are also being investigated.

EBIC measurements of diode uniformity and of minority carrier diffusion length have begun. Preliminary results suggest a diffusion length of about 25 μm .

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INTRODUCTION

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 10 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. If dip coating or other approaches for producing silicon on ceramic (SOC) can be shown to produce solar cell-quality sheet silicon, it offers an outstanding cost-effective way to produce inexpensive, large-area solar cells.

The SOC approach has excellent scale-up potentialities. With the dip coating method it is possible to coat several wide, large-area substrates in one dipping. An alternative plan would be to silicon-coat, in a continuous manner, large-area substrates. The investigation has shown that as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

Since the inception of this program, an experimental dip coating facility was designed and constructed. In this facility a variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match

the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm² in area have been achieved with single crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this (SOC) sheet silicon, to date, is promising. Photodiodes have been fabricated that, without the benefit of an antireflecting coating and minimized series resistance, demonstrated a measured conversion efficiency of ~5 percent. After correction for the absence of an antireflection coating and allowing for excess series resistance, which results from the fabrication geometry, these dip-coated layers show an inherent conversion efficiency of 9.5 percent.

The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The aluminum and other impurities of the substrate are believed to adversely affect solar cell conversion efficiency. A special type of graphite coating on the substrate has shown a potentiality for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar cell performance should be forthcoming.

An alternative solution to this dissolution problem which will be investigated is to limit the contact area and contact time between the ceramic and the molten silicon. This approach will be pursued by designing and constructing a second silicon coating facility. This additional facility will be designed to coat in a continuous manner one face of long, large-area substrates. The design will restrict the contact area of the ceramic with molten silicon and completely eliminate progressive contamination of the

melt. Further, it will permit a study of possible continued grain growth by accommodating the use of longer substrates. Finally it will reveal problems that are likely to be encountered in a scale-up process.

The balance of this document will report the progress achieved during the past quarter year of effort.

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TECHNICAL DISCUSSION

DIP COATING RESULTS

The dip coating effort during this past reporting period was directed to the following tasks:

1. To further characterize the role of pulling rate and melt temperature on silicon layer thickness and crystalline grain size.
2. To evaluate the effect of dip-coating substrates which were held at an angle to the surface of the melt during insertion and withdrawal from the melt.
3. To examine the compatibility of additional ceramic bodies and graphite coatings to the dip coating process.
4. To further study the dissolution of mullite substrates in molten silicon and to evaluate preliminary methods for minimizing or arresting this dissolution.

To date we have been unable to accurately measure and adjust the silicon melt temperature in our present dip coating facility. This problem has made it difficult to systematically characterize important layer growth parameters. Initially, thermocouple failure problems hindered this characterization effort. The temperature control thermocouple failure problem was solved, but a method for immersing a thermocouple into the molten silicon was never satisfactorily accomplished. Therefore, during this reporting period melt temperatures recorded and reported are referenced to the indicated temperature where silicon solidification is first observed in the melt. Since this method of temperature determination is subjective in

nature, an ideal method for collecting sufficient data for a specific characterization would be to operate the dip coating facility around the clock on a 24 hour/day basis. This was tried, but unfortunately after several hours of operation, silicon vapors from the melt deposit on the crucible just above the surface of the melt. Eventually this deposit restricts the immersion of our present size substrates. This annoying deposit can be melted by applying excessive melt power, but once this is done the temperature controller cannot be adequately reset to return to the exact temperature needed to continue the original experiment. Measures to overcome this experimental handicap are discussed in the Recommendation section of this report.

Figure 1 shows the silicon layer thickness as a function of pulling rate for a given melt temperature. The majority of the data were taken during one dip coating run at one temperature setting. A few additional data points, having equally reliable melt temperatures, were added to support the thickness-pull rate trend. The data is not yet complete, but the trend indicated in Figure 1 is supported by several recent unrelated dip coating runs. It is increasingly evident that in the present setup smooth, larger-grain silicon layers will not be achievable at melt temperatures less than 6 to 8°C above the melting point of silicon. Pulling rates of 6 cm/min at these temperatures should make it possible to attain smooth, large-grain (as large as 2.5-mm wide) layers of the order of 50 to 100 μ m in thickness. As shown in Figure 1, the layer thickness increases rapidly at pulling rates less than 6 cm/min. At faster pulling rates (12-18 cm/min), the layers can be made to grow thicker by lowering the melt temperature, but never without irregular dendritic growths protruding above the main surface of the layer. The above data is based on the thermal characteristics of the present system and therefore should not be interpreted as placing exact limitations on coating methods in general.

Ten substrates were dipped at an angle of 45° to the surface of the melt during insertion and withdrawal from the melt. The objective of this experiment was to see if changing the geometry of the meniscus would influence

Figure 1. Silicon Layer Thickness as a Function of Pulling Rate

the coating rate and/or quality. The principal parameters that were varied were pull rate and the sign of the dip angle (carbon-coated side of the substrate facing up or down). Six substrates were dipped with the carbon-coated side up and four with the coated side down. The pull rate was varied from 1.2 to 6 cm/min.

Examination of the silicon coatings showed that angle dipping did not drastically alter the rate or manner in which the coatings solidified. The coatings looked quite comparable to those dipped vertically, with coating thickness decreasing with increasing pull rate. However, it appeared that the coating thickness of the angle-dipped samples was more uniform than those dipped vertically. The large dendrites formed at the beginning of solidification on the angle-dipped samples did not protrude from the surface as much as those dipped vertically.

It was also interesting to note that those samples dipped with the carbon coating facing up came out of the apparatus with the silicon side clean (no silicon monoxide) and coated completely to the bottom edge, while those dipped with the carbon-coated side down came out with a light oxide coating and the last ~5 mm of substrate virtually bare. The cleanliness of the silicon surface can be explained by self-shielding of the silicon coating from the oxide vapors coming off the melt, by the substrate in one case and direct exposure to them in the other. The lack of coating at the bottom edge of the samples dipped with the carbon side down is a consequence of the manner in which the liquid "bridge" between the substrate and melt surface is formed and broken at the instant the bottom edge is pulled from the melt.

Four substrates made from segments sliced axially from McDanel's MV-30 slip cast mullite tubing were also dipped. These samples were dipped vertically with the tube axis parallel to the pulling direction. The expected variations in coating thickness were observed as pull rates and temperatures were varied. However, in comparing the nature of the silicon on the

convex surfaces to that on the concave surface it appeared that the dendrites formed on the convex surfaces were increasing in width at a somewhat higher rate than that observed on a flat surface. This could be due to either thermal or crystallographic conditions and will be investigated further. These sections of tubing yielded crack-free silicon layers with good adhesion and withstood the thermal shock of being immersed into molten silicon.

Four McDanel MV-20 rolled dried and fired mullite substrates which had a Vitre-Graf graphite coating on all surfaces were dip-coated during this reporting period. The coatings were prepared by Tylan Corporation and are reported to be $\sim 7\text{-}\mu\text{m}$ thick. The primary purpose for dip-coating these substrates was to evaluate the passivation capability of these particular graphite coatings in preventing dissolution of the mullite in the silicon melt. Since the resistivity of the silicon layer is a convenient method for obtaining the amount of mullite dissolved, thick ($150\text{--}400\text{ }\mu\text{m}$) silicon coatings were grown on the substrates to improve the accuracy of the resistivity measurements.

The Vitre-Graf coatings are comparable in wettability to the rubbed-on graphite coatings typically used, but their rate of dissolution in molten silicon is considerably less. One portion of the previously mentioned passivation capability study included soaking a Vitre-Graf coated mullite substrate in molten silicon for a period of one hour. Upon withdrawal of the substrate from the melt after this prolonged soaking, the substrate possessed a smooth, uniform silicon coating thereby demonstrating the durability of these particular graphite coatings in molten silicon. By comparison, the rubbed-on graphite coatings completely dissolved in molten silicon in less than an hour.

While there was no obvious dissolution of the Vitre-Graf coating following this prolonged soak, molten silicon did to a limited extent permeate the Vitre-Graf coating and mechanically bond to the mullite substrate. The bonding points were small in area and few in number; thus, upon sectioning

the substrate a few portions of the silicon, together with the Vitre-Graf coating, separated from the substrate. Examination of the edges of sectioned pieces revealed some cracking within the substrate. The cracking could result from a thermal mismatch between the Vitre-Graf coating and the substrate, or it could be that the thicker silicon coating on all surfaces of the substrate is an indication that the thermal expansion coefficient of McDanel MV-20 mullite does not match that of silicon as closely as believed. The latter conclusion is supported by the lack of substrate cracking on a Vitre-Graf coated substrate having a thinner ($\sim 150 \mu\text{m}$) silicon layer grown on all surfaces of the substrate. With thin silicon layers, the silicon rather than the substrate would yield due to thermal stress.

SUBSTRATE CHARACTERIZATION

The Honeywell Chemistry Laboratory used emission spectroscopy to identify the impurities in the following three ceramic bodies:

1. McDanel MV-20 rolled, dried and fired mullite
2. McDanel MV-30 slip cast mullite
3. American Lava hot-pressed mullite

The dominant impurities of interest are Fe and Ti, both known to be detrimental to solar cell performance. As shown in Table 1, the Fe and Ti content in the American Lava pressed mullite is considerably less than in the McDanel compositions. The American Lava, however, contains 72 percent by weight Al_2O_3 and has never been satisfactorily dip-coated with silicon because of its thermal expansion mismatch. Most of the dip coating effort has centered around MV-20 rolled, dried and fired substrate bodies because of their physical properties and cost potentialities. It has not yet, however, been systematically demonstrated that its 0.554/0.42 $\text{Al}_2\text{O}_3/\text{SiO}_2$ composition is the optimum composition.

Table 1. Emission Spectroscopy Chemical Analysis of Various Mullites (Performed at Honeywell)

McDanel (MV-20)		McDanel (MV-30)	American Lava
Fe	0.89 wt%	0.55 wt%	0.75 wt%
Ti	0.78 wt%	0.54 wt%	0.021 wt%
Mg	0.20 wt%	0.13 wt%	0.48 wt%
Ma	0.28 wt%	<0.1 wt%	<0.1 wt%
Ca	0.11 wt%	<0.03 wt%	<0.03 wt%
Mn	0.041 wt%	0.01 wt%	<0.01 wt%
V	0.031 wt%	0.03 wt%	<0.01 wt%
Cu	≤0.01 wt%	≤0.01 wt%	<0.01 wt%

During this reporting period, sections from McDanel's MV-30 large diameter slip cast mullite tubing were also dip-coated without any apparent cracking in either the silicon layer or the substrate. Its Al_2O_3 content, as shown in Table 2, is somewhat larger than that of the MV-20 composition. McDanel Refractory Porcelain Co. has made available to us another higher purity mullite slip cast body (see Table 3). This and other compositions of mullite will be investigated in an effort to determine the $\text{Al}_2\text{O}_3/\text{SiO}_2$ ratio which least stresses the silicon layers.

We presume that the excess SiO_2 in MV-20 and MV-30 is in a glassy phase and that the mechanical properties of the two-phase system are superior to those of the stoichiometric single phase (American Lava sample). It may be that this, rather than simply the expansion coefficient, is the key to dipping compatibility. Porosity and surface textures may also be key factors in determining the coatability of a ceramic, and, if substrates can be obtained, we plan to resolve the relative importance of these factors.

Table 2. McDanel Chemical Analysis of MV20 and MV30 Mullite

Typical Chemical Analysis, McDanel MV-20 Mullite	
Al_2O_3	55.4 wt%
SiO_2	42.0 wt%
K_2O	0.7 wt%
Na_2O	0.5 wt%
CaO	0.1 wt%
Fe_2O_3	0.8 wt%
TiO_2	0.5 wt%
MgO	0.04 wt%
Typical Chemical Analysis, McDanel MV-30 Mullite	
Al_2O_3	60.0 wt%
SiO_2	38.0 wt%
K_2O	0.5 wt%
Na_2O	0.08 wt%
CaO	0.1 wt%
Fe_2O_3	0.5 wt%
TiO_2	0.5 wt%
MgO	0.2 wt%

Table 3. McDanel Chemical Analysis of SA101 Mullite

McDanel SA101	
Calculated Chemical Analysis	
SiO ₂	- 33.30 wt%
Al ₂ O ₃	- 66.60 wt%
Fe ₂ O ₃	- < 0.05 wt%
TiO ₂	- < 0.01 wt%
Na ₂ O	- < 0.04 wt%
K ₂ O	- < 0.01 wt%
CaO	- < 0.03 wt%
Modulus of Rupture	26-30,000 psi
Thermal Expansion	4.8×10^{-6} in/in/°C (25°C - 1000°C)
Bulk Density	2.95 gm/cc
Color	White
Impenetrability	Gas-Tight
Dye Penetration ASTM	Tight
Maximum Working Temp.	1750°C
Thermal Conductivity	18 Btu/ft ² -hr-°F/in at 24°C (est.)

SILICON LAYER CHARACTERIZATION

Electrical Characterization

Earlier in the program, low-temperature infrared spectroscopy was used to determine that some dissolution of the mullite occurs in molten silicon. The aluminum oxide (Al_2O_3) component decomposes, and at least part of the aluminum atoms enter the silicon lattice to become electrically active acceptors. During this reporting period, the extent and the rate of dissolution were examined in a series of experiments using resistivity measurements to determine the aluminum concentration. The extent to which the mullite dissolution can be inhibited by a special graphite coating, namely Vitre-Graf, was also investigated.

A summary of investigative experiments is shown in Tables 4 and 5. Initially, the purity of the dip coating facility was checked by melting an undoped silicon charge and allowing it to remain molten for a period of two hours. Samples were then prepared from the top of the solidified melt and resistivity measurements were made where possible within single grains of silicon. The top of the solidified melt was chosen to be representative of the solidification rates involved in actual dip-coated layers of silicon and thus should more accurately simulate the effects of impurity segregation. The average resistivity of the above melt was 34.5 ohm-cm. All subsequent melt resistivity measurements were made in the same manner.

The above check was repeated except that 5.65×10^{15} boron atoms/cm³ were added to the silicon charge. As expected, this produced a p-type melt sample with a resistivity of 2.5 ohm-cm.

The effect of dissolved ultra pure graphite on the resistivity of the melt was checked by dipping a 0.86-cm diameter rod of this graphite 3.45-cm deep into undoped molten silicon and allowing it to remain for a period of one

Table 4. Electrical Characterization Data of Rubbed-On Graphite-Coated Substrates

Sample	Run-Melt No.	Time* (min)	ρ (ohm-cm)	Comments
Melt No. 28	28	0	34.5	System purity level check (pure silicon molten for 2 hrs. - no dopant - no dipping)
Melt No. 16	16	0	2.5	Dopant level check (silicon molten for 2 hours 5.65×10^{15} boron atoms/cc added - no dipping)
Melt No. 39	39	0	34.0	Ultra pure graphite rod soaked in pure molten silicon for one hour (no dopant - no dipping)
Melt No. 24	24	60	0.5	American Lava pressed mullite substrate allowed to soak 1 hr. in pure molten silicon (no dopant)
MR45	27	2.4	4.0	First dipped substrate in undoped silicon melt
MR47	27	66	0.45	Last dipped substrate in undoped silicon melt
Melt No. 27	27	66	0.45	After dipping MR45, MR46 and MR47 substrates
MR48	29	22	1.45	First dipped substrate in undoped silicon melt
MR52	29	62	0.47	Last dipped substrate in undoped silicon melt
Melt No. 29	29	62	0.47	After dipping MR48, through MR52 (substrates graphite coated on all surfaces)
MR101	45	3.7	9.2	First dipped substrate in undoped melt
MR102	45	7.3	5.6	Second dipped substrate in undoped melt
MR103	45	11.0	4.5	Third dipped substrate in undoped melt
MR104	45	14.7	3.0	Fourth dipped substrate in undoped melt
MR105	45	18.3	2.3	Fifth dipped substrate in undoped melt
Melt No. 45	45	18.3	2.2	After dipping substrates MR101 through MR105

* Accumulated time that respective melts were exposed to mullite.

Table 5. Electrical Characterization Data of Vitre-Graf Coated Substrates

Sample	Run-Melt No.	Time ⁽¹⁾ (min)	ρ (ohm-cm) ⁽²⁾	Comments
MR78-TC	38	60	2.28 WG 1.95 CG	After dipping and soaking 1 hr. in silicon melt doped with 5.65×10^{15} boron atoms/cm ³
Melt 38	38	60	2.48	After dipping substrate MR78-TC
MR97-TC	42	6.16	15.77 WG 8.15 CG	First dipped in undoped silicon melt
MR98-TC	42	66.16	3.23 WG 1.14 CG	Last dipped, after soaking 1 hr. in undoped silicon melt
Melt 42	42	66.16	7.86	After dipping substrates MR97-TC and MR98-TC
MR106-TC	46	6	2.24 WG 0.78 CG	First dipped in silicon melt doped with 5.65×10^{15} boron atoms/cm ³

- (1) Accumulated time that respective melts were exposed to the Vitre-Graf coated mullite substrates.
- (2) WG means resistivity measured with current flow in-line with crystal grains.
CG means resistivity measured with current flow across crystal grain boundaries.

hour. The entire submerged portion of the graphite rod was presumably dissolved by the molten silicon, but it had no effect on the resistivity of the solidified silicon charge.

Another undoped silicon charge was then melted and a 125- μm thick silicon layer was dip-coated on a MV-20 mullite substrate (MR45). Following this, an uncarbonized substrate (MR46) was dipped and soaked in the melt for a period of ~ 63 minutes. A third substrate (MR47) was also dip-coated with a 125- μm thick layer of silicon, and resistivity measurements of the above layers, as well as of the respective melt, were made. The results are shown in Table 4.

The above experiment with a new silicon charge was repeated with substrates which were fully coated with graphite on all sides and edges. The additional graphite, however, caused cooling of the melt and the first dipped substrate (MR48) partially froze in place, so that it was in the melt for 22 minutes. The purpose of this experiment was to determine whether or not the graphite coating on all surfaces would inhibit the dissolution of mullite. As shown in Table 4, the graphite coating neither helps nor hinders the final impurity level of the melt.

It was impossible to repeat the above experiment using American Lava's pressed mullite because of substrate breakage due to thermal expansion mismatch. Therefore, an uncarbonized American Lava pressed mullite substrate was allowed to soak for one hour in yet another undoped molten silicon charge and the resistivity of this solidified melt was taken. Table 4 shows that the impurity level of this melt, as determined from resistivity measurements, is essentially the same as those where McDanel MV-20 rolled, dried and fired substrates were used.

Finally, using another undoped silicon charge, five MV-20 mullite substrates (MR101 through MR105) were progressively dip-coated with silicon layers using identical growth conditions. Their respective resistivities as the melt became progressively contaminated are also shown in Table 4.

Figure 2 is a plot of the resistivity of these various silicon layers and melts as a function of the total accumulated time that the respective melts were exposed to MV-20 mullite. This data is taken from Table 4. It appears as though the aluminum impurity level of the melt increases rapidly during the first two or three minutes of contact time with the substrate, and then increases exponentially at a lesser rate, becoming very nearly saturated after an hour of contact time.

The initial rate of dissolution would be proportioned to the amount of exposed surface area with the rate decreasing as the solution approaches saturation. The effective surface area of the mullite depends on the surface roughness and on the degree of wetting of the substrate. The saturation solubility of the aluminum is determined by the amount of oxygen in the melt. Because of the quartz crucible, the silicon is saturated with oxygen, limiting the amount of dissolved aluminum to a concentration well below the solubility limit of aluminum by itself. Since several chemical reactions are involved, the detailed kinetics are undoubtedly not simple, as indicated by the several slopes in different regions of Figure 2.

Table 5 summarizes the benefit of Tylan Corporation's Vitre-Graf coating on MV-20 substrates for inhibiting the mullite dissolution rate in molten silicon. The results are based on four substrates and are not yet complete, but there is little doubt that they retard the dissolution rate.

Most encouraging was the results of Run No. 38 in which a Vitre-Graf coated substrate was allowed to soak in a boron-doped silicon melt for one hour. The melt was doped to produce a layer resistivity of ~ 2.5 ohm-cm, and after this prolonged soaking period the substrate (MR78-TC) had a uniform p-type silicon layer on all surfaces with a resistivity of 2.3 ohm-cm. The respective melt's resistivity of 2.5 ohm-cm was essentially the same as that measured in the dopant level check of Melt No. 16 (see Table 4).

Figure 2. Layer and Melt Resistivities versus Accumulated Time that the Respective Melts were Exposed to Mullite

Vitre-Graf coated substrates MR97-TC and MR98-TC were then successively dip-coated in an undoped silicon melt. Substrate MR98-TC was allowed to soak in the melt for one hour before it was removed with a smooth, uniform silicon layer. In addition to being listed in Table 5, MR97-TC and MR98-TC layer resistivities are also plotted in Figure 2 for the purpose of comparing them with the more generally used rubbed-on graphite coated substrate silicon layers.

It is interesting to note that for reasons not yet understood and contrary to what is generally expected, resistivities measured on the Vitre-Graf coated silicon layers where the current ran across grain boundaries were substantially lower than those where the current ran along the single grains. This was true on all four of the Vitre-Graf silicon layers, regardless of their impurity levels. This anomaly has been observed in other silicon layers, but never with a definite consistency. The data points shown in Figure 2 are an average for both current orientations.

As reported in an earlier section of this report, sectioning MR78-TC caused portions of the Vitre-Graf silicon layer to separate from the substrate. This made it possible to measure the sheet resistance of the silicon layer as well as that of the attached Vitre-Graf coating. Since the sheet resistance of the silicon layer was ~ 20 times that of the Vitre-Graf, it is evident that some type of conductivity barrier exists between the two. The sheet resistance of Vitre-Graf on the uncoated portion of the dip-coated layer was very similar to that attached to the silicon layer, giving further evidence that little, if any, of the Vitre-Graf coating was dissolved by the molten silicon after soaking in it for a period of one hour.

Chemical Characterization

We have had no results to date from the neutron activation analysis. Some preliminary results from Ion Beam Microprobe work at McCrone Associates are summarized in Table 6. The Na, Mg, Al, Ca and Fe are expected to be present because of the mullite. Mn, V and Cu might also be expected but were not detected. The Fe analysis is complicated by the fact that the Si_2 dimer of silicon has the same mass as Fe and presents an interference.

Table 6. Preliminary Ion Beam Microprobe Analysis

	(Counts/Sec)		
Sample	MR45-3A	MR47	MR12
Background	2-3	2-3	2-3
H	24	100	78
C	5.4	284	30
N	53	260	110
Na	58	316	171
Mg	73.5	28	n. d.
Al	47	290	90
K	59	30	9
Ca	13.5	328	15
$\text{Si}_2 + \text{Fe}$	93	328	105
$\rho(\text{ohm-cm})$	3-5	0.5	1.8
$[\text{Al}] \times \rho$	140-240	150	160
$[\text{Na}] \times \rho$	174-290	158	300
$[\text{N}] \times \rho$	200	130	200

From previous work we are confident that Al is the acceptor responsible for the resistivity. Therefore, the product of the Al concentration and the resistivity should be constant. This is approximately the case as shown by the bottom line in Table 6. Thus, the Al results are as expected. The Na and

N results also correlate well with the Al and resistivity, but the other impurities do not. The Fe results are qualitatively correct, but must be compared to results for pure Si. We are encouraged that this method may be useful in characterizing sheet silicon. To be useful as a quantitative technique, however, the results must be compared by use of bulk standards which are not available. We hope JPL will take action to make standard samples available.

The foregoing results are preliminary and are being rechecked with flat samples that should prevent problems in the instrument. Samples from the same substrates have been sent to Prof. C. T. Sah at the University of Illinois for analysis of recombination centers using transient capacitance spectroscopy.

Structural Characterization

Activity in the area of structural characterization of silicon on ceramic is in the early stages of development. The material has been subjected to the full range of applicable x-ray analytical techniques, but none is an efficiently usable procedure. Briefly, the results are summarized below.

Laue -- The photographs obtained with this procedure using a 1/2 mm collimator usually imaged several grains. It appears that there are enough small grains to interfere with the mapping of the larger grain distribution. The large beam Laue photographs showed the presence of long grains oriented parallel to the growth direction.

Oscillation Camera -- Photographs were obtained with the sample growth direction oriented parallel to the camera rotation axis. If the growth direction is a low index direction, we should detect the layer line structure characteristic of such a direction. No discernible layer line structure was observed.

Texture Camera -- Attempts to obtain pole figures for the various silicon diffraction planes were unsuccessful. The problem is associated with the dwell time at each sampling point. When the spiral sampling plan programmed into the texture camera is used there is insufficient time to record the strong diffraction peaks associated with the large grains. By deactivating the sample rotation the dwell time is increased. This produces a smooth intensity distribution along one radial line of the pole figure. Since many radial lines must be scanned, the total time involved becomes rather high.

Diffractometer -- A normal diffractometer scan gives the intensity of the central point on each of the pole figures of each diffraction line monitored. A more efficient procedure is to fix the diffraction angle and rotate the sample about the diffractometer axis. A radial portion of the pole figure is obtained similar to that described previously with the texture camera. In this case, the sample position relative to the incident and diffracted x-rays changes so that significant absorption effects are encountered. These can be corrected mathematically. With this procedure, many scans are necessary to cover the pole figure for each diffraction line. Thus, the same level of time as the texture camera is required.

Diffractometer measurements on a large grain region of sample MR45 showed that the strongest diffraction peak is from a silicon 220 plane which is about 10° from the sample surface. Similar results were also observed on samples MR5 and MR6. The {110} surfaces have been found to be dominant in the EFG and dendritic material so that it appears to be a general characteristic of sheet-grown silicon.

Channeling Pattern Analysis -- The procedures using the texture goniometer and the modified diffractometer give a statistical distribution of the silicon grain orientations. Other procedures are required to study individual grains. The procedure which can fulfill this need is the electron channeling pattern capability on the SEM. It samples small crystal areas ($\approx 10 \mu$) and displays

a pattern defining the crystal type and orientation. It can be visually interpreted and many crystals could be rapidly sampled to map a given sample. Provided the silicon samples have the necessary perfection levels, this procedure should provide the means by which the structural characterization of the silicon samples can be efficiently achieved.

SOLAR CELL AND PHOTODIODE CHARACTERIZATION

Diode Fabrication

Besides the photodiode made from the dip-coated silicon, two types of control photocells have been fabricated. The purpose of the control cells is to evaluate and optimize our device fabrication procedure, namely the diffusion and the electrical contacting procedure. Because of apparent unresolved discrepancies in the performance of the two types of control photodiodes, it is appropriate to describe the fabrication procedure and performance results in some detail.

The first type of control sample we made was designed primarily to monitor the phosphorus diffusion, and employs a conventional solar cell configuration, shown in Figure 3a. The cells are approximately 0.6 by 1.7 cm in size, with lapped and lightly etched top surfaces and lapped bottom surfaces. Lapping of the top surface is performed before the diffusion. The bottom diffused region is lapped off, and the edges of the top diffused region are mesa etched to decrease shunt resistance. The purpose of the lapping is to facilitate contacts to the n- and p-regions which were made using unsintered electroless nickel coated with indium solder.

Some data for such photodiodes is shown in Table 7. The efficiencies of uncoated cells varies between 8 and 9 percent. In some cases, there have been ceramic substrates in the same diffusion. We point this out because

The dotted lines show the edge of the n-region, defined by mesa etching. The contact label EN(p) means electroless nickel to p-type, and AG(n) means silver paste contact to n-type. When the contact metallization is not specified, it could mean sputtered nickel or silver-titanium, or other contacts to be evaluated.

Figure 3. Photodiode Configurations

of the possibility of cross contamination from the ceramic. As evidenced by the lack of degradation due to the presence of the ceramic, cross-contamination does not appear to be a problem.

Table 7. Control Photodiode Performance

No.	Mullite Present?	Time (Min.)	Temp (°C)	ρ_s ($\Omega/\square$)	V_{oc} (V)	J_{sc} (ma/cm ²)	Eff. (%)	Fill Factor
21	No	21.5	958	10.1	0.549	23.4	9.00	0.706
22	Yes	21.5	960	6.4	0.533	21.4	8.11	0.736
23	Yes	19.0	962	7.0	0.549	21.9	8.87	0.736
24	No	16.0	960	10.1	0.519	23.0	8.93	0.75
24	No	16.0	960	10.1	0.534	22.7	8.68	0.743
25	No	14.0	958		0.524	22.6	8.70	0.75
25	No	14.0	958		0.553	23.1	9.03	0.721
26	No	10.0	958		0.540	23.0	8.90	0.736
29	No	8.0	962		0.539	23.4	8.97	0.720
32	Yes	10.0	958	10.3	0.530	20.6	7.2	0.659
33	Yes	10.0	964	8.9	0.529	20.1	7.16	0.672
34	No	16.0	966	7.9	0.530	26.0	7.76	0.564
35	Yes	31.0	870	12.2	0.535	23.4	5.74	0.459

The second type of control cell is shown in Figure 3b. It is as nearly as possible identical to the silicon-on-ceramic photodiodes, Figure 3c. In this case, the contact to the p-region is made from the front and the contact to the n-region is made with silver paste. The properties of the various types of contacts are discussed in a separate section below. The surface of these diodes is polished and etched rather than lapped and etched. The

performance of the front contact cells has been consistently poorer than that of the conventional geometry, as discussed in the section on photodiode results below. Both V_{oc} and I_{sc} have been consistently low. The reason for this is not clear, but it must be due to either the contacts or the surface preparation. The fill factor is lower too, but this is understandable, because of the increased series resistance in this geometry.

Although we do not understand the reasons for the discrepancies, it is clear that they must be understood because our polycrystalline cells can only approach the performance of the front contact control cell. In an effort to understand the differences, cells having dual geometry, Figure 3d, have been made. One was made with unsintered contacts and the other with sintered contacts. In both cases, the values of V_{oc} were lower than those typical of conventional geometry cells, but higher than those with front contacts only. The values of V_{oc} are always lower (by about 0.02 volt) when the front contact is used in the dual geometry cell.

In the near future, we plan to evaluate the effects of surface preparation and contacts on photodiode performance. We plan to make photodiodes with decreased series resistance using a configuration such as that shown in Figure 3e. For control cells, we plan to make diodes following Figure 3f. This will permit measurement of the voltage drop at the contact, and permit ready evaluation of contact resistance for different types of contact.

Characterization of Electrical Contacts

During this quarter, we began a study to characterize and optimize our methods of making electrical contact. We feel this is important because of the unexplained differences in performance for solar cells made with either top or back contacts to the base region.

We have been using unsintered electroless nickel contacts to the base region. However, the electroless nickel does not consistently adhere to a polished surface or to an as-grown surface. We have found that sputtered nickel contacts show excellent adhesion to any silicon surface. We therefore made up samples of 2 ohm-cm, p-type single crystal silicon with different area contacts arranged so that four terminal contact resistance measurements could be made. The contact current-voltage relationship turned out to be nonlinear, as shown in Figure 4a, with small signal contact resistances in the range of $0.6 \Omega\text{-cm}^2$ for sputtered nickel contacts. Sintering at 450°C reduced the resistance somewhat and reduced the nonlinearity, as shown in Figure 4b. The surfaces in both cases were polished and unetched except for a sputter cleaning to remove oxide.

It was convenient to use a three-terminal method of measurement, as shown in Figure 4e. The voltage probe was either another contact or a tungsten probe with pressure contact to the surface. A voltage follower with an input impedance of 10^9 ohms was used, and it was found that the type of voltage contact made no difference in the results. The signal source was simply 60 cycle current from a filament transformer and variac.

The interesting current-voltage relationships observed with the sputtered contacts are unusual in that the nonlinearity is opposite to that observed for p-n junctions, Schottky diodes, tunneling MOS contacts or other plausible models of the contact behavior.

For comparison, the electroless nickel contacts were also characterized in the same way by use of the two control photodiodes which have the dual geometry shown in Figure 3d. In this case the surfaces were lapped and etched. The unsintered contacts in these diodes were quite poor as determined by visual examination, and as illustrated dramatically in Figure 4c. In this case the nickel acts as a Schottky diode to the p-type silicon shunted by a resistance of about $100 \Omega\text{-cm}^2$. The sintered electroless nickel

a) Unsintered sputtered nickel, $.01 \text{ cm}^2$ 2 ma/div vertical

b) Sintered sputtered nickel, $.01 \text{ cm}^2$ 5 ma/div. vertical

c) Unsintered electroless nickel, $.18 \text{ cm}^2$

d) Sintered electroless nickel, $.28 \text{ cm}^2$

(e)

Figure 4. Contact Current-Voltage Relationships and Method of Measurement

contact showed much lower small signal resistance of 0.9 ohm-cm^2 (Figure 4d) but still higher than that of the sputtered contacts. Actually, the contact resistance could be somewhat less than this because of spreading resistance in the base. It is interesting that the sintered contact again shows the nonohmic behavior of the sputtered contacts.

Work will continue in an effort to further characterize electrical contacts, the effect of surface preparation, and the effects on the solar cell performance. At any rate, our measurements strongly suggest that the contact resistance cannot be simply represented by a linear resistor in the equivalent circuit of a solar cell.

In addition to the nickel contacts to p-type silicon, the silver paste top contacts to the n-type regions have also been evaluated by the same method. These have been found to be consistently in the range of 0.5 ohm-cm^2 , about the same as that of the nickel contacts. On the other hand, silver paste contacts to the p-region form a Schottky barrier with a high barrier height, much worse than a tungsten pressure contact which has a lower barrier height.

In order to continue to evaluate our contact quality we plan to make control cells with the geometry of Figure 3f, as discussed above. In this way we can develop confidence that contact problems are not affecting our material characterization.

Photodiode Modeling

The fabrication procedure for the silicon-on-ceramic photodiodes and for the control cells has been discussed in some detail above. We have continued to see improved diode performance as the amount of mullite dissolved in the silicon has been reduced. In order to increase the accuracy

and reliability of the cell parameters deduced from the photodiode data, a computer program for fitting the data has been developed, based on an electrical equivalent circuit of the photodiode.

The Equivalent Circuit -- A solar cell is often represented as a photocurrent generator in parallel with one or two diodes, which together with series and shunt resistances make up the equivalent circuit of Figure 5.

Figure 5. Photodiode Equivalent Circuit

The left-hand diode represents the main complement of the junction current and I_1 ideally satisfies

$$I_1 = I_{10}[\exp(B_1 V_D) - 1] \quad (1)$$

with $V_D = V - IR_s$. If, for example, this is injected current, then $B_1 = q/kT$. In some devices a second distinct current component can be represented according to

$$I_2 = I_{20}[\exp(B_2 V_D) - 1] \quad (2)$$

where $B_2 < B_1$. This could represent generation-recombination or some other junction current mechanism.

According to the equivalent circuit, the current I into the device should satisfy

$$I = [-I_{ph} + I_1 + I_2 + V/R_{sh}]/[1 + R_s/R_{sh}]. \quad (3)$$

With this sign convention for I , the dark I - V characteristic ($I_{ph} = 0$) appears in the first and third quadrants while the illuminated ($I_{ph} > 0$) characteristic occupies principally the fourth quadrant.

Seven-Parameter and Five-Parameter Models -- A measurement run on a particular device provides a set of V , I pairs to which we would like to fit the model represented by Figure 5 and Equations (1) - (3). In the full model this is accomplished by systematically manipulating the seven adjustable parameters until the sum of the weighted squared differences between measured and calculated currents is minimized. For convenience in programming, the parameters are identified in an array P as follows:

$$P_1 = I_{ph}$$

$$P_2 = I_{10}$$

$$P_3 = B_1$$

$$P_4 = I_{20}$$

$$P_5 = B_2$$

$$P_6 = R_s$$

$$P_7 = R_{sh}$$

Some sets of data are adequately represented by a model containing one diode, and including a second diode does not significantly improve the least squares fit. For these cases the five-parameter model is used; that is, with P_4 and

P_5 held equal to zero. When the seven-parameter model is applied to this type of data, the nonlinear least squares method would have difficulties because the linearized normal equations are linearly dependent.

Parameter Calculations -- A computer program was written to minimize Q with respect to the parameters P_1 through P_7 :

$$Q = \sum_{k=1}^K W_k \cdot (I_k - Z_k)^2, \quad (4)$$

where the index k ranges over the K data points (typically K is between 15 and 30), W_k is the k^{th} weighting factor, I_k is the measured current and Z_k the calculated current. Since the parameters appear nonlinearly in the calculations, a nonlinear least-squares procedure^{1,2} is employed. This uses repeated linearization with restricted parameter movement at each step. The logical flow for these iterations is shown in Figure 6.

Weights are selected by different rules depending on whether the data are for the dark or illuminated characteristic. Currents measured in the dark are taken with both forward and reverse voltages, and their absolute values range over many orders of magnitude. Thus, for the dark data, it is appropriate to choose the weighting to minimize relative errors:

$$(\text{dark}) \quad W_k = (|I_k| + \epsilon)^{-2} \quad (5)$$

where ϵ is a small positive constant included to avoid dividing by zero. The situation is different for the illuminated data, because it is not necessary to change scales on the measuring instrument in going from the highest to

¹ K. Levenberg, Quart. Appl. Math. Vol 2, p. 164 (1944)

² R. A. Stryk, Ph.D. Thesis, University of Minnesota (1967)

Figure 6. Nonlinear Least-Squares Iterative Procedure

lowest currents. Hence a constant weight is employed in the calculations:

$$(illumined) W_k = 1.0 \quad (6)$$

Calculation of Z_k -- The current calculation from Equations (1) - (3) is complicated by the fact that the diode voltage V_D itself depends on the current via the series IR drop. In other words, the current is expressed as a nonlinear function of V , the parameter P , and itself:

$$Z_k = f(V_R, P, Z_k). \quad (7)$$

The subroutine FUNF calculates each Z_k recursively, as shown in Figure 7. Starting with I_k as a first estimate of Z_k , the error $E = Z_k - f(V_R, P, Z_k)$ and its analytic derivative $\frac{\partial E}{\partial Z_k}$ are calculated. A new estimate is made and the procedure is repeated until E is within the accuracy tolerance. This method converges rapidly, whereas the more direct method of proceeding to the (n+1)st estimate by means of

$$Z_k^{(n+1)} = f(V_R, P, Z_k^{(n)}),$$

was found to diverge.

The matrix of partial derivatives $\frac{\partial Z_k}{\partial P_j}$ (the array DER) is then calculated for use in the least squares linearizations.

Shunt Circuit Current, Open Circuit Voltage, Fill Factor and Efficiency --

Having found the optimum seven-parameter or five-parameter fit to the illuminated data, the program then proceeds to calculate solar cell performance parameters. Additional data needed for these calculations are the illumination intensity $I(\text{mv}/\text{cm}^2)$ and the active device area $A(\text{cm}^2)$.

The short-circuit current is the (recursive) solution of

SUBROUTINE FUNF(V,I,P,Z,DER)

Figure 7. Flow Diagram for Calculating Z and DER (Subroutine FUNF)

$$I_{SC} = f(O, P, I_{SC}) \quad (8)$$

whereas the open-circuit voltage satisfies

$$O = f(V_{OC}, P, O) \quad (9)$$

To determine the fill factor it is necessary to find the values $V = V_m$ and $I = I_m$ which maximize the power

$$\omega = |V \cdot f(V, P, I)| \quad (10)$$

subject to $I = f(V, P, I)$. The maximizing point satisfies the conditions

$$\frac{d\omega}{dV} = I_m + V_m \cdot \frac{\partial f}{\partial V} / (1 - \frac{\partial f}{\partial I}) = 0 \quad (11)$$

$$I_m = f(V_m, P, I_m).$$

The fill factor and efficiency are

$$F.F. = I_m V_m / I_{SC} V_{OC} \quad (12)$$

$$Eff. = I_m V_m / A\ell.$$

Photodiode Results

The measured results and the computer fits to the data are shown in Figures 8 - 12. The figures show the measured data as dots on the lower curve. These curves were all fit with a single exponential diode characteristic (a five-parameter fit), and the fit, shown by the lower curve, is quite good, usually within the accuracy of the data. The solar cell parameters of interest are given in the lower part of each figure.

Figure 8. I-V Characteristics of MR45B-2

Figure 9. I-V Characteristics of MR45B-3

Figure 10. I-V Characteristics of SC-27-1

Figure 11. I-V Characteristics of R78-33-7

Figure 12. I-V Characteristics of R78A-33-5

The upper curve in Figures 8 - 12 shows the calculated curves corrected for reflectivity loss (assumed to be 40 percent) and series and shunt resistance. These corrections are quite sizable and the corrected efficiency (inherent efficiency) is nearly twice the measured efficiency.

Figures 8 and 9 show photodiode characteristics for two small photodiodes from substrate number MR45. The melt in this case was not boron-doped so that only the aluminum from the dissolved mullite was the shallow acceptor dopant. These were small area photodiodes covering a single grain. A larger photodiode covering numerous grains had a lower efficiency and was used in a preliminary EBIC study reported below.

By comparison with the silicon on ceramic photodiodes, the control single crystal photodiodes made during the same diffusion run (SC-27) had essentially the same performance. Figure 10 shows a fit to one of the control photodiodes. The other photodiodes had V_{oc} values of 0.46 to 0.47 volt. Although the areas were not accurately measured in all of the other control diodes, their short circuit current density appeared to be quite uniform. Unfortunately, the conventional geometry control cell for SC-27 was destroyed in processing, but would very likely have had an efficiency of 8 - 9 percent as the other cells in Table 7.

As we have previously mentioned, the reason for the differences between control cells is not known, but must be one of the following:

1. Contacts
2. Surface preparation
3. Cross-contamination from the ceramic
4. A geometrical difference

All of the foregoing possibilities are being investigated, and we hope that understanding the problems will provide solutions that will give significantly improved photocells on the ceramic as well as the front contact control cells.

Some improvement in photodiode performance is obtained when the melt is protected from dissolution of the mullite. Data for two diodes from MR78-TC are shown in Figures 11 and 12. Again, there are small area diodes on single grains. The melt in this case was boron-doped and the ceramic had the Vitre-Graf coating which prevented dissolution of the mullite. The control photodiodes in this case were the dual geometry diodes used for control studies as discussed above and atypical poor photodiode performance.

In summary, diode performance has improved as contact of the melt to the mullite has decreased. The performance of small photodiodes on single grains is essentially the same as that of single crystal photodiodes made in the same way.

Preliminary EBIC Results

During this month, we made some preliminary EBIC measurements. A photodiode PPD10-1 from substrate number MR45 was fabricated by our usual procedure with an angle-lapped electroless nickel base contact and silver point contact to the n-region. The diode covered several large grains and an apparently small grain region, and had an uncorrected efficiency of only 1.5 percent. The EBIC image shown in Figure 13 taken at a beam voltage of 25 kV showed surprisingly uniform response over the entire mesa diode, whereas we would expect to see dark regions at the grain boundaries. Perhaps at lower voltages the nonuniformities would be evident. At higher magnification (Figure 13, lower right), the edge of the diode showed a

DIODE PPD-10-1
R45A-27-1

14X OPTICAL IMAGE

15X EBIC

Figure 13. Preliminary EBIC Measurement on Photodiode PPD 10-1.

streaking character that we believe is due to the diffusion of minority carriers generated by the electron beam. Thus the length of the streak should indicate the minority carrier diffusion length, L_D if the effects like surface recombination can be neglected. A rough estimate from the figure gives $L_D = 25 \mu\text{m}$. Although this diffusion length and the diode uniformity are encouraging, they seem to be inconsistent with the diode short circuit current and efficiency numbers.

CONCLUSIONS

During this past quarter of work, the following conclusions have been reached:

1. Based on the numerous substrates dip-coated to date, and given the thermal characteristics of the present dip coating facility, pulling rates of 5 to 7 cm/min are most likely to produce layers of the crystalline quality necessary for high efficiency solar cells. A dip coating facility temperature controller with superior settability is needed to complete the layer growth parameter study at temperatures near the melting point of silicon.
2. The angle-dipped layers were qualitatively similar to the vertical dipped layers, but show some potential for improved coating uniformity.
3. The dip coating process will likely require a mullite substrate with a composition containing an excess of SiO_2 in order to match the thermal expansion coefficient of silicon.
4. McDanel Refractory Porcelain Company's MV30 slip cast mullite bodies apparently also qualify as a candidate substrate material for the dip coating process.
5. Tylan Corporation's Vitre-Graf coatings on mullite substrates show wettability to molten silicon comparable with the rubbed-on graphite coatings generally used during this research program. They also show considerable promise toward inhibiting dissolution of the mullite substrate in the silicon melt. This is particularly true when their contact time with the melt is no greater than needed to produce good dip-coated silicon layers.

6. Rubbed-on ultra pure graphite substrate coatings which dissolve in the melt during the dip coating procedure have no effect on the resistivity of dip-coated silicon layers.
7. Rubbed-on ultra pure graphite substrate coatings apparently do little to inhibit the dissolution of the mullite substrate during the dip coating process.
8. The dissolution rate of American Lava Company's hot-pressed mullite is essentially equivalent to McDanel's MV20 composition.
9. Based on a preliminary Ion Beam Microprobe analysis, the Al concentration found in three samples of dip-coated silicon layers was approximately related to their measured resistivities.
10. Structural characterization of dip-coated layers shows some indication that the orientation is similar to that observed in ribbon growth.
11. Improved solar cell performance is probably a result of using silicon layers with a lower content of dissolved mullite.
12. Control photodiodes with front surface contacts to the base region show consistently poorer performance than cells fabricated by conventional geometry. In many cases the performance of such cells is no better than that of the silicon-on-ceramic cells.
13. Sintered nickel contacts have low contact resistance but exhibit a surprising nonlinearity which is opposite to a diode characteristic. As long as the contact resistance is low enough, the nonlinearity is immaterial.
14. Preliminary EBIC results have shown encouraging results regarding diffusion lengths, but these results must be verified with further measurements.

RECOMMENDATIONS

The following recommendations are made to improve the effectiveness of the present research program:

1. It is recommended that the present dip coating facility be modified as follows:
 - a. Replace the present temperature controller with an expanded scale model to improve the temperature settability near the melting point of silicon.
 - b. Install an additional thermocouple for readout purposes. This permits the present thermocouple to function solely as a temperature control thermocouple and eliminates any possible interference from temperature monitoring instruments.
 - c. Install an argon gas purifier to reduce generation of SiO.
 - d. Install timer clock valves on the water and gas supplies. This will make it possible to operate the facility for a larger portion of the working day by permitting it to be automatically shut down after working hours.
2. It is recommended that narrower rolled, dried and fired mullite substrates be procured. The periphery of the silicon melt is first to solidify, presumably due to the thermal gradient across its surface. Narrower substrates should permit growth studies in a more uniform temperature zone of the melt.
3. It is recommended that a design for a new continuous coating facility be initiated. This facility will demonstrate the scale-up potentiality of silicon coated ceramic sheets and permit further studies of the crystalline growth development by using longer substrates. Further, it will permit the substrate to have less

contact area with the molten silicon, reducing substrate dissolution, and will be designed to completely eliminate progressive contamination of the melt.

4. Larger ceramic substrates must be procured for use with the new facility.
5. It is recommended that a scale-up cost potential study of the dip coating and coating processes be initiated.

NEW TECHNOLOGY

There have been no reportable "New Technology" items uncovered during this reporting period.

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PROJECTED ACTIVITIES FOR NEXT QUARTER

In addition to initiating action on the tasks listed under "Recommendations," the following tasks will be pursued during the forthcoming quarter:

Layer Growth

1. Layer thickness as a function of pulling rate will be further evaluated at additional temperatures.
2. The study of a constant pulling rate at various temperatures as a function of layer thickness and surface morphology will be completed.
3. The substrate angle dipping study will be continued.
4. Dip-coated layer seeding experiments will be performed.
5. The role of impurities and constitutional supercooling in the growth process and as a limitation to growth rate will be looked at, at least qualitatively.

Substrate Characterization

1. The following methods for precarbonizing ceramic substrates will be investigated:
 - a. Utilization of the organic binders by firing in an inert or reducing atmosphere.
 - b. Carbonization of one face by impregnating one surface with graphite powder, followed by an inert or reducing atmosphere firing.
 - c. Carbonizing the entire substrate by mixing ceramic powders with graphite powders, followed by an inert or reducing atmosphere firing.

- d. Incorporation of SiC in one face of the substrate.
2. Purer mullite substrates of various Al_2O_3/SiO_2 compositions will be investigated for minimizing stress within the silicon layers. This will also help to identify the effect of higher purity on solar cell performance. The extent of these studies will be determined by the availability of substrates.

Material Evaluation

1. The inhibiting effect of Vitre-Graf coated substrates on the dissolution of mullite will be further studied.
2. The Ion Beam Microprobe analysis and Neutron Activation analysis results will be reviewed and reported.

Solar Cell Fabrication and Evaluation

1. Solar cells will be fabricated from Al-doped single crystal silicon to further explore the adverse effects of Al as an acceptor atom.
2. Lower temperature p-n junction diffusion will be investigated.
3. Greater numbers of larger area solar cells, as well as photodiodes both fabricated on high purity mullite substrates, will be fabricated and evaluated.
4. Minority carrier diffusion lengths will be measured by EBIC, as well as by the surface photo-voltage techniques.
5. Special geometry cells will be fabricated to enable more quantitative evaluation of contact resistance for different type contacts and surface preparations.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Fig. 14, 15, and 16.

NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE RESEARCH CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

△ - PLANNED GOALS
▲ - ACCOMPLISHED GOALS

* STARTING DATE 10/21/75

Figure 14. Updated Program Plan

Figure 15. Updated Program Labor Summary

Figure 16. Updated Program Cost Summary