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(Vol. 1)

ORELA Data Acquisition System Hardware

Vol. 1: Introduction

J. W. Reynolds

OAK RIDGE NATIONAL LABORATORY

OPERATED BY UNION CARBIDE CORPORATION FOR THE ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION

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INSTRUMENTATION AND CONTROLS DIVISION

ORELA DATA ACQUISITION SYSTEM HARDWARE

Vol. 1: Introduction

J. W. Reynolds

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Other volumes in this series of reports on *ORELA Data Acquisition System Hardware* are:

ORNL/TM-5639 (Vol. 2 of ORNL/TM-5638)	Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)
ORNL/TM-5640 (Vol. 3 of ORNL/TM-5638)	Scaler Interfaces (Q-5036-1, -2, -4 through -11, -29, and -30)
ORNL/TM-5641 (Vol. 4 of ORNL/TM-5638)	ORELA Device Controllers (Q-5098)
ORNL/TM-5642 (Vol. 5 of ORNL/TM-5638)	SEL 810B/PDP-4/PDP-9 Intercomputer Link
ORNL/TM-5643 (Vol. 6 of ORNL/TM-5638)	Eight-Stage Stacking Buffer Memory (Q-5066)
ORNL/TM-5644 (Vol. 7 of ORNL/TM-5638)	Instruction Manual for the Multiplexer Channel and Scaler Interface Tester (Q-5130)
ORNL/TM-5645 (Vol. 8 of ORNL/TM-5638)	Instruction Manual for the Ground Isolation Driver and Receiver Cards on the Quiet Ground System at ORELA

CONTENTS

	<u>Page</u>
ABSTRACT	v
1. INTRODUCTION	1
1.1 Oak Ridge Electron Linear Accelerator Facility . . .	1
1.2 ORELA Data Handling System	1
2. ORELA DATA ACQUISITION	5
2.1 Acquisition of Data	5
2.2 On-Line Examination of Data	7
2.3 Experiment Control and Monitoring	8
2.4 Peripheral Support of Data Acquisition	8
2.5 Ground Isolation at the ORELA Facility	10
2.6 Cabling of the ORELA Data Acquisition System	13
3. DATA ACQUISITION AND COMMUNICATION PERIPHERALS	13
3.1 Word-Addressed Fixed-Head Disk (WAFHD)	14
3.1.1 Disk Operation	15
3.2 Four-Channel Priority Multiplexer (FCPM)	19
3.2.1 Multiplexer Operation	20
3.3 Cathode-Ray Tube Display (CRTD)	23
3.3.1 CRTD Operation	23
3.4 Scaler Interface and Device Controllers	25
3.4.1 Scaler Interface Operation	25
3.4.2 Device Controller Operation	29
3.5 Intercomputer Links	32
3.5.1 Link Operation	32
3.6 Binary Synchronous Communications Interface (BSCI) .	33
4. REVIEW OF MODIFICATIONS TO THE SEL 810B COMPUTER FOR THE ORELA DATA ACQUISITION SYSTEM	34
4.1 Modifications to the CPU	34
4.1.1 Special Modifications by SEL	34
4.1.2 System Modifications by ORNL	35
4.1.3 Special Interrupts	36
4.1.4 Disk Initialize Complete Interrupt on the DACs	36
4.1.5 BTC Word Count Equal Zero Control on the PEC and DAC 3	36
4.2 Modifications to Standard Peripherals	37
4.2.1 Magnetic Tape Controller	37
4.2.2 Intercomputer Link	38
4.2.3 Line Printer	39
4.3 Modifications to Nonstandard Peripherals	39
4.3.1 Disk Revolution Not Used Interrupt on the Word-Addressed Fixed-Head Disk	39
4.3.2 Cathode-Ray Tube Display	40
4.3.3 Binary Synchronous Communications Interface .	41
4.3.4 Four-Channel Priority Multiplexer	41
4.3.5 Scaler Interface	41

	<u>Page</u>
5. ORELA DRAWING SERIES	42
5.1 Q-2928, ORELA Data Acquisition	42
5.2 Q-2956, PDP-4 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link	42
5.3 Q-3079, ORELA Digital Multiplexer, Level Matching	42
5.4 Q-5036, Scaler Interface and Four-Channel Priority Multiplexer	42
5.5 Q-5066, Eight-Stage Stacking Buffer Memory	43
5.6 Q-5072, PDP-9 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link	43
5.7 Q-5094, Ground Isolation Receiver and Driver Tester	43
5.8 Q-5098, ORELA Device Controller	44
5.9 Q-5108, Binary Synchronous Communications Interface (SEL 130-100500-000)	44
5.10 Q-5109, ORELA Isolated Pulse Generator	44
5.11 Q-5110, ORELA Digital Multiplexer, Level Matching	44
5.12 Q-5130, ORELA Data Acquisition, Multiplexer-Scaler Tester	45
5.13 Q-5183, Word-Addressed Fixed-Head Disk Logic (SEL 53335)	45
5.14 Q-5184, 810B I/O Expander (SEL 53344)	45
5.15 Q-5185, Cathode-Ray Tube Display (SEL 53351)	45
5.16 Q-5186, PEC/DAC 2 or PEC/DAC 3 Intercomputer Link (SEL 53360)	45
5.17 Q-5187, 810B/PDP-4 Intercomputer Link (SEL 53422)	46
5.18 Q-5188, PEC/DAC 1 Intercomputer Link (SEL 53425)	46
5.19 Q-5193, Automatic Update WAFHD (SEL 160-100835-000)	46
6. ENGINEERING DRAWINGS	46
APPENDIX A. DRAWING LISTS FOR ORNL INSTRUMENTATION AND CONTROLS DIVISION DRAWING SERIES USED AT ORELA	57
APPENDIX B. PERFORMANCE SPECIFICATIONS AND RELATED DOCUMENTS FOR THE ORELA DATA HANDLING SYSTEM	72
APPENDIX C. COMPUTER HARDWARE CONFIGURATION	74
APPENDIX D. TECHNICAL, DESIGN, OPERATION, AND MAINTENANCE MANUALS FOR THE ORELA DATA ACQUISITION SYSTEM	76
APPENDIX E. PROGRAMMING NOTES FOR ORELA	79

ABSTRACT

This report introduces the ORELA Data Acquisition System and reviews with a minimum amount of detail the component parts of the system, which are described with engineering and design details in Vols. 2-8 of this report. Each specifically designed piece of hardware is briefly described with a simplified block diagram. Modifications to standard peripheral devices are reviewed. A list of drawings and programming notes are also included.

1. INTRODUCTION

1.1 Oak Ridge Electron Linear Accelerator Facility

The Oak Ridge Electron Linear Accelerator Facility (ORELA) has been specifically designed as a facility for neutron cross-section measurements by the time-of-flight technique. ORELA differs from existing electron accelerators in two ways.

The facility was designed to produce high-intensity bursts of neutrons. The electron linear accelerator routinely produces 1000 bursts/sec of 140-MeV electrons with a pulse duration as short as 2.3 nsec. At the peak current of 15 A, the neutron production is 10^{10} neutrons per burst for the shortest bursts.¹

Second, ORELA was designed so that a number of cross-section experiments can be performed simultaneously. This goal of simultaneous operation of several experiments, a maximum of six to date, has been achieved by using the multiple flight paths radiating from the target room (see Fig. 1 for a physical location), the multiple flight stations on each flight path, the laboratory facilities surrounding the central data area, and a shared data acquisition computer system. (The accelerator control console is at the west end of the central data area.)

The flight stations contain the fast electronics for initial processing of the nuclear detector signals on a time scale of nanoseconds. The laboratories, and in some cases the flight stations, contain the equipment to digitize the nanosecond detector signals on a time scale of a few microseconds. At this point, the data passes into the ORELA Data Acquisition portion of the ORELA Data Handling System.

1.2 ORELA Data Handling System

The ORELA Data Acquisition System in the central data area stores these signals on a time scale of tens of microseconds for examination by a physicist on a time scale of a few minutes, hours, days, or possibly a week. The facility is available for data acquisition 24 hours a day,

Fig. 1. 'Oak Ridge Electron Linear Accelerator Facility.

seven days a week, except during periods of scheduled accelerator maintenance, which occur for approximately two days every fourteen days of operation.

The data acquisition system supplies data by a fast intercomputer link to an interactive analysis system where the stored data undergoes numerical manipulation and graphical interpretation to provide interim results necessary to evaluate the course of the experiment. Finally, a detailed numerical analysis is provided, leading to published tables, graphs, and comparisons with theory on a time scale of a few days to several months.

A block diagram of the ORELA Data Handling System is given in Fig. 2. The shaded blocks in the upper left corner, except for Data Acquisition Computer System 5 (DAC 5), make up the ORELA Data Acquisition System, which will be examined in further detail. The ORELA Immediate Analysis System consists of the Display Stations and Remote Terminals in the lower left corner, supported by a PDP-10 Time-Sharing System (on the right of Fig. 2) with 10^8 channels of on-line disk storage for the data sets from ORELA. The PDP-10 system also performs a communications coordinating function² for the Systems Engineering Laboratories, Inc. (SEL) 840A (DAC System 5) and an IBM 2780 Data Terminal at the Oak Ridge Y-12 Plant to either an IBM 360/75 or 360/91. The two IBM computers are also used for calculations that are more efficiently performed by the larger computers in support of ORELA data analysis.

A brief overview of the major features of the ORELA Data Acquisition³ hardware is presented in the next section, beginning with acquisition of data, experiment control and monitoring, peripheral support of data acquisition, the quiet ground and ground isolation system, and the cabling at the ORELA Facility. Volumes 2 through 8 of this report, which furnish further details on logical units of the data collection equipment, are referenced in Sects. 3 and 5 of this volume.

Section 3 contains block diagrams, programming information, and a brief functional description of the special peripheral devices designed for ORELA.

Section 4 is a review of the modifications to the component parts of the ORELA Data Acquisition System.

Fig. 2. ORELA Data Acquisition and Handling System.

Section 5 provides a quick reference to the ORNL Instrumentation and Controls Division Drawing Series used at ORELA, with references to Vols. 2 through 8 as they apply to a particular drawing series. A list of drawings for each series is contained in Appendix A. Section 6 contains the individual drawings which are cited and discussed in this volume.

Appendix B contains a list of hardware for the DACs and Peripheral Equipment Controller (PEC).

Appendix C contains a list of specifications and related documents for the ORELA Data Handling System.

Appendix D contains a list of technical, design, operation, and maintenance manuals by SEL and other manufacturers for the peripherals attached to the ORELA Data Acquisition System.

Appendix E contains programming notes for each nonstandard peripheral in the ORELA Data Acquisition System. A table of Block Transfer Control (BTC) and interrupt location assignments are included. The current lists of BTC and Priority Interrupt Assignments are available on the PDP-10 Data Analysis System with file identifiers SELBTC.LST[106,1006] and SELPIA.LST[106,1006].

2. ORELA DATA ACQUISITION

2.1 Acquisition of Data

In order to fully utilize the resolution available in the time-of-flight and pulse-height information, a data acquisition facility with a storage capacity of 2.1×10^6 channels of count information (65,535 counts per channel) has been designed and placed in operation. The storage capacity of 2.1×10^6 channels is divided among three semi-independent DAC systems with approximately 7.4×10^5 , 3.5×10^5 , and 10^6 channels in each system. The systems are referred to as DAC 1, 2, and 3 respectively (see Fig. 3 for a block diagram of a DAC). Appendix B includes a list of hardware. Data is stored on a uniquely controlled Word-Addressed Fixed-Head Disk (WAFHD) (Sect. 3.1). Each system also stores a maximum of 44,544 words of programming in up to 87 packages

Fig. 3. ORELA Data Acquisition Computer.

that are retrievable by name. These packages, typically 512 words in length, are organized into the ORELA Data Acquisition Monitor System.⁴ A software-limited subset of these packages is referred to as ORELA Data Acquisition Routines (ODAR).

Data streams with system data rates up to 8000 events/sec containing 30 bits of binary information per event can be sorted and stored in the 10^6 channels of DAC 3, whereas the other two subsystems are restricted to a system data rate of 5000 events/sec. The DAC 3 disk is an automatic update version of the disks on DAC 1 and 2. The system data rate is defined as the number of events per second that are stored on the WAFHD (by incrementing the contents of randomly chosen disk addresses) after an experimenter's input data passes through his CRUNCH⁴ routine. An experimenter's CRUNCH routine, consisting of several packages as required by each experiment, reduces each event to a track number and track position for disk storage by incrementation of a channel. The system data rate is shared by a maximum of four experimenters who have their digitized time and/or pulse-height data connected to the Four-Channel Priority Multiplexer (FCPM) (Sect. 3.2) on each DAC. The experimenter's data rate may be either less than or greater than the system data rate if multiple storages are executed for each event or data are presorted for areas of interest. The Experimenter's Equipment Block Diagram on ORNL Dwg. No. Q-2928-5* illustrates the types of equipment that have been connected to a multiplexer channel. (Note that the drawing number within the block gives the dash number of the circuit diagram within the drawing series.)

2.2 On-Line Examination of Data

During data acquisition, experimenters can view their data (ODAR Dispatch Routines, App. E restrict access) on an 8- by 10-in. Cathode-Ray Tube Display (CRTD) (Sect. 3.3) under control of a display program. Data from any of the three DACs can be shown on the display attached to a particular DAC. The display program produces a linear or semi-logarithmic display of a maximum of 512 channels of data. Such functions as expansion and contraction of the X and Y axes, changing between a

* See Sect. 6, Engineering Drawings, for the Q-drawings cited in this volume.

linear and semi-logarithmic display, starting and stopping a scan of the experimenter's data, initializing the display to a selected portion of the data, generating a dual display for comparison of two spectra, and typing the neutron or gamma energy of a selected channel is accomplished either with "light buttons" (see Appendix E Programming Notes 6CRT Light Pen Function Points) selected by a light pen attached to the display or by typing a command string (see Appendix E Programming Notes Cathode-Ray Tube Display, 6CRT Teletype Commands) on the console teletype. The raw data is transferred from the disk to a buffer area in core memory where it is represented by display control words. A block transfer control channel (direct memory access) is then used to cyclically transfer this display information core buffer to the display control unit without further program intervention.

2.3 Experiment Control and Monitoring

The large number of channels available to an experimenter allows sets of data such as sample-in and sample-out to be taken through manual or automatic control. The automatic control and monitoring are achieved through a control program operating a Device Controller (Sect. 3.4) attached to the Scaler Interface (Sect. 3.4). Each experimenter may have a Device Controller that has been customized for personal application while sharing the access to the Scaler Interface with a maximum of three other experimenters. The Experimenter Equipment Block Diagram (Dwg. No. Q-2928-5) illustrates the types of equipment that have been connected to a Device Controller.

2.4 Peripheral Support of Data Acquisition

The three DACs are connected to a PEC (see Fig. 4) through three intercomputer links (Sect. 3.5). The PEC provides services to the DACs, such as a card reader to read cards for setting up parameters for a run of data, a line printer to provide listings of the data setup and partial listings of the raw data, a Calcomp X-Y plotter to provide plots in either point or histogram modes with linear or semi-logarithmic scales,

Fig. 4. ORELA Peripheral Equipment Controller.

two nine-track magnetic-tape drives for storage of raw data during and at the end of a run, and a Binary Synchronous Communications Interface (BSCI) (Sect. 3.6) for transfer of raw data to an interactive display system for immediate analysis. (See 7XXX Experimenter's Dispatch Routine in Appendix C for the functions that are used by most experimenters. A particular experimenter's initials replace the XXX in actual use.) The Immediate Analysis and Coordinating Computer (IACC), a PDP-10, and its associated peripherals (see Fig. 2) provide the capability of preliminary analysis of the data during the experiment by means of three interactive display stations and three remote time-sharing Keyboard Send Receive (KSR) terminals.

2.5 Ground Isolation at the ORELA Facility

A single-point ground philosophy was adopted for ORELA and was included in the construction as a 40- by 80-ft ground mat located under the accelerator and modulator rooms. The ground mat consists of a matrix of 4/0 copper cable on 1-ft centers that is welded at all intersections around the outside of the mat and at a maximum distance of 6 ft between welds within the mat area. (Figure 5 shows a view of the mat.) Two ground connections are brought above ground, one for the accelerator and one for the quiet ground to the experimenters. The quiet ground to the experimenters is continuously monitored for an indication of current flow above a background level. An excessive current condition is indicated on an annunciator panel at the accelerator control console.

The quiet ground isolation system for the laboratory area of the ORELA Facility is shown in schematic form on Dwg. No. Q-2928-14 as an overlay on the building floor plan. The copper ground plates in each laboratory are shown at their approximate physical location. (The routing of the 2/0 ground cables between the common ground plate in Lab I and the individual laboratories does not follow the actual wiring.) The points of isolation between the experimenters and the computer data acquisition system are indicated by symbols, as shown in the legend on the right of the drawing. Each of the ground cables from the experimenters can be checked with a ground current monitor for local loops

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Fig. 5. ORELA ground mat looking east with modulator pits in center of mat.

between experimenters; for the case of excessive current in the common connection, the monitor can be used to isolate the cause. This feature has already proven itself in isolating a fault when the power ground in a Nuclear Instrument Module (NIM) bin was pinched, allowing a short to building ground.

The isolation of each signal line to and from the DAC is accomplished by using a signal-powered proprietary circuit of the Iso-Switch Corporation. The following information and figure are taken from their data sheet.⁵

The Iso-switch is a true 4-terminal device (2 input terminals and 2 output terminals). No power supply is required. It uses a high efficiency oscillator, powered only by the digital signal input itself, to transfer energy across an isolating transformer and into a detector. The isolated DC output of this detector is used to control the base-emitter junction of the output transistor switch.

Interface to DTL/TTL is illustrated for clarification only. Note that the IC is connected as a *sink*; not as a source.

See the circuit diagrams (Dwg. Nos. Q-5036-25 and 30) for the FCPM and Scaler Interface isolation, respectively, for the isolation details of each piece of equipment. Volume 8 of this report contains schematics of the ground isolation and receiver cards (part of Drawing Series Q-5072) and Instruction Manual for a Ground Isolation Driver and Receiver Card Tester (Drawing Series Q-5094).

2.6 Cabling of the ORELA Data Acquisition System

A floor plan of the computer equipment at ORELA is on Dwg. No. Q-2928-2. Cabling for each experimenter is routed from the Data Collection Equipment (DCE) Cabinet on DAC 3 (location C7 on the floor plan) to the experimenter's laboratory by cable trays (Dwg. No. Q-2928-4 has a plan view) under the raised floor. There are eight cable connections each from the DAC 3 DCE to DACs 1 and 2. The cabling for each of the DACs, the PEC, and the interconnecting cabling is on Dwg. No. Q-2928-3. The cabling has been arranged to allow substitution of DAC 2 for the PEC in case of a PEC failure requiring several days to repair. A re-cabling list is on Dwg. No. Q-2928-3. Drawing Number Q-2928-15 shows the interrupt cabling from the peripheral units to the PEC and the alternate routing to DAC 2. In addition, if the PEC has a short-term failure and there is an urgent need to dump data from a DAC, then a DAC can be connected to the Magnetic Tape Units (MTU) by removing two cables at the MTU, transferring two cables from the intercomputer link on the PEC to the MTU, and connecting the MTU interrupts to the DAC. In either case, a change in the ORELA Data Acquisition Monitor Programs⁴ on the DAC is also required. Note that nonstandard signal assignments are made on the I/O cable of each DAC as noted on Dwg. No. Q-2928-3.

3. DATA ACQUISITION AND COMMUNICATION PERIPHERALS

All of the following peripheral units are nonstandard pieces of hardware that were specified by the ORELA project, designed at SEL, and modified at ORELA as a result of operating experience. The intercomputer links between the SEL 810B computers are an exception, as the later models used are an SEL special systems standard with modifications by ORELA.

The sections covering each piece of hardware contain a general description of use, a simplified block diagram, and a brief explanation of operation. Detailed theory of operation is covered either in other sections of this report or in SEL technical manuals.

3.1 Word-Addressed Fixed-Head Disk (WAFHD)

Simultaneous operation of several experiments requires storage of a large amount of totalized data at moderate counting rates in hundreds of thousands of channels. The state-of-the-art and economic reality ruled out the convenient and easy-to-use core memory in sizes large enough for this requirement. Techniques such as associative storage⁶⁻¹⁰ and zone selection storage¹¹ in small-core memories have been implemented in other systems to increase the apparent channel capacity with minimized storage costs, but neither technique appeared to be applicable to ORELA's problem. A programmed disk system for large histograms of 3×10^5 channels, which has a practical limit of 2000 events/sec and uses a movable-head disk, has been described recently.¹² The ORELA system has fixed-head disks and a semirandom access controller; its practical limit is 5000 events/sec into about 0.8×10^6 channels. A second disk in the system has about 0.4×10^6 channels. The third disk in the system, with an improved controller, has a limit of 8000 events/sec into about 1.05×10^6 channels. The discrepancy between the high serial storage rate and the low random storage rate of a disk was overcome by use of an improved disk control logic¹³ that is coupled to a program in a small computer.

The parameters for the disks are listed in Table 1. Note that the DAC 3 disk has a larger number of tracks and a smaller number of words per track. An additional capability for DAC 3, called Update, halves the transfers required between the disk and computer memory to accomplish the same task.

The limitations of interleaving, access to one-fourth or one-half of the disk on each revolution, and the necessity of accessing all sequential addresses of an interleaf are overcome by using a list operation for transfers to and from all disks. The channel number to be accessed is determined by the track position, a relative location within a list that is specific to one interleaf number, and by a track address (track number), which includes the contents of the track position list. The interleaf is included by considering the disk buffer to be organized as interleaf 0, 1, 2, and 3, with each interleaf transferred as a list.

Table 1. Word-Addressed Fixed-Head Disk parameters

Disk	DAC 1	DAC 2	DAC 3
Words	786,432	393,216	1,048,576
Tracks	512	256	1,024
Words/track ^a	1,540	1,540	1,028
Bits/word	21 ^b	21 ^b	32 ^c
Bits/sec (x 10 ⁶)	1.875	1.875	1.908
Bit period (nsec)	533	533	524
Interleaf	4	4	2
Track switching time (μsec)	33.6	33.6	16.8
Theoretical access (words/sec) ^d	11,136	11,136	14,790

^aFour words per track are not accessible.

^bThree preamble bits, 16 data bits, 1 parity bit, and 1 guard bit.

^cTwelve preamble bits, 16 data bits, 1 parity bit, and 3 postamble bits.

^d $(\text{words/track})/2(\text{interleaf})17.24 \text{ msec/rev.}$

The translation to actual track position takes place in the disk controller hardware. The data sections on the disk are set up by the package 7COM and updated through the package 7RUN of ODAR.⁴ Programming notes for the disk are included in Appendix C.

3.1.1 Disk Operation

A diagram of the WAFHD and controller is shown in Fig. 6. The symbols BTC1 and BTC2 are for two of the direct memory access channels¹⁴ of the SEL 810B computer. The Read-Write control contains a track register and decoding matrix for head selection, a data register, a parallel-to-serial and serial-to-parallel converter, and a bit counter for control within a word.

The operation of the disk is as follows. A command to start reading a particular interleaf is sent to the disk controller from the computer. The track address is obtained by BTC1 control, and the corresponding head is selected. A prerecorded disk Index signal is read from the disk to start time zero for the disk control. The Index

Fig. 6. Word-Addressed Fixed-Head Disk (WAFHD) block diagram.

signal, coupled with a Ready signal from the direct memory access channels, generates an Active signal, which allows the Word Clock signal from the timing track of the disk to be counted in the position register. The two least significant bits of the position register are combined with the interleaf bits to generate an Execute signal to the Read-Write control. The word is serially read from the disk and transferred in parallel to the data register under control of the bit counter. BTC2 causes a transfer to the computer memory to take place. Then BTC1 transfers a new track address to the disk control. Each interleaf coincidence (the interleaf selected is equal to the least significant bits of the track position counter) actuates a Read cycle until a maximum of 384 words are read. [It is possible to read (write) part of an interleaf starting at its beginning.] When the position register reaches a count of 1537, an End of Revolution signal is generated that resets the Active flip-flop. A Block Transfer Complete Interrupt (BTCI) signal is generated when the last data word of an interleaf is transferred by BTC2. The BTCI signal forces an entry to a program that starts the next cycle, either a Read or a Write on a different interleaf. Several revolutions later, data that were read and subsequently incremented by a program are written onto the disk. The major difference in writing is that the access to memory on BTC2 takes place before the Word Clock signal from the disk occurs.

The improved controller on DAC 3 has an Update instruction that uses a memory and adder within the disk controller to temporarily store a list of random track addresses with the corresponding incremented data. This additional system is shown in Fig. 7. The list containing track addresses and increment fields is transferred from fast memory by way of BTC1, in step with a read data transfer from the disk for the particular track address. Simultaneously, BTC2 is used to transfer zeros to the list locations in preparation for use as a new track buffer. (The Block Priority Control and disk controller logic sequence the accesses to computer memory alternately between BTC1 and BTC2, with a BTC1 access always occurring first at the beginning of a list transfer.) The increment field is added to the data that were read. The track address and incremented data are then stored until the following disk revolution,

ORNL-DWG 76-15898

Fig. 7. Update control block diagram for the WAFHD.

at which time this information is written on the disk to complete an Update instruction. Note that each Update instruction uses two consecutive revolutions of the disk. The controller will accept another disk instruction at the completion of the list transfer; however, execution will be delayed until the Update-Write cycle is completed.

The detailed logic diagrams are in Drawing Series Q-5183 (SEL Drawing Series 53335) with a detailed description in an SEL Technical Manual;¹⁵ Drawing Series Q-5193 (SEL Drawing Series 130-100835-000) contains the detailed logic diagrams and a timing diagram for the Update version of the WAFHD.

3.2 Four-Channel Priority Multiplexer (FCPM)

The FCPM has a maximum transfer rate of $25,000 \text{ events sec}^{-1}$ channel⁻¹. This multiplexer input data rate is reduced by the disk storage hardware (maximum access rate to all channels is 11,140 channels/sec on DACs 1 and 2 and 14,790 channels/sec on DAC 3), by the event processing routines, and by partial filling of the disk buffers to a combined system event rate for all four channels of 5000 events/sec on DACs 1 and 2 or 8000 events/sec on DAC 3. However, short-term peaks can be handled by the multiplexer input buffer and an experimenter's CRUNCH routine may purposely delete events.

Each event, consisting of 30 bits of data, is transferred into the SEL 810B computer memory via a BTC channel (direct memory access) as two 16-bit words. The first word transferred has a channel identification number, 0 through 3, included as the two most significant bits. The coding of these bits is determined by the hardware.

The following is a typical format for the multiplexer first word:

The second word contains 16 bits of time-of-flight data. The data portion of the first word may extend to bit 3 if no tagging is used. The data in both words can be all time-of-flight or it can be a combination of pulse-height and time-of-flight data. The word format is defined for each experiment, with the least significant bit of the time-of-flight data always occurring in bit 15 of the second word.

A multiplexer transfer checking circuit is used to detect an odd number of transfers to the computer memory. If an error occurs, an interrupt is generated which is then used by the 7MUL package of ODAR⁴ to initiate a multiplexer error routine. The error rate is a function of the particular combination of experimenter's data rates and their channel number assignments. The number of occurrences can be typed out by using the SYstem SStatus (SYST)⁴ call, entry 0, to the ORELA Data Acquisition Monitor as shown in the following output:

```
* SYST
+
ØCT 9  3:47:38
      (0) 7GGS      (1) 7JWT      (2) 7JAH      (3) 7GLM
BU~  11973039      22591758      478376      20913930
BNU~      935      4128      80      8371
IBU~      2      0      1      0
      210 MPXR ERRORS
```

Programming Notes for the FCPM are included in Appendix C.

3.2.1 Multiplexer Operation

A simplified block diagram of the FCPM is shown in Fig. 8. Note that all of the control signals are strobed by a timing signal derived from the SEL 810B computer clock.

A Data Ready (DR) pulse from the experimenter's equipment sets a Channel X Busy (CXBSY) flip-flop. The CXBSY flip-flop output is returned to the experimenter. The event data must be held constant while CXBSY is present. ClBSY (Fig. 8) is then strobed into a pair of word flip-flops (C and D for channel 1) along with the active CXBSYs from the

Fig. 8. Four-Channel Priority Multiplexer block diagram.

other three channels. A word-transfer timing control circuit then generates a BTC3 Data Transfer Request (DTR) to the Block Priority Controller (BPC) at the SEL 810B computer. (There are a maximum of eight BTC channels on the SEL 810B computer.) The BPC responds via the BTC3 channel connected to the multiplexer with a BTC3 Gate Data Out (GDO) that causes the first word (Word C) in Multiplexer Channel 1 to be gated onto the I/O Bus of the computer. The GDO signal is slightly delayed and returned to the BPC as BTC3 Unit Data Here. The data is then strobed into memory by the BPC, which then removes the GDO signal. The removal of GDO resets the Word C flip-flop in the multiplexer. The word-transfer control circuit generates another DTR at the next timing pulse from the computer to initiate a transfer of the second word (Word D). When the transfer of Word D is completed, ClBSY flip-flop is reset. ClBSY to the experimenter is removed and a Data Accepted pulse is routed to the experimenter. The event transfer started by DR is now complete.

If other channels are busy when the ClBSY signal is strobed into word flip-flops C and D, they will also be transferred to the computer memory in the priority sequence, A through H, as required. Another DR on channel 1 will wait until all words of the existing priority sequence have been transferred to the computer memory.

About 90% of the data in any channel is transferred to memory within 10 to 14 μ sec, with an occasional event requiring a maximum of 30 μ sec. If a DR signal in a channel misses a priority transfer sequence of the remaining three channels, then a maximum busy period of approximately 72 μ sec could occur.

The detailed logic diagrams are in Dwg. Nos. Q-5036-12 through -24. Volume 2 of this report contains a detailed description of word formats, signal levels, connector layouts, etc. A Stacking Buffer Memory that is used in conjunction with the FCPM is described in Vol. 6, and a tester for the multiplexer channels is described in Vol. 7 of the report.

3.3 Cathode-Ray Tube Display (CRTD)

The display system in use on the data acquisition system is an 8- by 10-in. CRTD (Hewlett-Packard, Model 1300A X-Y Display) with an SEL-designed controller operating on a BTC channel for automatic refresh from core memory. The utility of the display is intimately related to the display package 6CRT⁴ of ODAR, since the controller is basically a three-axis (X, Y, and intensity) digital-to-analog (d-a) converter. The X and Y axes contain 10 bits, while the Z or intensity axis uses two bits for four levels of intensity, including blank as the lowest level. The 6CRT package displays a 512-point data curve and a 14-point light pen function area (see 6CRT Light Pen Function Points and Teletype Commands in Appendix E). The additional control features are an increment mode that allows transfer of a list of Y-values to plot a curve and control logic to read the X and Y coordinates when a point is picked by the attached light pen. Note that store and erase logic is included in the controller for use with a storage tube. The storage function will not be implemented. Programming Notes for the CRTD are included in Appendix E.

3.3.1 CRTD Operation

The data registers of the CRTD controller are shown in Fig. 9. After initialization,¹⁶ with the control set for automatic reinitialization through the use of unit decode, I/O Sync, and the BTC Interface, the controller (in conjunction with the BTC Interface) produces the display from a particular core area. The data points have one bit to specify the coordinate and two bits to specify the intensity (see CRTD Programming Notes in Appendix E). The data point list has one X-value (equal to zero) and 512 Y-values with a medium intensity specified. The X-value is routed to the X-coordinate d-a converter. The Y-values are then routed to the Y-coordinate d-a converter, with each Y-value initiating a 25- μ sec intensify transfer cycle. (The transfer cycle for nonintensified points is 3 μ sec.) The first 10 μ sec are allowed for settling of the beam after changing the d-a converter inputs, 5 μ sec

Fig. 9. Cathode-Ray Tube Display block diagram.

are used to intensify the beam, and the remaining 10 μ sec constitute a delay adjusted to allow a flicker-free display of 1024 points when a dual command is executed by the 6CRT package.

The detailed logic diagrams are in Drawing Series Q-5185 (SEL Drawing Series 53351) with a detailed description of operation in an SEL Technical Manual.¹⁶

3.4 Scaler Interface and Device Controllers

A data acquisition system is not complete without some degree of monitoring and control to free the experimenter from the routine tasks of data collection. The Scaler Interface coupled to a maximum of four Device Controllers provides these two functions in the ORELA Data Acquisition System. The Scaler Interface in the Data Collection Equipment Cabinet at the SEL 810B computer operates under program control to read in the contents of scalers or the position status of sampling changers to perform the monitoring function. The present Device Controllers are capable of transferring data from eight devices and eight internally gated scalers into the computer. The control function, also under program control, makes use of scaler read-in, time, or other parameters to change the experiment conditions according to a predefined list. The control is accomplished by generation of eight subgroups of twelve pulses that are generated either singly or in parallel in any desired combination. Timing sequences with a minimum of 3 μ sec between pulses can be generated by using a combination of programming loops and the 60-cycle clock interrupt. Programming Notes for the Scaler Interface are included in Appendix C.

3.4.1 Scaler Interface Operation

The program-controlled Scaler Interface can be separated into three related sections: addressing, pulse selection (Fig. 10), and data input control (Fig. 11). The interface is controlled with a command word by the I/O synchronization¹⁷ of the SEL 810B computer. The command word determines the format as either an address or a pulse command by the

Fig. 10. Scaler Interface, device addressing, and pulse selection.

Fig. 11. Scaler Interface, data input control.

state of bit 0, either off or on respectively. The detailed logic diagrams are in Dwg. Nos. Q-5036-1 through -11. Volume 3 of this report is a detailed description of word formats, signal levels, and connector assignments for the Scaler Interface. A tester is described in Vol. 6.

3.4.1.1 Addressing. The address in a FORMAT "0" command is specified by bits 11 through 15 of the command word. These bits are stored in a five-bit address register. The most significant bits of the address (11 and 12) are then encoded to produce four group signals. Each of the four group signals is then routed to a Group X pin of the cables connecting the Device Controllers. The software of ODAR requires the same number for the multiplexer (Sect. 3.2) channel and the Scaler Interface group. The address outputs are used by the Device Controller to select a data input path.

3.4.1.2 Pulse selection. A FORMAT "1" command will generate pulse outputs as specified by bits 4 through 15 of the command word. All pulses occur simultaneously. Although the width of the pulses can be manually adjusted over four ranges (0.3 to 6 μ sec, 2 to 60 μ sec, 20 to 600 μ sec, and 0.3 to 6 msec) in actual practice they have been set to either 1 or 2 μ sec, as required by the Device Controllers (see Vol. 3, Sect. 3.2 for restrictions). The Gate Input Bus and Load Word 1 and 2 pulses are used to control the read-in of data placed on the input lines of the Device Controller.

3.4.1.3 Data input paths. The data input paths (Fig. 11) consist of an interrupt path on the left and a 32-bit program-controlled path on the right. Both paths use the pulse generation mode of the Scaler Interface, and the latter also uses address selection for routing data through the Device Controller. Transfers on the interrupt path are started by a Ready interrupt that is routed to the computer. The interrupt control program then responds with a Gate Input Bus pulse followed by an input instruction¹⁸ from the SEL 810B computer. This data path has been reserved for system use.

The 32-bit program-controlled word path is initiated from either a predefined condition of monitored inputs, a predefined amount of time, or an experimenter interrupt. The Load Word program sequence generates a device address followed by a Load Word pulse and is completed with an input instruction either direct to memory or into the accumulator of the computer. The two 16-bit Load Word paths can be operated independently.

3.4.2 Device Controller Operation

The common control of the Scaler Interface is shared by a maximum of four Device Controllers on one DAC. When a Group X signal to a Device Controller is enabled, it allows a program-generated control sequence to be performed for that particular experimenter. About 75% of the logic in a Device Controller is in a standard configuration for all of the presently designed controllers. The remaining 25% has been specialized to meet the input and output signal requirements and control (e.g., a stepping motor) of a particular experimenter. The block diagram of a controller is shown in Fig. 12. The figure within the logic block indicates the number of circuits in the logic. There are five sections to the control: address encoding, pulse definition, register storage, a status monitor (not shown), and a 32-bit parallel input data multiplexer. The detailed logic diagrams for the Device Controllers are in Drawing Series Q-5098. The standard part is on Dwg. Nos. -1 to -9, while the specialized part is on Dwg. Nos. -10 to -19, -20 to -29, etc. Volume 4 of this report contains a detailed description of word formats, signal levels, and connector layouts. The specialization for each experimenter is added as required by an appendix. The ODAR control routines (4XXX, 5XXX, and 6XXX, where XXX is the experimenter's initials) are available upon request from each experimenter.

3.4.2.1 Address encoding. The Group X signal, where X (0, 1, 2, or 3) is defined by a cable connector, and the three address lines from the Scaler Interface are combined in eight AND gates to provide Scaler Select levels (SCSELX0 through X7). These signals are then used by the pulse definition and input data multiplexer logic.

Fig. 12. Device Controller block diagram.

3.4.2.2 Pulse definition. The pulse definition logic combines the SCSELXY signals with the twelve input pulses in banks of two input AND gates to provide a pulse group PXY01 through PXY12. These 96 defined pulses are then used to clear and set registers, to generate routing data for the input data multiplexer, or to control external functions as required. Twelve of the pulses are designated for internal use within the Device Controller.

3.4.2.3 Register storage. The register storage as presently used contains 24 bits in two groups of 12 bits. Clear pulses further divide each 12-bit register, defined by pulses PX1- or PX2-, into segments of 5, 5, and 2. These registers are then used to control five position paddle filters or sample changers. The external circuit drivers on the output of the registers restrict the controller to one experimenter location.

The storage can be expanded to a practical maximum of 72 bits with 24 pulses available for other control. Twelve of the control pulses are now defined in the standard logic; however, six of these pulses are used as register clears and could be reassigned in another design.

3.4.2.4 Status monitor. The status monitor produces an OPERATE signal if four monitor conditions are satisfied: (1) start pulses from the linear accelerator are occurring at an adjustable minimum rate; (2) the SEL 810B computer is in the RUN condition; (3) the FCPM is connected; and (4) a Program Start pulse has been generated. The FCPM logic produces a signal, MPXR CONTROL, that contains two of the status conditions, RUN and multiplexer connected. The Program Start pulse and its inverse, Program Stop, are two of the Device Controller internal control pulses.

3.4.2.5 Input data multiplexer. The input data multiplexer is a 32-bit parallel 16-input gated data path that is controlled by the defined pulses and encoded addresses supplied by the Scaler Interface. Three choices of inputs are allowed: a Scaler Bus used with internal AND gating in the scalers (a maximum of eight scalers is presently allowed),

one of eight externally gated devices, and all inputs disabled. The Scaler Bus can be extended in blocks of eight additional inputs (to a maximum of 64) by using two pulses to control the routing for each eight additional scalers. The gates for the externally gated devices are in the controller.

3.5 Intercomputer Links

Four intercomputer links are operating between the PEC and the DAC; a fifth link, PEC/PDP-7, is planned for future installation. The original link, PEC/DAC 1, and two more recent links (SEL Model 711401B), PEC/DAC 2 and PEC/DAC 3, have been modified (see Sect. 4.2.2) for use with the ORELA Data Acquisition System. Each link can now generate an interrupt to the other computer, independent of BTC initialization.¹⁴ The command word cannot be sent to the other computer under any circumstances. Programming Notes for the links are included in Appendix E.

3.5.1 Link Operation

All of the links operate in an asynchronous mode. Transfer of a block of data is started by the generation of an interrupt to the other computer. Either a Buffer Empty or a Buffer Full level is used to signal the other computer (#2) for taking output from or sending input to the originating computer (#1). The response to this level is either a Data Accepted or a Data Here pulse for input to and output from the accepting computer (#2). The transfer rate is determined by the BTC activity in each machine; however, the maximum transfer rate is 443 kHz. BTC transfers automatically generate these synchronization pulses. The PDP-4 generates the control pulses by use of a control program. No direct memory access to or from the PDP-4 is possible with the existing hardware. On the other hand, the PDP-9 is capable of both direct memory access and program controlled transfers to and from the accumulator. The transfers on the links are controlled by the monitor package 7LNK.⁴

The detailed drawings for the SEL 810B Intercomputer Links are on Drawing Series Q-5188 (SEL Drawing Series 53425) for PEC/DAC 1 and Drawing Series Q-5186 (SEL Drawing Series 53360) for PEC/DAC 2 and PEC/DAC 3. SEL's *Technical Manual, Intercomputer Data Link*¹⁹ is applicable to both links; however, the DAC 1 link does contain logic that is not included in the other two links. Volume 2 of SEL's *Technical Manual, Data Acquisition System*²⁰ also contains a description of the DAC 1 Intercomputer Link.

The SEL 810B Interface, Drawing Series Q-5187 (SEL Drawing Series 53422), for the SEL 810B/PDP-4/PDP-9 Intercomputer Link is described in Vol. 2 of SEL's *Technical Manual, Data Acquisition System*.²⁰ A detailed description of the PDP-4 and PDP-9 Interfaces on the SEL 810B/PDP-4/PDP-9 Intercomputer Link is in Vol. 5 of this report.

3.6 Binary Synchronous Communications Interface (BSCI)

The BSCI is used to communicate with the Immediate Analysis and Coordinating Computer² over telephone pairs with a Western Electric 301B Data Set operating at 40.8 kilobaud. The BSCI is a word-to-byte-to-bit-stream converter on output and the reverse on input. It has logic to generate the synchronizing (SYN) character on transmission and recognition logic for the SYN character to synchronize the interface with the incoming bit stream on reception. Other communication control characters²¹⁻²³ are also recognized and used to control information transfer to and from the computer. Transmission is controlled by the packages 7MUP, 7SND, 7BSI, and 7BSO in the ORELA Data Acquisition Monitor.⁴ Programming Notes for the BSCI are included in Appendix E.

The logic schematics Drawing Series Q-5108 (SEL Drawing Series 130-100500-000) are in Volume 2 of ref. 23 with the supporting assembly, cable, and printed circuit drawings. An explanation of the communication control procedures is on pp. 2-6 to 2-10 of ref. 23.

4. REVIEW OF MODIFICATIONS TO THE SEL 810B COMPUTER FOR THE ORELA DATA ACQUISITION SYSTEM

The installation of the ORELA Data Acquisition System in April 1969 (now referred to as Phase I), consisting of DAC 1 and 2, has been followed by a nearly continuous modification of the hardware and software as the ORELA Facility began to acquire data, at first from a single experimenter and later from two or more. Several modifications were included in the computer hardware to increase its capabilities by providing control that was not otherwise available. Modifications have been made to three groups of equipment: (1) the central processing unit (CPU) of the SEL 810B computer; (2) standard peripheral units such as the magnetic tape controller, the intercomputer links, and the line printer; and (3) nonstandard peripheral units. These three groups are briefly covered in Sects. 4.1, 4.2, and 4.3 respectively.

4.1 Modifications to the CPU

Special modifications to the CPU for ORELA are indicated on the prints for DAC 1 and DAC 2 by a note to the left of the title block, "Used on project no. J2191." The majority of these revisions have been incorporated in the current production of the SEL 810B computer. The PEC and DAC 3 contain these modifications.

4.1.1 Special Modifications by SEL

Four of the special modifications that are not included in current production are shown on the Computer Reference Copy (on file in the Central Data Area of Building 6010) of the drawings listed below. The gates and flip-flops are shaded in red. In addition, there are two modifications that are not incorporated as revised drawings.

<u>Change</u>	<u>SEL Dwg. No.</u>	<u>Sheet, Area</u>	<u>Comment</u>
1	130-810017-000	25C6	
2	130-810057-000	5	Diodes in SX lines to prevent cross talk.
3	130-810147-000	3D5	A disk programming restriction eliminates this change in DAC 3.
4	130-810167-000	2D4	
5	130-810057-000	6B7	These changes use the active interrupt signal (AI3 or AI2) to turn on the interrupt light when an interrupt is being processed.
	130-810087-000	7B5	
	130-810087-000	9A4	
	130-810087-000	8A4	
6	130-810087-000	8A6	Connects the intercomputer link interrupts between the PEC and DAC 1 to DAC 1 via DAC 1 I/O Bus cable.
	53425	13B6	
	53425	15A1	

4.1.2 System Modifications by ORNL

These are miscellaneous modifications that were needed to increase system capabilities or to aid program debugging. They are included as dated changes on the drawings.

<u>Change</u>	<u>SEL Dwg. No.</u>	<u>Sheet, Area</u>	<u>Comment</u>
1	130-810087-000	8C6	RUN+ to I/O Bus for use in generating the MPXR CONTROL signal. See Dwg. No. Q-5036-20.
2	130-810057-000	6C2	Turns on X Index light if the index pointer is set to the X-register.
	130-810087-000	7A4	
	130-810117-000	5B2	
3	130-810077-000	6A8	Prevents generation of Memory Parity Errors when inputting data via a BTC channel. Wiring for DAC 3 is not the same as for DAC 1 and DAC 2.

4.1.3 Special Interrupts

Three software-triggered interrupts have been provided by connecting the interrupt inputs to a positive or negative source of voltage as required by the input used (see SEL Dwg. No. 130-810017-000, Sheet 26, area C7) to generate an interrupt request.²⁴ An enable instruction (PIE) to either the TTY ESCAPE, CRUNCH, or LINK interrupt (see SELPIA.LST in Appendix E) will allow the particular interrupt to become active in the normal manner.

4.1.3.1 TTY ESCAPE. Typing a CNTRL H forces generation of this interrupt through 7NTP, the teletype handler package of the ORELA Data Acquisition Monitor.⁴

4.1.3.2 CRUNCH. The CRUNCH interrupt is initiated by 7MUL and 7RUN, the packages for controlling the multiplexer and the disk during data acquisition.

4.1.3.3 LINK. The LINK interrupt is initiated by 7LNK, the package controlling the communication between the PEC and all of the other computers.

4.1.4 Disk Initialize Complete Interrupt on the DACs

A latch has been added that is set by LWCRI and reset at T7 (SEL Dwg. No. 130-810177-000, Sheet 2D4). The latch provides a Disk Initialize complete interrupt to the software to allow FWA and WC changes on the BTC while operating the disk BTCs in automatic reinitialization mode.

4.1.5 BTC Word Count Equal Zero Control on the PEC and DAC 3

ECO 71-494 revised the word count control for earlier recognition of WC = 0, particularly in applications requiring maximum rate transfers. This change would not allow a BTC complete interrupt to be

generated by setting the BTC to terminate with a $WC = 0$. This ECO has been modified on BTC4 through BTC8 in the PEC and on BTC4 in DAC 3 by removing a wire (SEL Dwg. No. 130-810187-00, Sheet 9A5) between a flip-flop (pin 2X13) and an eight-input NAND gate (pin 2X41). All of these BTCs are used by the intercomputer links in the data acquisition system.

4.2 Modifications to Standard Peripherals

Modifications have been made to three standard peripheral units: the magnetic tape controller, the intercomputer links, and the line printer. The modifications to these units increase system capabilities by allowing a simple procedure, sometimes semiautomatic, for recovery from either a procedural or a hardware error.

4.2.1 Magnetic Tape Controller

Changes were made to the Program Error Latch (SEL Dwg. No. 130-800217-000, Sheet 6D1) and Busy Control (SEL Dwg. No. 130-800217-000, Sheets 14C3 and 14D3).

4.2.1.1 Program error clear. The BCD indicator on the front panel of the TCU was reassigned to indicate a PROGram error; a push-button reset, PROG CLEAR, was added to allow a manual escape from a procedural error in which the magnetic tape transport number selected by a rotary switch on the transport does not agree with the transport number selected by the program. Note that the programmed transport number is designated by a control word in the parameter list of 2MAG, the magnetic tape I/O handler for the ORELA Data Acquisition Monitor.⁴ This control-word transport number is derived either from a keyboard entry or a transport number that is preselected by some other package, such as 3MTP, 7SND, and 9MAG.

4.2.1.2 Busy. Two changes were made to the Busy flip-flop control: (1) a push-button reset was added (SEL Dwg. No. 130-800217-000, Sheet 14C3) to provide a means of resetting after a procedural error (for instance, a manual reset while a tape drive is operating), and (2) a gate was added (SEL Dwg. No. 130-800217-000, Sheet 14D3) to prevent a busy condition from being set at Close Window (CWO) time if the motion flip-flop was reset.

4.2.2 Intercomputer Link

Three modifications have been made to the intercomputer links between the PEC and the DACs. Two SEL Drawing Series, 53425 and 53360, are used, the former by the PEC/DAC 1 Link and the latter by the PEC/DAC 2 and PEC/DAC 3 Links. SEL Drawing Series 53425, an extension of Drawing Series 53360, contains additions that were specifically added for ORELA. These modifications are not presently used by the ORELA Monitor and are either functionally disconnected (as shown by the shaded logic on Sheets 2, 3, 8, and 9 of Drawing Series 53425) or not used by the software (SEL Drawing Series 53425, Sheet 15). Sheet 15 contains test logic and End of Record interrupts. The three modifications are described below.

4.2.2.1 Function of bit 6 in CEU second word. The function of bit 6 in the CEU second word was changed from that of transferring the CEU second word to the other computer to that of clearing the output buffer control flip-flop (see SEL Dwg. Nos. 53360 or 53425, Sheets 3 and 9, area D5, ORNL Rev. E and C respectively).

4.2.2.2 On-line switch. An on-line switch was added (SEL Drawing Series 53360) and modified (SEL Drawing Series 53425) to disable the output initialize interrupt when the switch is in the OFF-LINE position. The switch is normally at the ON-LINE position, except for selectively disabling communication between the DACs and the PEC during troubleshooting or program debugging (see SEL Drawing Series 53360 and 53425, Sheets 3 and 9, area D5, ORNL Rev. E and B respectively).

4.2.2.3 Master clear of output buffer. The Master Clear signals, MC1+ and MC2+, to the output buffer control flip-flops have been modified so that a Master Clear from either computer will clear both of the output buffer control flip-flops. This requirement resulted from the need to define the state of the intercomputer links when an intercomputer link is cleared by turning the power off.

4.2.3 Line Printer

The source of 115 V ac for the +3.6 V dc power to the SEL logic chassis in the shuttle line printer was removed from the power sequence control of the line printer. The SEL logic is on unless the main circuit breaker is tripped. This change allows the logic to respond to a command instruction when the mechanical portion of the line printer is off.

4.3 Modifications to Nonstandard Peripherals

Modifications have been made to five nonstandard peripheral units. These units, in order of increasing number or complexity of changes, are the WAFHD, the CRTD, the BSCI, the FCPM, and the Scaler Interface. The changes to the latter two logically separate units, physically in one chassis with one drawing series, were so extensive that a new ORNL Drawing Series Q-5036 has been produced superseding SEL Drawing Series 53320.

4.3.1 Disk Revolution Not Used Interrupt on the Word-Addressed Fixed-Head Disk

If a read or write command has not been received by the disk controller when the Disk Index point is recognized by the controller hardware, a DRNUI is generated. This signal is used by 7RUN, a disk handler package on the ORELA Data Acquisition Monitor, to restart the update process during data acquisition. See Dwg. No. Q-5183-6, location B8, or SEL Dwg. No. 53335, Sheet 6B8, Rev. A for the changes.

4.3.2 Cathode-Ray Tube Display

Four changes were made to the CRTD controller. Two of these changes resulted from operation with the 6CRT program. The other two changes were required when switching to the 8- by 10-in. HP1300A display CRT. The references are to drawing dash number and location on ORNL Drawing Series Q-5185. These changes have been included in the CRTD for DAC 3 as ECOs 72-621, -622, and -690.

4.3.2.1 Set high-order X-address bits during increment mode. The CRTD controller was modified (7C5 and 6B6) to allow a new X-address to be gated into a storage register. The low-order bits (13, 14, 15) are always set to zero by the hardware.

4.3.2.2 Disable BTC transfers on light pen strike. Transfers via the BTC were blocked (3A5 and 7B2) until the light pen interrupt was serviced.

4.3.2.3 Intensity driver conversion. The intensity driver (SEL Dwg. No. 160-83330) was modified to provide a -1 to +1 V (blanked to maximum intensity) signal for the HP1300A X-Y Display. The original levels were +50 to +75 V.

4.3.2.4 Operational amplifier gain change. The gains of the d-a operational amplifier (SEL Dwg. No. 160-052540) for the X and Y coordinates of the display were modified for use with the HP1300A X-Y Display. Resistor R10 was changed from 2050 Ω to 680 Ω . A 120- μ F bypass capacitor was also added to reduce an oscillation of a displayed point. The leads to the horizontal and vertical deflection plates in the HP1300A X-Y Display were also reversed.

4.3.3 Binary Synchronous Communications Interface

Twenty-two changes have been made in the BSCI. Some of these changes were included in the *Technical Manual* for the BSCI²³ and SEL Drawing Series 130-100500-000. All of the changes are marked on the ORNL sepias (designated as Drawing Series Q-5108) of the SEL Drawing Series. A list of revised drawings keyed to the paragraph changes in the SEL *Technical Manual*²³ has been inserted in the ORELA copies of the manual. The ORELA manuals have been corrected.

The BSCI changes were made to correct control errors when certain control characters occurred as data during transparent mode or appeared as a cyclic redundancy check character at the end of a data block.

4.3.4 Four-Channel Priority Multiplexer

The modifications made to the multiplexer were the addition of three groups of 16-input lines, the rerouting of four channel-control signals to eight-word control flip-flops, and the addition of multiplexer error detection logic. The first two changes converted the four multiplexer channels from one dual-word and three single-word channels to four dual-word channels with a separate 75-pin connector for each channel. The latter change exposed a hardware malfunction, caused by pulse splitting, that was reduced in the number of occurrences but could not be completely eliminated.

The multiplexer operation is described in Vol. 2 of this report.

4.3.5 Scaler Interface

The Scaler Interface modifications were made to increase flexibility in using the available inputs to the interface. Reassignment of control signals and input lines allowed separation of the interface inputs into an interrupt-activated 16-bit Input Bus and a 32-bit program-controlled Word Input. The latter section also includes the Scaler Select signals and 12 Scaler Pulses for device control and input multiplexing on the two 16-bit Word Inputs.

The Scaler Interface is described in Vol. 2 of this report.

5. ORELA DRAWING SERIES

The following drawing series (see Appendix A) were used at ORELA for the purposes listed.

5.1 Q-2928, ORELA Data Acquisition

This series contains miscellaneous drawings such as block diagrams, equipment floor plans, cable tray layouts, computer cabling, ground system wiring, performance specification drawings, etc.

5.2 Q-2956, PDP-4 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link

The Dwg. Nos. Q-2956-30 through -39 in the series are for the PDP-4 interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link (see Drawing Series Q-5072 for the PDP-9 Interface and the SEL 810B ground isolation). See Vol. 5 of this report for details.

5.3 Q-3079, ORELA Digital Multiplexer, Level Matching

This drawing series was used as an interim drawing series for signal-level matching of an Eldorado Clock or a TMC Time-of-Flight Analyzer to the FCPM before installation of the ground isolation system. The circuit drawing (Dwg. No. Q-3079-1) has been superseded by Dwg. Nos. Q-5110-1 and -2 respectively.

5.4 Q-5036, Scaler Interface and Four-Channel Priority Multiplexer

This series contains extensively revised copies of SEL Drawing Series 53320¹⁵ for the Scaler Interface and the FCPM. Each of the dash numbers in the series corresponds to a sheet of the original drawing series. The ground isolation circuits for the FCPM and Scaler Interface are Q-5036-25 and -30 respectively.

The modifications to the Scaler Interface consisted of reassignment of the Scaler Interface signals to two connectors so that the Scaler Input Bus and the interrupt signals Scaler Data Ready and Scaler Overflow for interrupt control are separated from the 32-bit Scaler Word Bus, the Scaler Select signals, and the Scaler Pulses used in program controlled input. See Vol. 3 of this report for details.

The modifications to the FCPM included the addition of input lines to convert the four multiplexer channels from one dual-word and three single-word channels to four dual-word channels with a 75-pin connector for each channel. See Vol. 2 of this report for details.

5.5 Q-5066, Eight-Stage Stacking Buffer Memory

The Eight-Stage Stacking Buffer Memory drawings are in this series. See Vol. 6 of this report for details.

5.6 Q-5072, PDP-9 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link

Drawing Series Q-5072 includes the drawings for the PDP-9 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link. The ground isolation chassis at the SEL 810B is Dwg. No. Q-5072-15 of the series. See Drawing Series Q-2956 for the PDP-4 Interface and ground isolation. This series also contains the individual isolation modules used throughout the system. See Vols. 5 and 8 of this report for details.

5.7 Q-5094, Ground Isolation Receiver and Driver Tester

Series Q-5094 is a drawing series for a tester for the ground isolation driver and receiver cards in Drawing Series Q-5072. See Vol. 8 of this report for details.

5.8 Q-5098, ORELA Device Controller

This series contains the drawings for the ORELA Device Controller, a generalized control system that is specialized for a particular application such as sample changer control by either pneumatic or motor driven operation, read-in of scalers or other devices, generation of miscellaneous control pulses, etc. Three specialized controllers have been built. See Drawing Series Q-5109 for pulse generation only. See Vol. 4 of this report for details.

5.9 Q-5108, Binary Synchronous Communications Interface (SEL 130-100500-000)

This series contains modified sepia copies of the original drawings for the BSCI supplied by SEL as Drawing Series 130-100500-000, sheets 1 to 29, plus miscellaneous special circuit cards. The modifications to the drawings corrected operational deficiencies discovered after the initial checkout of the system with an SEL-designed tester and program. See a revised copy of SEL Publication No. 315-552090-001²³ for details.

5.10 Q-5109, ORELA Isolated Pulse Generator

This series contains the drawings for the ORELA Isolated Pulse Generator Nuclear Instrument Module. The pulse generator produces 12 pulses, singly or in combination, through a control program. The pulse generator logic is also included in the Device Controller (Drawing Series Q-5098) where it can be expanded to 96 pulses for each of four channels connected to one data acquisition computer. See Vol. 4 of this report for details.

5.11 Q-5110, ORELA Digital Multiplexer, Level Matching

This series contains the drawings for the interfaces used to match the signal levels of existing and new equipment. The interfaces also isolate the cable capacitance (60 to 400 ft of twisted pairs) from the

experimenter's equipment and drive the ground isolation module (Dwg. No. Q-5036-25) to the multiplexer.

5.12 Q-5130, ORELA Data Acquisition, Multiplexer-Scaler Tester

This series contains the drawings for a tester used with the FCPM input or the Scaler Interface. It generates four test patterns either under control of a self-contained clock when used with the multiplexer or under control of a computer program when used with the Scaler Interface. See Vol. 7 of this report for details.

5.13 Q-5183, Word-Addressed Fixed-Head Disk Logic (SEL 53335)

This series contains revised sepias of SEL Drawing Series 53335 for the WAFHD on DAC 1 and DAC 2.

5.14 Q-5184, 810B I/O Expander (SEL 53344)

This series contains revised sepias of SEL Drawing Series 53344 for the I/O Expander on the PEC.

5.15 Q-5185, Cathode-Ray Tube Display (SEL 53351)

This series contains revised sepias of SEL Drawing Series 53351 for the CRTD.

5.16 Q-5186, PEC/DAC 2 or PEC/DAC 3 Intercomputer Link (SEL 53360)

This series contains revised sepias of SEL Drawing Series 53360 for the Intercomputer Links between PEC/DAC 2 and PEC/DAC 3.

5.17 Q-5187, 810B/PDP-4 Intercomputer Link (SEL 53422)

This series contains revised sepias of SEL Drawing Series 53422 for the SEL 810B/PDP-4 Intercomputer Link.

5.18 Q-5188, PEC/DAC 1 Intercomputer Link (SEL 53425)

This series contains revised sepias of SEL Drawing Series 53425 for the Intercomputer Link between PEC/DAC 1.

5.19 Q-5193, Automatic Update WAFHD (SEL 160-100835-000)

This series contains sepias of SEL Drawing Series 160-100835-000 for the Automatic Update WAFHD on DAC 3.

6. ENGINEERING DRAWINGS

<u>Drawing No.</u>	<u>Page</u>
Q-2928-2	47
Q-2928-3	48
Q-2928-4	49
Q-2928-5	50
Q-2928-14	51
Q-2928-15	52
Q-5036-25	53
Q-5036-30	54

LEGEND

- 810B Computer (2 Cabinets in DAC 2)
- PTRP Paper Tape Reader Punch
- TCU Tape Control Unit
- MT Magnetic Tape Unit
- CR Card Reader
- LP Line Printer
- X-Y Calcomp Plotter
- KSR35 Teletype KSR35
- ASR35 Teletype ASR35
- DCE Data Collection Equipment
(Digital Multiplexer, Scalar
Interface, Cathode Ray Tube Display)
- E Experimental Equipment
- I/O Remote I/O Remoter for DCE; I/O Bus
Expander; Computer Links.
- ☒ Cable Tray Access

TYPICAL TRAY ELEVATIONS:

NOTES:
1- Dimensions in doorways are cable tray distance from DCE to experimental equipment.

BLDG 600, SEL 8108 COMP INTERRUPT CABLING		Q-2928-15	
BLDG 6010 GROUND ISOLATION		Q-2928-16	
EXPERIMENT EQUIPMENT-BLOCK DWS		Q-2928-5	
LABORATORY CABLE TRAY- PLAN		Q-2928-4	
BLDG 600 SEL 8108 COMP CABLING		Q-2928-3	
REFERENCE DRAWINGS		DWG. NO.	
DESIGN	WFG	DESIGNED BY	DATE
DESIGNED BY	DATE	CHECKED BY	DATE
DESIGNED BY	DATE	CHECKED BY	DATE
U. W. REYNOLDS			
ORELA DATA ACQUISITION			
BLDG. 6010			
CENTRAL DATA AREA			
COMPUTER EQUIPMENT LAYOUT			
INSTRUMENTATION AND CONTROLS DIVISION			
OAK RIDGE NATIONAL LABORATORY			
OPERATED BY			
UNION CARBIDE CORP.			
DESIGNED BY	WFG	DATE	12/1/64
DESIGNED BY	DATE	CHECKED BY	DATE
Q-2928-2		R11	

LASTED ON DISCHARGE REASON DISCHARGE		OAK RIDGE NATIONAL LABORATORY OPERATED BY UNION CARBIDE CORP.	
FRACTIONAL: 2 1/2 hr DISTILLATE: 2 1/2 hr AQUEOUS: 2 1/2 hr	NAME: <i>W. G. Miller</i> PROJECT: <i>W. G. Miller</i> DATE: <i>11/11/50</i>	SAMPLE: <i>W. G. Miller</i> DATE: <i>11/11/50</i> ANALYST: <i>W. G. Miller</i>	CASE: <i>W. G. Miller</i> DATE: <i>11/11/50</i> ANALYST: <i>W. G. Miller</i>
COMMENTS:		0-2928-2 R

NO.	REVISIONS	DATE	BY	APPD
1	AS	12-11-70		
2				
3				
4				
5				
6				
7				
8				
9				
10				

REFERENCE DRAWINGS		DWG. NO.
DESIGN BY: J. W. REYNOLDS		
ORELA DATA ACQUISITION		
BUILDING 600 LABORATORY		
CABLE TRAY PLAN		
INSTRUMENTATION AND CONTROLS DIVISION		
OAK RIDGE NATIONAL LABORATORY		
UNION CARBIDE CORP.		
DATE: 12-11-70	BY: J. W. REYNOLDS	APPD: J. W. REYNOLDS
Q-2920-4		20

Computer Equipment Layout		Q-2928-2
Sel 8108 Computer Cabling		Q-2928-3
REFERENCE DRAWINGS		DWG. NO.
DESIGNER <i>W.D. [Signature]</i>	DATE 12-1-68	REVISIONS DATE 12-1-68
DESIGNED <i>W.D. [Signature]</i>	DATE 12-1-68	REVISIONS DATE 12-1-68
COORDINATED BY <i>J.W. Reynolds</i>		REVISIONS DATE 12-1-68
PROJECT TITLE ORELA DATA ACQUISITION		
EXPERIMENTER EQUIPMENT BLOCK DIAGRAM		
INSTRUMENTATION AND CONTROLS DIVISION OAK RIDGE NATIONAL LABORATORY OPERATED BY UNION CARBIDE CORP.		
DESIGNED <i>[Signature]</i>	DATE 12-1-68	REVISIONS DATE 12-1-68
DESIGNED <i>[Signature]</i>	DATE 12-1-68	REVISIONS DATE 12-1-68
Q-2928-5

LEGEND:

- Cable tray access. Cable trays are isolated from building ground and tied to experimenter ground plate in lab.
- 2/0 Ground Cable.
- Experimenters Clean Ground
- Laboratory Copper Ground Plate
- Single ground Isolation
- Double ground Isolation
- Cabinet ground Supplied through Isolated ground on Power Cord
- Isolated Pulse Generator Q-509
- Device Controller Q-5098

Computer Equip. Layout				Q-2928-2	
Cable Tray Plan				Q-2928-4	
REFERENCE DRAWINGS					
DWG. NO.		DWG. NO.			
DESIGN	DATE	REVISION	DATE	DESIGN	DATE
MFG	6-8-78				
DESIGN	DATE	DESIGN	DATE	DESIGN	DATE
CHECKED BY				CHECKED BY	
J.W. Reynolds					
PROJECT TITLE					
ORELA DATA ACQUISITION					
BUILDING 6010					
GROUND ISOLATION					
INSTRUMENTATION AND CONTROLS DIVISION					
OAK RIDGE NATIONAL LABORATORY					
OPERATED BY					
UNION CARBIDE CORP.					
DESIGN	DATE	DESIGN	DATE	DESIGN	DATE
6-1-78	6-1-78	6-1-78	6-1-78	6-1-78	6-1-78
PROJECT APPROVAL					
Q-2928-14 Ro					

MICROFILMED

Q-2928-15

REVISIONS		NO.	DATE	BY	APPD.
1

INTERNAL INTERRUPT WIRING FOR DAC 1 & DAC 2

NOTES:

- 1- See SEL Dwg. 130-810177-000, sheet 13, location B3 for source.
- 2- See SEL Dwg. 140-053400-000, sheet 1, location B3 for source of clock.
- 3- See SEL Dwg. 130-810037-000, sheet 8, location A6 (I/O Bus connection 503 & 504). These signals are generated in the Intercomputer Link (PEC/DAC 1), SEL Dwg. 53425, sheet 13, location A6 in the I/O Remoter cabinet.
- 4- See SEL Dwg. 130-810187-000, sheet 13, location B3 for source.

INTERRUPT SWITCH CONNECTOR LABELS

* Shorting plug. All pins shorted together except: pair 312/412 is not connected & pair 107/207 is connected to 108/208. Only the signal half of the pair is shown above.

Computer Cabling		Q-2928-3
REFERENCE DRAWINGS		
WFG 12-172	RPR 11-10-74	
R.P. Rose	J.W. Reynolds	
COORDINATOR: J.W. Reynolds		
PROJECT TITLE		
ORELA Data Acquisition		
BLDG 6010		
SEL 810B COMPUTERS		
INTERRUPT CABLING		
INSTRUMENTATION AND CONTROLS DIVISION		
OAK RIDGE NATIONAL LABORATORY		
UNION CARBIDE CORP.		
DATE: 11/8/72		
Q-2928-15 R0

NOTES:
1. Data Ready Off grounds both the Data Ready signal to the computer and Mpxr. Control to the experimenter. The grounds are isolated from each other.

3	Add Section to Data Ready Sw	4-17-72	WDR	YAL
2	Change Exp. Tag Locations	12-17-72	WDR	YAL
1	Let's Ready ON/OFF SW	8-3-71	WDR	YAL
NO.	REVISIONS	DATE	BY	APPD.
1	U & WDR	10-23-70		

SEL 810B Mpxr Gnd. Isolation - Pnl's.	Q-5036-25
RCVR Cards are Circuit	Q-5072-9C
and Isolating Driver, Single Isolator 0 to 0 Input	Q-5072-13B
and Isolating Driver, Double Isolator 0 to 0 Input	Q-5072-11A
and Isolating Driver, Single Isolator 0 to 0 Out	Q-5072-9B
and Isolating Driver, Dual Isolator 0 to 0 Out	Q-5072-9A
SEL 810B Multiplexer - Scaler Isolation Assy	Q-5036-28

REFERENCE DRAWINGS	DWG. NO.
J. REYNOLDS	

SEL 810B MULTIPLEXER ISOLATION
GROUND ISOLATORS DRIVERS RECEIVERS WIRING

INSTRUMENTATION AND CONTROLS DIVISION OAK RIDGE NATIONAL LABORATORY
OPERATED BY UNION CARBIDE CORP.

Q-5036-25	R3
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3. J. W. Reynolds, N. A. Betz, and D. A. McCully, "ORELA Data Acquisition into Greater than 10^5 Channels through a Priority Multiplexer Operating on a Direct Memory Access and a Program Controlled Device Interface," *IEEE Trans. Nucl. Sci.* NS-17(1): 383-89 (1970).
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5. Iso-Switch Corporation, Data Sheet No. 835A, Costa Mesa, California, p. 1 (1969).
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17. Systems Engineering Laboratories, Inc., *Design Manual, SEL 810B Input/Output Interface*, pp. 3-6 to 3-13 (August 1969).
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APPENDIX A
DRAWING LISTS
FOR
ORNL INSTRUMENTATION AND CONTROLS DIVISION DRAWING SERIES
USED AT
ORELA*

Series	Title
Q-2928	ORELA Data Acquisition
Q-2956	PDP-4 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link
Q-3079	ORELA Digital Multiplexer, Level Matching
Q-5036	Scaler Interface and Four-Channel Priority Multiplexer
Q-5066	Eight-Stage Stacking Buffer Memory
Q-5072	PDP-9 Interface on the SEL 810B/PDP-4/PDP-9 Intercomputer Link
Q-5094	Ground Isolation Receiver and Driver Tester
Q-5098	ORELA Device Controller
Q-5108	Binary Synchronous Communications Interface (SEL Drawing Series 130-100500-000)
Q-5109	ORELA Isolated Pulse Generator
Q-5110	ORELA Digital Multiplexer, Level Matching
Q-5130	ORELA Data Acquisition, Multiplexer-Scaler Tester
Q-5183	Word-Addressed Fixed-Head Disk Logic (SEL Drawing Series 53335)
Q-5184	810B I/O Expander (SEL Drawing Series 53344)
Q-5185	Cathode-Ray Tube Display (SEL Drawing Series 53351)
Q-5186	PEC/DAC 2 or PEC/DAC 3 Intercomputer Link (SEL Drawing Series 53360)
Q-5187	810B/PDP-4 Intercomputer Link (SEL Drawing Series 53422)
Q-5188	PEC/DAC 1 Intercomputer Link (SEL Drawing Series 53425)
Q-5193	Automatic Update Word-Addressed Fixed-Head Disk (SEL Drawing Series 160-100835-000)

* These ORNL Drawing Series are available from the author.

ORELA Data Acquisition
Drawing Series Q-2928

Number	Subtitle
-1	Computer System Block Diagram
-2	Building 6010 Central Data Area, Computer Equipment Layout
-3	Building 6010 SEL 810B Computer Cabling
-4	Building 6010 Laboratory Cable Tray Plan
-5	Experimenter Equipment Block Diagram
-6	CRT Mounting Sketch, Fig. 3.1 of CSP-500-24
-7	Data Collection Equipment Cabinet Layout, Fig. 3.3 of CSP-500-24
-8	System Connector Panel and Connector Details
-9	Automatic Update Word-Addressed Fixed-Head Disk Block Diagram
-10	Multiplexer and Scaler Chassis Connectors
-11	BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors
-12	PDP-10 Computer Equipment, Building 4500, Room 258 Floor Plan
-13	General Electric TDM-330, Data Set Circuit (Sepia of General Electric original)
-14	Building 6010, Ground Isolation
-15	Building 6010, SEL 810B Computers, Interrupt Cabling

PDP-4C Serial 23
ORELA 810B/PDP-4/PDP-9 Link
Drawing Series Q-2956

Number	Subtitle
-30	Module Utilization
-31	Program Interrupts and Skip Bus Expansion
-32	Device Selector Extension
-33	Control and Input from SEL 810B
-35	Output to SEL, Bits 0 to 7
-36	Output to SEL, Bits 8 to 15
-37	PDP-4 Ground Isolators and Power Supply Metalphoto Panels
-38	PDP-4 Ground Isolators, Drivers and Receivers

ORELA Digital Multiplexer
Level Matching
Drawing Series Q-3079

Number	Subtitle
-1	True: -3 volts to +3 volts, False: 0 volts to 0 volts (OBSOLETE, see Dwg. No. Q-5110-X)
-2	DEC Connector Block NIM Mounting Bar
-3	Front Module Panel (OBSOLETE, see Dwg. No. Q-5110-1X)
-4	Rear Module Panel (OBSOLETE, see Dwg. No. Q-5110-1X)
-5	Level Matching Module Assembly and Details
-10A	Cable Driver Circuit, True: +3 to -3 volts, False: 0 to 0 volts
-10B	Etched Circuit for Cable Driver Circuit

Scaler Interface

Drawing Series Q-5036
 SEL Drawing Series 53320 (with Revisions)
 Logic Diagram, Unit 1R2

Number	Subtitle
-1	Decode Unit 22
-2	I/O Sync Logic
-4	Scaler Interrupt Control
-5	Scaler Address Control
-6	Scaler Input Data Register Word #1 Part #1 (bits 0-7)
-7	Scaler Input Data Register Word #1 Part #2 (bits 8-15)
-8	Scaler Input Data Register Word #2 Part #1 (bits 0-7)
-9	Scaler Input Data Register Word #2 Part #2 (bits 8-15)
-10	Scaler Pulse Output Part 1 (Pulse 1 to 6)
-11	Scaler Pulse Output Part 2 (Pulse 7 to 12)
-21	I/O Bus Bits 0-3
-22	I/O Bus Bits 4-7
-23	I/O Bus Bits 8-11
-24	I/O Bus Bits 12-15
	SEL 810B Multiplexer-Scaler Isolation
-29	Assembly, Four-Wide Nuclear Instrument Module for DEC A, K, R, M Series Logic Cards
	SEL 810B Scaler Isolation
-30	Master Receivers and Drivers
-31	Master Receivers and Drivers Panels

Four-Channel Priority Multiplexer

Drawing Series Q-5036 (with Revisions)

SEL Drawing Series 53320

Digital MUX

Number	Subtitle
-2	I/O Sync Logic
-3	Decode Unit 23
-12	Strobe Register
-13	Priority Part 1 (word A,B,C&D - Channel 0 & 1)
-14	Priority Part 2 (word E,F,G&H - Channel 2 & 3)
-15	Input Gates - A&B
-16	Input Gates - C&D
-17	Input Gates - E&F
-18	Input Gates - G&H
-19	Strobe Generator
-20	BTC Interface
	<u>Logic Diagram, Unit 1R2</u>
-21	I/O Bus Bits 0-3
-22	I/O Bus Bits 4-7
-23	I/O Bus Bits 8-11
-24	I/O Bus Bits 12-15
	SEL 810B Multiplexer Isolation
-25	Ground Isolators, Drivers, and Receivers
-26	Ground Isolators Front and Rear Panels
-27	Multiplexer Input Ground Isolators, Drivers, and Receivers
-28	Multiplexer Input Ground Isolators, Front and Rear Panels
	SEL 810B Multiplexer-Scaler Isolation
-29	Assembly, Four-Wide Nuclear Instrument Module for DEC A, K, R, and M Series Logic Cards

Stacking Buffer Memory
Drawing Series Q-5066

Number	Subtitle
-1	Interfacing Control Logic
-2	Memory Registers 1 thru 4 Logic
-3	Memory Registers 5 thru 8 Logic
-4	Three-Wide NIM Backplate
-5	Metalphoto Panel

ORELA PDP-9/810B Interface
Drawing Series Q-5072

Number	Subtitle
-1	Program Interrupt Skip and Data Transfer Control
-2	Data Channel Control
-3	Input and Output Gating
-4	Cabling and Device Selectors
<u>Circuit Cards for Ground Isolation</u>	
-5	GND Isolating Driver 0 to -3 Input
-6	Etched Circuit Board for -5
-7	GND Isolating Driver -3 to 0 Input
-8	Etched Circuit Board for -7
-9A	GND Isolating Receiver, Dual Isolator, 0 to -3 Out
-9B	GND Isolating Receiver, Single Isolator, 0 to +3 Out
-9C	GND Isolating Receiver, Dual Isolator, 0 to +3 Out
-10	Etched Circuit Board for -9A, -9B, & -9C
-11A	GND Isolating Driver, Double Isolator, 0 to +3 Input
-12	Etched Circuit Board for -11A
-13A	GND Isolating Driver, Double Isolator, +3 to 0 Input
-13B	GND Isolating Driver, Single Isolator, +3 to 0 Input
-14	Etched Circuit Board for -13A and -13B
-15	SEL 810B Ground Isolators, Master Receivers, and Drivers
-16	810B Ground Isolators, 810B Power Supply <u>+12</u> v DC, Panels
-17	Module Utilization

Ground Isolation Driver and Receiver Tester
Drawing Series Q-5094

Number	Subtitle
-1	Circuit
-2	Metalphoto Panel

ORELA Device Controller
Drawing Series Q-5098

Number	Subtitle
-1	Select Decode and Pulses X001 thru X312
-2	Select Decode and Pulses X401 thru X712
-3	Data Input Channel 0 to 3, Word 1
-4	Data Input Channel 0 to 3, Word 2
-5	Data Input Channel 4 to 7, Word 1
-6	Data Input Channel 4 to 7, Word 2
-7	Block Diagram
-8	Special Circuit Card Diagrams
-9A	Back Panels and Side Plates
-9B	Front Panel Mounting Rails
-9C	Front Panels
-9D	Metalphoto Nameplates
-10	Control Registers (JAH), 5 & 10 Meter Paddles, Beam Stop, and Hot Sample Changer Motor Control Status
-11	OPERATE, Scaler Control, Lamp Drivers, and Hot Sample Motor Control Pulses (JAH)
-12	Monitor Switch Receivers (JAH)
-19	Module Utilization (JAH) and Cabling Diagram
-20	Control Registers (RLM), 5-Meter Filters, and 40-Meter Sample Changer
-21	OPERATE, Scaler Control, and Lamp Drivers (RLM)
-22	Switch Receivers and 40 Meter Interface (RLM)
-28	40-Meter Control (RLM)
-29	Module Utilization (RLM) and Cabling Diagram
-30	Control Register (GDS), Beam Stop, and Linear Filters 1 to 10
-31	OPERATE, Scaler Control, Lamp Drivers, and Positive Pulses PX301 thru PX306 (GDS)
-32	Monitor Switch Receivers (GDS)
-39	Module Utilization (GDS) and Cabling Diagram

Binary Synchronous Communications Interface
Drawing Series Q-5108

Number	Subtitle
-0	Data Flow Logic Block Diagram
	<u>Logic Diagram, BSCI</u>
	Sepia of SEL Drawing Series 130-100500-000
-1	Unit Decode
-2	I/O Sync Logic
-3	Test Logic
-4	BTC Interface
-5	Priority Interrupt Logic
-6	CEU Storage
-7	Output Data Control
-8	Word Timing
-9	Read Data Control
-10	I/O Register 1 Byte 0
-11	I/O Register 1 Byte 1
-12	Data Buffer Control
-13	I/O Register 2 Byte 0
-14	I/O Register 2 Byte 1
-15	Output Parity Generator
-16	S/R Data Multiplexer Byte 0
-17	S/R Data Multiplexer Byte 1
-18	Shift Register Byte 0
-19	Shift Register Byte 1
-20	Input Parity Check
-21	CRC Control
-22	CRC Polynomial Generator
-23	CRC Compare Logic
-24	Control Panel Interface
-25	Time Out Logic
-26	Time Out Logic
-27	Read Data Control

Number	Subtitle
-28	Circuit Complement
-29	Circuit Complement
<u>Sepia of SEL Drawing Series Q-5108</u>	
-30	138-100052, Sheet 1 Block Diagram, BSCI
-31	160-100277, Sheet 1 Isolation Switch Assy.
-32	141-100311, Sheet 1 Card Location BSCI
-33	160-900105, Sheet 1 Current Loop Receiver Assy.
-34	160-900106, Sheet 1 Coax Terminator Assy.
-35	160-900093, Sheet 1 Universal Counter Assy.
-36	160-900094, Sheet 1 Logic Mix Assy.

ORELA Isolated Pulse Generator
Drawing Series Q-5109

Number	Subtitle
-1	Select Device X0 and Pulse X001 thru X012
-2	Not used
-3	Front and Rear Panels
-4	Module Assembly

ORELA Digital Multiplexer, Level Matching
Drawing Series Q-5110

Number	Subtitle
-1	Eldorado Clock Isolation Driver Circuit
-2	TMC TF 440-10 & 8192 ADC ND 2200 Isolation Driver Interface
-3	Time Digitizer EGG Model TDC-100 and 8192 ADC ND 2200 Isolation Driver Interface
-4	Multiparameter Patch Board
<u>Metalphoto Panels</u>	
-11	Eldorado Clock
-12	TMC FD 440-10 & 8192 ADC ND 2200
-13	EGG TDC-100 & 8192 ADC ND 2200

ORELA Data Acquisition
Drawing Series Q-5130

Number	Subtitle
-1	Multiplexer-Scaler Selectable Pattern Tester
-2	Not Used
-3	Front and Rear Panels

I/O Expander
 Drawing Series Q-5184
 Sepia of SEL Drawing Series 53344
 Logic Diagram, 810B I/O Expander

Number	Subtitle
-1	Output Control Lines
-2	Output Control Lines
-3	Input Control Lines
-4	Data Controls
-5	Data Bus, Bit 1-3
-6	Data Bus, Bit 4-6
-7	Data Bus, Bit 7-9
-8	Data Bus, Bit 10-12
-9	Data Bus, Bit 13-15
-10	BTC Remoter #1, BTC4
-11	BTC Remoter #2, BTC5

Cathode-Ray Tube Display
 Drawing Series Q-5185
 Sepia of SEL Drawing Series 53351
 Logic Diagram, 1R1

Number	Subtitle
-1	Unit Decode Logic
-2	I/O Sync Logic
-3	Unit I/O BTC Control
-4	Data Input and Storage Reg.
-5	Data Out, CRT Interface
-6	Increment Counter and Gates
-7	CEU Buffer Control Logic
-8	D/A Storage Reg. & Control Logic
-9	10-Bit D/A
-10	Schematic Diagram, Photo Pen (SEL Dwg. No. 53418)

PEC/DAC 2 or DAC 3 Intercomputer Link

Drawing Series Q-5186

Sepia of SEL Drawing Series 53360 (ORNL Revised)

Logic Diagrams

Number	Subtitle
-1	Unit Decode Logic, Computer No. 1
-2	I/O Sync Logic, Computer No. 1
-3	BTCI #1
-4	Computer #1 Link Output Bits 0-7
-5	Computer #1 Link Output Bits 8-15
-6	Computer #1 Link Output Bits 8-15/16-23
-7	Unit Decode Logic Computer #2
-8	I/O Sync Logic Computer #2
-9	BTCI #2
-10	Computer #2 Link Output Bits 0-7
-11	Computer #2 Link Output Bits 8-15
-12	Computer #2 Link Output Bits 8-15/16-23
-13	Word Interrupts
-14	Circuit Complement

SEL 810B/PDP-4/PDP-9 Link Interface

Drawing Series Q-5187

Sepia of SEL Drawing Series 53422

Logic Diagrams, PDP-4 Link

Number	Subtitle
-1	Unit I/O, Sync Logic
-2	Sync Logic
-3	BTC Interface
-4	Interrupt Logic
-5	Interrupt Logic
-6	I/O Bus Output Buffer, Bits 0-7
-7	I/O Bus Output Buffer, Bits 8-15
-8	I/O Bus Input Buffer, Bits 0-7
-9	I/O Bus Input Buffer, Bits 8-15

PEC/DAC 1 Intercomputer Link
Drawing Series Q-5188
Sepia of SEL Drawing Series 53425
Logic Diagram, Intercomputer Link

Number	Subtitle
-1	Unit Decode Logic, DAC 1
-2	I/O Sync Logic, DAC 1
-3	BTCI #1, DAC 1
-4	Computer #1, Output Bits 0-7
-5	Computer #1, Output Bits 8-15 (Not Used)
-6	Computer #1, Output Bits 8-15
-7	Unit Decode Logic, PEC
-8	I/O Sync Logic, PEC
-9	BTCI #2, PEC
-10	Computer #2, Output Bits 0-7
-11	Computer #2, Output Bits 8-15 (Not Used)
-12	Computer #2, Output Bits 8-15
-13	Word Interrupts
-14	Complement List
-15	Test Logic and EOR Interrupts

Automatic Update Word-Addressed Fixed Head Disk
Drawing Series Q-5193
Sepia of SEL Drawing Series 130-100835-000
Logic Diagram, Word-Addressed Fixed-Head Disk

Number	Subtitle
-1	Logic Diagram I/O Interface Logic WAFHD
-2	Logic Diagram I/O Sync Logic
-3	Logic Diagram Test Logic WAFHD
-4	Logic Diagram BTCI Control WAFHD
-5	Logic Diagram BTC 2 Control (Data) WAFHD
-6	Logic Diagram Priority Interrupt Logic WAFHD
-7	Logic Diagram I/O Bus WAFHD
-8	Logic Diagram Command Storage Logic WAFHD
-9	Logic Diagram Track Buffer Management Logic WAFHD
-10	Logic Diagram Data Buffer Management Logic WAFHD
-11	Logic Diagram Word Count Logic and Index Delay WAFHD
-12	Logic Diagram Active Word Control WAFHD
-13	Logic Diagram Sync Pattern and Parity Generator WAFHD
-14	Logic Diagram Data Register 1 Byte 0-1 WAFHD
-15	Logic Diagram Data Register 2 Byte 0-1 WAFHD
-16	Logic Diagram Data Register 3 Byte 1-0 Track Address Register WAFHD
-17	Logic Diagram Track and Increment Register WAFHD
-18	Logic Diagram R5 Data Delay 512 Word Storage Register
-19	Logic Diagram P6T Rack Delay 512 Word Storage Register
-20	Logic Diagram Fuel Adder (Update) WAFHD
-21	Logic Diagram Serial Data Register WAFHD
-22	Logic Diagram Disc Interface WAFHD
-23	Logic Diagram Status Panel WAFHD
-24	Logic Diagram Timing
-25	Logic Diagram Timing
-26	Logic Diagram Circuit Complement WAFHD
-27	Card Location and Complement List WAFHD (SEL Dwg. No. 100144)
-28	DAC-3 Disc Buffer Register 512 Word $\times$ 8 Bit Storage PC Board

APPENDIX B

PERFORMANCE SPECIFICATIONS AND RELATED DOCUMENTS FOR THE
ORELA DATA HANDLING SYSTEM

Proposal to Acquire a Data Handling System for the Oak Ridge Electron Linear Accelerator, W. R. Burrus, J. A. Harvey, F. C. Maienschein, J. W. Reynolds, and J. G. Sullivan, ORNL/TM-1746, January 17, 1967.

Instrument Department Performance Specification CSP-500-3 Preliminary for ORELA Data Acquisition Computer System, J. W. Reynolds and J. W. Woody, Jr., January 17, 1967.

Instrument Department Performance Specification CSP-500-3 Revised for ORELA Data Acquisition Computer System, J. W. Reynolds and J. W. Woody, Jr., April 17, 1967.

Application Notes on the Immediate Analysis Computer Display System for ORELA Data Acquisition and Handling, J. W. Reynolds, ORNL/TM-2116, January 30, 1968.

Instrument Department Performance Specification CSP-500-3 for the Immediate Analysis and Coordinating Computer, J. W. Reynolds and J. W. Woody, Jr., May 29, 1968.

Instrument Department Performance Specification CSP-500-6 Revision A for the Immediate Analysis and Coordinating Computer, J. W. Reynolds and J. W. Woody, Jr., July 11, 1969.

Communication Standards for Instrument Department Performance Specifications CSP-500-6 Revision (July 11, 1969), Purchase Order 51X-23900V, J. W. Reynolds and N. A. Betz, April 20, 1970.

Instrument Department Performance Specification CSP-500-13 for A Binary Synchronous Communications Interface to be Used with Systems Engineering Laboratories 810B Computer, J. W. Reynolds and J. W. Woody, Jr., June 12, 1970.

Instrument Department Performance Specification CSP-500-24 for ORELA Data Acquisition Computer Three, Phase IIIA, J. W. Reynolds and J. W. Woody, Jr., November 5, 1971; Revision A - February 18, 1972; Revision B - March 10, 1972; Revision C - March 20, 1972; Revision D - July 28, 1972.

APPENDIX C

COMPUTER HARDWARE CONFIGURATION

Mainframe

All DACs and the PEC have memory parity, stall alarm, power fail safe, Variable Base Register (VBR), Index Register, and a 60-Hz Clock.

DAC 1 and DAC 3 have five Block Transfer Controllers (BTCs) and three groups of priority interrupts.

DAC 2 and the PEC have eight BTCs and four groups of priority interrupts.

Peripherals

All DACs have the following peripherals:

<u>SEL Number</u>	<u>Octal unit number</u>	<u>Description</u>
80-712-K35A	1	KSR Console Typewriter*
81-525A	2	Paper Tape Reader (300 CPS) and Punch (110 CPS) [†]
D53335 and 130-100835-000	20	Word-Addressed Fixed-Head Disk [‡]
2191	22	Scaler Interface
2191	23	Digital Data Multiplexer
711401B	24	PEC/DAC Intercomputer Link [§]
040103-1	26	Cathode-Ray Tube Display with Light Pen

* ASR on DAC 2 and 3.

[†] On DAC 1 only.

[‡] DAC 1 has 786,432 words on 512 tracks, DAC 2 has 393,216 words on 256 tracks, and DAC 3 has 1,048,576 words on 1024 tracks. The disk on DAC 3 has an instruction, Update, which is not in either DAC 1 or DAC 2.

[§] Two links are located at the PEC in the mainframe and I/O Remote Cabinet. The third link is on DAC 3.

The PEC has the following peripherals:

<u>SEL Number</u>	<u>Octal unit Number</u>	<u>Description</u>
80-712-K35A	1	KSR Console Teletype
81-525A	2	Paper Tape Reader (300 CPS) and Punch (110 CPS)
81-450A	4	Card Reader (400 cpm)
81-610-98A and 81-615-14A (7 track drive) with 81-615-07A (9 track option)	6	Magnetic Tape Controller for eight tape units with two nine-track magnetic tape units (45 in./sec, 800 bytes/in.) attached
81-810A	11	12-in. Calcomp plotter
091518	25	PEC/PDP-4 Link
711401B	31,32,33	PEC/DAC Intercomputer Link
552090	43	Binary Synchronous Communications Inter- face Unit

APPENDIX D

TECHNICAL, DESIGN, OPERATION, AND MAINTENANCE MANUALS
FOR THE ORELA DATA ACQUISITION SYSTEM

The following technical, design, operation, and maintenance manuals are published by SEL, Inc.:

<u>Title</u>	<u>Publication Number</u>
Reference Manual, SEL 810B General Purpose Computer, November 1968	301-095118
Design Manual, SEL 810B Input/Output Interface, August 1969	310-095117
Technical Manual, Data Acquisition System, 3 Vols., June 1969	315-219100
Technical Manual, SEL 810B General Purpose Computer, May 1969	303-095019
Drawings Manual, SEL 810B General Purpose Computer, May 1969	304-095116
Operating Reference Manual, SEL 810A/810B Operating System, July 1969	312-095071
Technical Manual, SEL 810A/810B Assembler Program, November 1968	322-095094
Technical Manual, SEL 810A/810B Diagnostics, February 1969	322-095061
Reference Manual, SEL 810/840 Computer Series FORTRAN IV, November 1968	323-095054
Reference Manual, SEL 810A/810B Assembler, November 1968	323-095052
Operator Manual, SEL 810A/810B Computer/Peripheral, January 1969	302-095064
Technical Manual, Models 80-711 and 80-712 Type-writer Systems, March 1968	305-095070
Technical Manual, Model 80-500 Series Paper Tape System, October 1967	305-095065

<u>Title</u>	<u>Publication Number</u>
Technical Manual, Model 80-450 Series Card Reader (Uptime), December 1967	305-095014
Technical Manual, Model 80-800 Series X-Y Plotter, November 1967	305-095012
Technical Manual, Models 80-610 and 80-615 Series Magnetic Tape Systems, August 1969	305-095005
Technical Manual, Model 80-733A Shuttle Line Printer, September 1968	305-095085
Technical Manual, Intercomputer Data Link, April 1969	306-701401
Technical Manual, Binary Synchronous Communications, April 1972	315-552090
Interface Unit, April 1970	

The following publications contain detailed electro-mechanical information on the peripheral equipment:

<u>Title</u>	<u>Manufacturer</u>
Technical Manual, Models ASR-35, KSR-35, and KSR-33 Teletype	Teletype Corp.
Technical Manual, Model BRPE Tape Punch	Teletype Corp.
Technical Manual, Model 13510 and 13520 Fixed-Head Disk	Digital Development Corp.
Technical Manual, Model 2500, Paper Tape Reader	Digitronics
Maintenance Manual, Model 400 Card Reader	Uptime
Technical Manual, Model 565 X-Y Plotter	Calcomp
Maintenance Manual, Model TM-9 Magnetic Tape Transport	Ampex
Technical Manual, Series 4000 Shuttle Printer	Mohawk
Operating and Service Manual, Model 1300A X-Y Display	Hewlett-Packard
Technical Manual LBI-15732, TDM-330 Data Set	General Electric

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APPENDIX E

PROGRAMMING NOTES FOR ORELA

This appendix contains the Unit Numbers, BTC assignments, and Interrupt assignments for the DACs and the PEC in the ORELA Data Acquisition System. Programming Notes for each nonstandard unit define the Command External Unit (CEU) and Test External Unit (TEU) instruction second word formats, list any programming cautions, and briefly describe each interrupt generated or used by the unit.

<u>Unit</u>	<u>Description</u>
'20	Word-Addressed Fixed-Head Disk
'22	Scaler Interface
'23	Four-Channel Priority Multiplexer
'24	Intercomputer Link
'25	SEL 810B/PDP-4/PDP-9 Link
'26	Cathode-Ray Tube Display 6CRT Light Pen Function Points 6CRT Teletype Commands
'43	Binary Synchronous Communications Interface

UNIT NUMBERS

<u>Description</u>	<u>Octal</u>
35 ASR or KSR Typewriter	1
High-Speed Paper Tape System	2
Card Reader	4
Line Printer	5
Tape Control Unit	6
X-Y Plotter	11
Word-Addressed Fixed-Head Disk	20
Scaler Interface	22
Four-Channel Priority Multiplexer	23
CRT Display	26
DAC 1, 2, or 3 to PEC	24
PEC/PDP-4	25
PEC/DAC 1	31
PEC/DAC 2	32
PEC/DAC 3	33
PEC/IACC	43

SELBTC.LST		BTC ASSIGNMENTS		JULY 18, 1972	
CORE					
BTC	LOCATION	DAC 1,2 & 3	PEC	DAC 2 AS PEC	
1 FWA WC	'1060 '1061	DISK TRACK	DISK	DISK TRACK	
2 FWA WC	'1062 1063	DISK DATA	MAGNETIC TAPE	DISK DATA	
3 FWA WC	1064 1065	MULTIPLEXER	IACC LINK	MULTIPLEXER	
4 FWA WC	1066 1067	PEC LINK	DAC 1 LINK	MAGNETIC TAPE	
5 FWA WC	1070 1071	CRT DISPLAY	DAC 2 LINK	CRTD & PDP-7 LINK	
6 FWA WC	1072 1073	-----	DAC 3 LINK	DAC 1 & 3 LINKS	
7 FWA WC	1074 1075	-----	PDP-4/9 LINK	PDP-419 LINK	
8 FWA WC	1076 1077	-----	PDP-7 LINK	IACC LINK	

SELPIA.LST

PRIORITY INTERRUPT ASSIGNMENTS

5-7-73

DAC 1	DAC 2	DAC 3	GROUP-LEVEL	ADDRESS	PEC
MEMORY PARITY ERROR			0-1	'1002	
MEMORY PARITY ERROR			0-2	'1003	
DISK PARITY OR PROGRAM ERROR			0-3	'1004	DISK PARITY OR PROGRAM ERROR
MAGNETIC TAPE WORD TRANSFER			0-4	'1005	BSCI TERMINATE TRANSMIT
DISK, BTC 1 INITIALIZE COMPLETE			0-5	'1006	CARD READER
MULTIPLEXER ERROR			0-6	'1007	
DISK, BTC 2 COMPLETE			0-7	'1010	
MULTIPLEXER, BTC 3 COMPLETE			0-8	'1011	
KSR OR ASR INPUT			0-9	'1012	KSR INPUT
KSR OR ASR OUTPUT			0-10	'1013	KSR OUTPUT
CRT LIGHT PEN			0-11	'1014	
MASK			0-12	'1015	MASK
60 HERTZ CLOCK			1-1	'1022	
CRT, BTC 5 COMPLETE			1-2	'1023	
			1-3	'1024	
			1-4	'1025	
			1-5	'1026	
			1-6	'1027	
			1-7	'1030	
			1-8	'1031	
			1-9	'1032	
			1-10	'1033	
DISK REVOLUTION NOT USED			1-11	'1034	
CRUNCH			1-12	'1035	CRUNCH
SCALER OVERFLOW			2-1	'1042	
SCALER DATA READY			2-2	'1043	
			2-3	'1044	BSCI ERROR
			2-4	'1045	MAGNETIC TAPE WORD TRANSFER
LINK			2-5	'1046	LINK
			2-6	'1047	MAGNETIC TAPE END OF RECORD
PEC, BTC 4 COMPLETE			2-7	'1050	DAC 1, BTC 4 COMPLETE
			2-8	'1051	DAC 2, BTC 5 COMPLETE
PEC INPUT			2-9	'1052	DAC 3, BTC 6 COMPLETE
HS PAPER TAPE READER (DAC 1)			2-10	'1053	PDP-4/9, BTC 7 COMPLETE
HS PAPER TAPE PUNCH (DAC 1)			2-11	'1054	
TELETYPE ESCAPE			2-12	'1055	
			3-1	'1102	BSCI CONTROL
			3-2	'1103	DAC 1 OUTPUT INITIALIZE
			3-3	'1104	DAC 2 OUTPUT INITIALIZE
			3-4	'1105	DAC 3 INPUT
*****DISTRIBUTION*****			3-5	'1106	PDP-4/9 INPUT
*** J.G.CRAVEN ***			3-6	'1107	
*** CHANGE LOG ***			3-7	'1110	60 HZ CLOCK
*** CONSOLE (4) ***			3-8	'1111	CALCOMP END OF EXECUTE
*** J.W.REYNOLDS ***			3-9	'1112	LINE PRINTER END PRINT
*** R.P.ROSENBAUM ***			3-10	'1113	HS PAPER TAPE READER
*****			3-11	'1114	HS PAPER TAPE PUNCH
			3-12	'1115	TELETYPE ESCAPE

7XXX EXPERIMENTERS DISPATCH ROUTINE

<u>Entry*</u>	<u>Parameters</u>	<u>Function</u>
A	-2	Delete data and parameter files.
B	-1, X, NG	Input parameters from either the teletype (if X = 1), the paper tape reader (if X = 2), or the card reader (if X = 4).
C	0	Type out counters.
D	1	Continue experiment.
E	2	Display data. [†]
F	3, MTU, ID	Stop run and dump onto magnetic tape.
G	4	Stop run.
H	5, MC, CP	Clear channels and start run (Code: CRTL T). ^{††}
I	6	Input comments (two carriage returns terminates).
J	7	Output comments.
K	8, 1	Type out crunching parameters.
	8, 5	Line print crunching parameters.
L	9, MTU, ID	Restore data from tape to disk.
M	10, MTU, ID	Add data from tape to disk.
N	11, MTU, ID	Subtract tape data from disk data.
O	12, -5	Line print all scalars.
	12, 0	Type all scalars.
	12, N	Type scalars for position card N (1-16).

MUST DO ENTRY B BEFORE ENTRY P

P	13, -X	Input position cards from either the teletype (if X = 1), the paper tape reader (if X = 2), or the card reader (if X = 4).
	13, X	Type the position cards (if X = 1) or line print the position cards (if X = 5).
Q	14, -1, CP	Force a cycle to the position card, CP.
R	15	Give status of scaler program.

* Entries A-N are standard for all experimenters.

[†] See 6CRT Light Pen Function Points and Teletype Commands.

^{††} Each experimenter has an assigned code.

CP = starting card position,
NG = number of group cards,
MC = multiplexer channel,
ID = run number identification,
MTU = magnetic tape unit number, if negative rewind the tape before using.

NONSTANDARD UNITS

There are seven nonstandard units in the ORELA Phase I system of computers. They were designed by SEL to specifications* provided by ORELA. All of the units have been modified as a result of use to increase their performance capability.

<u>Octal unit number</u>	<u>Description</u>
'20	Word-Addressed Fixed-Head Disk
'22	Scaler Interface
'23	Four-Channel Priority Multiplexer
'24	PEC/DAC Intercomputer (DAC Unit Number)
'25	PEC/PDP-4 Link
'26	Cathode-Ray Tube Display
'31, '32, '33	PEC/DAC Intercomputer Links (unit numbers for PEC/DAC links of the PEC)
'43	Binary Synchronous Communications Interface, IACC Communications Link

If bit numbers are missing (noted by an asterisk) under the TEU and CEU second word headings it is best to place zeros in the missing bit locations, as these locations may eventually have some function. Some bits have a function in both states.

The following rules apply to the TEU and CEU second words in all SEL peripherals:

1. CEU Second Word

- (a) Inputting a BTC Current Word Address (CWA) cannot be combined with Read, Write, or Initialize BTC.

2. TEU Second Word

- (a) Any combination of functions may be used.
- (b) Skip is usually the "go" condition. If functions are combined and any one of them yields the no-skip condition, the next instruction after the TEU second word is executed (instead of being skipped).

* See Appendix B.

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Word-Addressed Fixed-Head Disk
Unit '20

<u>Bit</u>	<u>CEU Second Word</u>	<u>Bit</u>	<u>TEU Second Word</u>
0	Initialize track and data BTC's	0	Skip if disk is on-line
1	Connect interrupts	1	Skip if no parity error
2	Parity or Program Error interrupt	2	Skip if disk is not busy
3	Disk revolution not used	3	Skip if no program error
4	*		††
5	*		
6	Transfer track CWA		
7	*		
8	*		
9	Update		
10	*		
11	$\frac{0\ 1\ 2\ 3}{0\ 0\ 1\ 1}$ interleave [†]		
12	0 1 0 1		
13	Transfer data CWA		
14	Write		
15	Read		

* Not used.

[†] 0 and 1 on Update WAFHD.

^{††} All other bits are not used.

Notes:

- (1) The disk uses two BTC channels: one for track address and a second for data.
- (2) Eleven microseconds is the minimum time available at the completion of one revolution before the next instruction must be accepted to insure initialization before the disk index reference point. A disk revolution will be skipped if the CEU is not executed within this window. The minimum time occurs from an interleave 3 (1 on the Automatic-Update WAFHD) instruction to any other interleave.
- (3) Update instruction is only available on the 10⁶ word disk on DAC 3.

Programming Cautions:

- (1) Error interrupts occur before there is time to test for an error with a TEU instruction.
- (2) Both BTCs must access the same number of words in an interleave; otherwise, a Program Error may be generated.

Interrupts:

Parity or Program Error. A test for either of these errors can be made with a TEU instruction. A Program Error will occur if word transfers through the BTCs attached to the disk are prevented by either the software or the hardware; for instance, no response to a CEU to some other unit could hang up the machine in an I/O Hold condition.

Disk Revolution Not Used. The DRNUI signal generates an interrupt that is produced when a disk revolution is not used to read, write, or update. 7RUN of ODAR uses it along with BTC2 Complete Interrupt to control the disk.

BTC2 Complete. The BTC2 Complete signal generates an interrupt that indicates completion of a transfer to or from the disk. Another command is accepted by the Automatic-Update WAFHD at this time, but execution is delayed until the Update-Write cycle is completed. This is the hardware End of Block signal, 2ENDOB.

BTC1 Initialization Complete. The BTC1 Initialization Complete signal generates an interrupt that occurs when the Word Count has been transferred from core into a register in BTC1. It allows the programmer to change the First Word Address (FWA) and Word Count (WC). BTC1 and BTC2 Complete occurs some time after this interrupt.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
"0"											2		1	4		2	1
											Group		Scaler Select				

- (1) Thirty-two-bit data words are gated into two 16-bit buffer registers by a Load Word 1 and Load Word 2 pulse. Each Load Word pulse must be followed by an AIP or MIP* instruction to transfer the word from a buffer register into the computer.
- (2) Sixteen-bit data words on a Scaler Input Bus are routed to the I/O Bus as a result of a Scaler Data Ready Priority interrupt and a Gate Input Bus control pulse. There is no buffer register on this input; therefore, the incoming data must remain constant.
- (3) There are no test instructions for the Scaler Interface.

* Instruction mnemonics: Accumulator Input from Peripheral Unit, Memory Input from Peripheral Unit. See Systems Engineering Laboratories, Inc., *Reference Manual, SEL 810B General Purpose Computer*, Publication No. 301-095118 (November 1968).

(4) To send a pulse:

```
CEU '22
DATA 1      Pulse Address P01--
BRU *-2
CEU '22
DATA '100001    Pulse P0101
BRU *-2
```

(5) To read a word:

```
LOOP CEU '22
    DATA 1          Address 0-1
    BRU *-2
    CEU '22
    DATA '110000    Load Word 1
    BRU *-2
    AIP '22
    BRU ERR          Something is wrong
```

Programming Cautions:

A delay of four machine cycles must be included between an Address Mode instruction and a Pulse Mode instruction if a Load Word bit is set.

Interrupts:

Scaler Data Ready. When this interrupt occurs, data are available on the 16-bit Scaler Input Bus.

Scaler Overflow. The use of this interrupt has not been assigned.

Scaler Channel X. These four interrupts are triggered and used by each experimenter. Their use is defined by his control program.

Four-Channel Priority Multiplexer Unit '23

CEU Second Word

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

↑
Initialize BTC

Transfer CWA

Notes:

- (1) The FCPM is an input device under BTC control. It cannot be operated with AIP or MIP* instructions.
- (2) There are no test instructions for the multiplexer.

Programming Cautions:

- (1) Make certain that the BTC Complete interrupt level is enabled before the BTC is initialized.
- (2) Execution of a second CEU '23 will steal the multiplexer from the first CEU '23 before it terminates.
- (3) The word count must be even; otherwise, a multiplexer error will be generated on completion of a block transfer.

Interrupts:

Multiplexer Error. The Multiplexer Error interrupt is used to increment a double precision counter in 7MUL that can be printed out by a SYST entry zero. An Input Bursts Used (IBU) count for each experimenter is incremented if the multiplexer error prevents completing a burst. The Multiplexer Error Counter in 7MUL is set to zero by a reset command (----) or by restarting the monitor at location '1700.

BTC3 Complete. This interrupt is used to control the current multiplexer input buffer location and to initiate the CRUNCH interrupt. This is the hardware End of Block signal, 3ENDOB.

CRUNCH. The software-triggered CRUNCH interrupt is used to route each event in a block of data to the experimenter's CRUNCH routine 7XXX (XXX are the experimenter's initials).

* Instruction mnemonics: Accumulator Input from Peripheral Unit, Memory Input from Peripheral Unit. See Systems Engineering Laboratories, Inc., *Reference Manual, SEL 810B General Purpose Computer*, Publication No. 301-095118 (November 1968).

Multiplexer Channel X. These four interrupts are triggered and used by each experimenter. Their use has not been specified by any program.

Intercomputer Link

PEC/DAC 1 Link, Unit '31/'24

PEC/DAC 2 Link, Unit '32/'24

PEC/DAC 3 Link, Unit '33/'24

<u>Bit</u>	<u>CEU Second Word</u>	<u>Bit</u>	<u>TEU Second Word</u>
0	Initialize BTC	0	*
1	*	1	*
2	*	2	Skip if link is not busy
3	*	3	*
4	I/O Input/Output	4	*
5	Output interrupt. Bit 4 must be 0.	5	*
6	Clear output buffer	6	*
7	*	7	*
8	*	8	*
9	*	9	*
10	*	10	*
11	*	11	*
12	*	12	*
13	Transfer CWA	13	*
14	*	14	*
15	*	15	*

* Not used.

Notes:

- (1) Link tests BUSY if either computer has initialized its BTC.
- (2) Interrupts are designated by their engineering labels.
- (3) An On-Off Line switch in each PEC/DAC Link can be used to turn off the link interrupt to the PEC and DAC. The normal mode is ON-LINE.
- (4) The function of bits 5 and 6 has been changed from that listed in the SEL Intercomputer Link Manual.

Programming Cautions:

The links will always accept a CEU instruction. The second CEU will override a transfer that has been started but not completed by the first CEU.

Interrupts:

Output. This interrupt is generated by each end of an intercomputer link to request attention by the other computer. It can be triggered independently of all other CEU functions. Note that it has been separated from the initialization requirement of the link as supplied by SEL Model 711401B Intercomputer Link.

BTC Complete. This is an interrupt that signals to the program that the transfer of a block of data has been completed. This is the hardware End of Block signal, 4ENDOBB in the DACs and 4ENDOBB, 5ENDOBB, and 6ENDOBB in the PEC for the links to DAC 1, 2, and 3 respectively.

PEC/PDP-4/PDP-9 Intercomputer Link
Unit '25

<u>Bit</u>	<u>CEU Second Word</u>	<u>Bit</u>	<u>TEU Second Word</u>
0	Initialize BTC	0	*
1	*	1	*
2	*	2	Skip if link is not busy
3	*	3	Skip if link is on-line
4	I/O Input/Output	4	*
5	Output interrupt	5	*
6	*	6	*
7	*	7	*
8	*	8	*
9	*	9	*
10	*	10	*
11	*	11	*
12	*	12	*
13	Transfer CWA	13	*
14	*	14	*
15	*	15	*

* Not used.

Notes:

- (1) Link tests BUSY if the PEC BTC has been initialized or if the PDP-4 is enabled. The PDP-9 cannot be tested for busy.
- (2) Interrupts are designated by their engineering labels. Two other interrupts, Input and End of Record, are available but not used.
- (3) An On-Off Line switch on the 4/9 Link can be used to turn off the incoming interrupts to the PEC. The normal mode is ON-LINE.

Programming Cautions:

The link will always accept a CEU instruction. The second CEU will override a transfer that has been started but not completed by the first CEU.

Interrupts:

Output. This interrupt is generated by each end of the B/4/9 Link to request attention by the other computer. It can be triggered independently of all other CEU functions. The PDP-4 and PDP-9 cannot interrupt each other.

BTC Complete. This is an interrupt that signals to the program that the transfer of a block of data has been completed. This is the hardware End of Block signal, 7ENDOB, at the PEC. This type of interrupt is not generated in the PDP-4. It is called overflow (OVFLO) in the PDP-9.

SEL/PDP-9 Link Interface

IOT Assignments for the PDP-9

<u>Mnemonic</u>	<u>Instruction</u>	<u>Function</u>
LBSF	705661	Skip if the PDP-4 is not busy.
LNBL	705664	Enable the SEL/PDP-9 Link.
LDIS	705642	Disable SEL/PDP-9 Link.
LISF	705601	Skip if the SEL Input (to PDP-9) flag is set.
LICF	705604	Clear the SEL Input flag.
LIPG	705602	Generate the SEL Input priority (from PDP-9) interrupt.
LOSF	705621	Skip if the SEL Output (from PDP-9) flag is set.
LOCF	705624	Clear the SEL Output flag.
LOPG	705622	Generate the SEL Output priority (to PDP-9) interrupt.
LESF	705641	Skip if the SEL End of Record flag is set.
LECF	705644	Clear the SEL End of Record flag.
LFRG	705662	Generate the PDP-9 End of Record interrupt.
LBES	705701	Skip if the SEL input buffer is empty.
LDHG	705704	PDP-9 Accumulator output to SEL. (Generate PDP-9 Data Here.)
LBFS	705721	Skip if the SEL output buffer is full.
LDAG	705712	Clear PDP-9 Accumulator and take input from SEL. (Generate PDP-9 Data Accepted.)
LSMR*	705722	Set data channel mode for Read (input).
LSMW*	705742	Set data channel mode for Write (output).
LOFS	705741	Skip if the data channel has overflowed.
LDSF	705761	Skip if the data channel is busy.
LDCF	705762	Clear the data channel Busy and Overflow.
LSTG	705744	Generate System Tag 2 pulse (also known as SB2.)

* Also sets Channel Busy flip-flop.

Notes:

- (1) There is no BUSY test for the 810B. It is assumed that the 810B is available if the PDP-4 is not busy.
- (2) The link must be enabled in order to send or receive interrupts and data. The PDP-4 Busy signal will block the enable IOT from enabling the PDP-9 Interface.

Programming Cautions:

A test for BUSY should be used before and after the link is enabled to insure that the link is available and that the PDP-9 has control.

Interrupts:

Input. This interrupt is not received or generated at the 810B Interface when the monitor package 7LNK is being used.

Output. This interrupt is used in both directions by the monitor package 7LNK.

End of Record. This interrupt is not used by the SEL monitor package 7LNK. It is automatically generated in the 810B Interface but has been disconnected at the PDP-9.

810B/PDP-4 Link Interface

IOT Assignments for the PDP-4

<u>Mnemonic</u>	<u>Instruction</u>	<u>Function</u>
LISF	705001	Skip if SEL Input (to PDP-4) flag is set.
LICF	705002	Clear SEL Input flag.
LIPG	705004	Generate SEL Input priority interrupt.
LOSF	705101	Skip if SEL Output (from PDP-4) flag is set.
LOCF	705102	Clear SEL Output flag.
LOPG	705104	Generate SEL Output priority interrupt.
LESF	705201	Skip if SEL End of Record flag is set.
LECF	705202	Clear SEL End of Record flag.
LDIS	705204	Disable 810B/PDP-4 Link.
LBES	705301	Skip if SEL buffer is empty.
LDHG	705302	Generate PDP-4 Data Here (data is in Accumulator).
LNBL	705304	Enable 810B/PDP-4 Link.
LBFS	705401	Skip if SEL buffer is full.
LLAC	705412	Clear Accumulator and gate data to Accumulator.
LDAG	705404	Generate PDP-4 Data Accepted.
LBSF	705501	Skip if the link Busy flag is set.
LERG	705502	Generate PDP-4 End of Record.
	705504	

Notes:

(1) The 810B tests BUSY if its BTC has been connected. If the PDP-9 is using the link, an enable IOT (LNBL) will not enable the link. There is no skip test for Enable.

(2) The link must be enabled in order to send or receive interrupts and data.

Programming Cautions:

A test for BUSY should be used before the link is enabled; however, it is possible for the PDP-9 to capture the link for use in the time between the instructions. Therefore, a BUSY test after the enable instruction should insure that the link is not in use by the PDP-9.

Interrupts:

Input. This interrupt is not received or generated at the SEL 810B Interface when the SEL monitor package 7LNK is being used.

Output. This interrupt is used in both directions by the SEL monitor package 7LNK.

End of Record. This interrupt is not used by the SEL monitor package 7LNK. It is automatically generated in the 810B Interface but has been disconnected at the PDP-4.

Cathode-Ray Tube Display
Unit '26

<u>Bit</u>	<u>CEU Second Word</u>	<u>Bit</u>	<u>Data Word</u>
0	BTC initialize	0	1/0 X/Y Address
1	Enable Light Pen	1	Intensity 1 2
2	Clear X Address	2	Blank 0 0
			Low 0 1
			Med. 1 0
			High 1 1
3	Clear Y Address	3	*
4	*	4	*
5	*	5	*
6	Increment X by 8	6	MSB
7	Increment X by 4	7	} 10 bit binary address (0 - 1023)
8	Increment X by 2	8	
9	Increment X by 1	9	
10	*	10	
11	*	11	
12	*	12	
13	Transfer CWA	13	
14	*	14	
15	*	15	LSB

* Not used.

Notes:

- (1) There are no TEU instructions on the CRTD.
- (2) Light pen interrupt coordinates are read X then Y with either AIP or MIP instructions.
- (3) Increment mode (Bits 6, 7, 8, or 9 on) causes a Y-data word to step the X axis by the increment selected.

Programming Cautions:

- (1) If increment mode is selected (Bits 6, 7, 8, or 9 on), then an X-position data word will set the display to the X-value with the three least significant bits equal to zero.

(2) Do not select more than one increment in a CEU. The results are not always consistent.

(3) A light pen interrupt stops BTC transfers until the X-Y coordinates are read by AIP or MIP instructions.

Interrupts:

Light Pen. An interrupt is generated when a point is picked with the light pen enabled. The X-Y coordinate of the point is then available for use in a program.

6CRT Light Pen Function Points

A	C	E	G	I	K	M
.	.	.	.	.	.	.
B	D	F	H	J	L	N
.	.	.	.	.	.	.

A = Start forward scan.

B = Stop scan and reset function points I and J.

C = Increase the X-increment.

D = Decrease the X-increment.

E = Increase the Y-increment.

F = Decrease the Y-increment.

G = Semi-logarithmic display.

H = Linear display.

I = Type the base channel number (B), the channel number (C), the channel contents (V), and the neutron energy of the following channels picked with the light pen.

J = Type the base channel number (B), the channel number (C), the channel contents (V), and the gamma energy of the following channels picked with the light pen.

K = Increase the Y-increment on the upper display.

L = Decrease the Y-increment on the upper display.

M = Start the backward scan.

N = Reset all function points.

6CRT Teletype Commands

<u>Command</u>	<u>Function</u>
xxx	Set the starting channel of the display to xxx.
Axxx	Add xxx to the starting channel of the display.
Bxxx	Set the base channel to xxx.
Cxxx YYY	Set time zero to xxx nanoseconds and the flight path distance to YYY millimeters.
	$E_{EV} = [72.297 * YYY] / (TOF - xxx)]^2$

Dxxx	Initiate the dual (upper) display with a displacement of xxx between starting channels.
Exxx	Type the base channel number (B), the channel number (C), the contents of the channel (V), and the neutron energy.
F	Type the ten channel numbers and their contents that have the highest counts.
Gxxx	Type the base channel number (B), the channel number (C), the contents of the channel (V), and the gamma ray energy (KV/channel).
Hxxx YYY	Type the sum of channels xxx through xxx+YYY.
Ixxx YYY	Set electron volts per channel to YYY and electron volts to xxx. $GE_{keV} = \text{channel no.} * YYY + xxx$
J	Not used
K	Not used
Lxxx YYY	Line print channels xxx through xxx+YYY in multiples of 8.
Mxxx YYY	Type the running sum of channels xxx through xxx+YYY.
Nxxx YYY	Line print the running sum of channels xxx through xxx+YYY.
Ø	Not used
Pxxx YYY	Type channels xxx through XXX+YYY.
Q	Not used
R	Not used
Sxxx	Subtract xxx from the starting channel of the display.
T	Type the base channel number (B), the starting channel of the display (C), the contents of the channel (V), and the neutron energy.
$0 < xxx < 2^{30} \quad 0 < YYY < 2^{30}$	

Notes:

A rub-out will terminate the display and return control to the system. Typing a DO will terminate the dual display. If xxx is equal to the starting channel of the display, a period may be typed in place of the xxx and space. The dual (upper) display is for visual reference only.

Binary Synchronous Communications Interface
Unit '43

<u>Bit</u>	<u>CEU Second Word</u>	<u>Bit</u>	<u>TEU Second Word</u>
0	Initialize BTC	0	Reverse sense of test
1	1/0 Connect/Disconnect interrupt in bits 2-4	1	*
2	Transmit Not interrupt	2	Skip if link is not busy
3	Control interrupt	3	Skip if link is on-line
4	Error interrupt	4	*
5	*	5	*
6	*	6	*
7	*	7	*
8	*	8	Skip if no data overrun
9	*	9	Skip if no program error
10	00 - End BTC with ETB, 10 - end BTC with ITB	10	*
11	01 - End BTC with ETX, 11 - sets program error	11	Skip if no character parity error
12	End transmission (for use with AOP/MOP)	12	Skip if no block check error
13	Input BTC current word address	13	*
14	Set unit to transmit	14	Skip if no receive synchronization
15	Set unit to read	15	Skip if no transmit response timeout

* Not used.

Notes:

- (1) Two modes of transmission are possible: normal (American Standard Code for Information Interchange - ASCII) or transparent. The transparent mode allows the parity bit (level 8) to be used as data.
- (2) A checking polynomial, $X^{16} + X^{15} + X^2 + 1$, generates a 16-bit block check character for either mode of transmission.
- (3) Normal (ASCII) text uses an odd parity check for each character.
- (4) See performance specifications CSP-500-6 or CSP-500-13 for acceptable Line Control Sequences.

Programming Cautions:

Do not use ITB ending. The software at the PDP-15 prohibits its use, and the CRC control logic in the BSCI requires modification.

Interrupts:

Transmit Not. This interrupt is generated after transmission of the two CRC characters when the interface returns to the idle state (neither receive nor transmit).

Control. The Control interrupt is generated as a result of the following: (a) receiving any DLE XXX response; (b) receiving the ending characters ENQ,* NAK or EOT; (c) receiving the block end characters ITB, ETB, ETX or the corresponding DLE XXX sequence in transparent text mode if the block check characters (a 16-bit CRC) received agree with internally generated block check characters; and (d) after transmission of the two block check characters.

Error. The Error interrupt is generated as a result of the following six conditions: (a) Data Overrun, a receive error caused by not emptying the receive buffer within one character time (196 μ sec); (b) Program, a receive error caused by the receipt of DLE, SOH, EOT, or NAK within a block of normal text or a setup error caused by (1) attempting to send a block with bits 10 and 11 of the CEU second word set or (2) executing a CEU with bits 14 and 15 set; (c) Parity, a receive error caused by an even number of ones in a character when in normal text mode; (d) Block Check, a receive error resulting from not satisfying the condition for Control interrupt; (e) Receive Synchronization Timeout, a receive error caused by not receiving within 2 sec from the last occurrence the synchronization character SYN(DLE SYN) in normal (transparent) text mode; (f) Transmit Response Timeout, an error condition that results from not obtaining line synchronization within 3.25 sec from the end of a transmission.

* The three-character abbreviations in this section are mnemonics for characters in USASCII.²¹

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