MASTER

AUTOMATED ARRAY ASSEMBLY

Quarterly Report No. 4

R. V. D'Aiello

May 1977

Work Performed Under Contract No. NAS-7-100-954352

**RCA Laboratories
Princeton, New Jersey**

ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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**Prepared Under Contract No. 954352 For
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103**

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PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from February 3, 1977 to May 2, 1977 in the Process and Applied Materials Research Laboratory, P. Rappaport, Director; Materials Research Laboratory, J. J. Tietjen, Director; Materials and Process Laboratory, Solid State Division, H. Veloric, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, P. Wright, Director. The Program Director is B. F. Williams. The Project Scientist is R. D'Aiello and the Project Supervisor is D. Richman, Head, Semiconductor Materials Research. Others who participated in the research and writing of this report are:

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SECTION I

SUMMARY

An experimental production facility has been established in the RCA Solid State Division (SSD) located at Somerville, NJ. This production line will be used to fabricate 3-in.-diameter silicon solar cells using the elements of the manufacturing sequences identified in our previous studies as most likely to achieve the JPL Low-Cost Silicon Solar Array Project (LSSA) cost goal of \$0.50/W. The major objective is to produce a sufficient number (>1000) of solar cells in such a manner as to test the sensitivity of the resultant distribution of cell characteristics to controlled variations in the process parameters.

A plan for introducing and selecting variables was established including three major junction-formation techniques: ion implantation, gaseous (POCl_3), and spin-on diffusion sources. The testing and development of screen-printed metallization with evaporated Ti/Ag contacts used as a control is a major part of the program.

During this quarter, organization of the facility was accomplished, including incoming wafer inspection, lot identification, and data logging; in addition, equipment assembly and check-out was completed. Twenty-two wafer lots (25 wafers/lot) were started with some lots devoted to initial calibration of equipment.

A plan for modeling and analyzing solar cell performance is presented which is based on measured dark I-V characteristics and a computed value of light-generated current. A statistical approach is outlined for relating measured electrical performance with the manufacturing sequences.

Panel design procedures are outlined in some detail starting with the problem of cell selection from an assumed Gaussian distribution of cell parameters. Further considerations of cell size in relation to packing factor and geometric, structural, and land usage factors are given.

SECTION II

INTRODUCTION

In our previous work, we have identified potential manufacturing sequences for solar cell array modules which satisfy the ERDA/JPL LSSA goal of \$0.50/W selling price. It was shown that in a highly automated line, a cost of \$0.30/W can be achieved, assuming the use of 3-in.-diameter wafers at zero cost for the silicon. The attainment of these cost goals relies heavily upon such processes as screen-printed metallization, spin-on or spray-on antireflection (AR) coatings, ion implantation, and a double-glass construction of panels. The costs predicted are very sensitive to the yield achievable using these processes and to the efficiency of the cells produced.

It is the purpose of this work to simulate the major elements of these manufacturing sequences in a small pilot production facility so that we can assess the product output and quality sensitivity to a set of variables most likely to affect the solar cell efficiency and electrical parameters.

The spectrum of process variables is shown schematically in Fig. 1, where the details for the case of ion implantation are given. It can be seen that the number of experimental runs can grow very rapidly, so that in the time allotted to this study, all combinations of variables can not be examined. However, judicious sampling of some variables and detailed study of others should allow an identification of the primary variables and how they impact both cost and performance.

For the case of ion implantation, a major emphasis is placed on controlled variation of the implant parameters, dopant type, energy, and dose since these can be reproducibly controlled and are expected to affect cost and performance.

The implantation will be done through a mask which delineates a planar junction at the periphery of the wafers. This process, which eliminates the need for a rim etch and junction cleanup, has been successfully tested on a small scale in our laboratory.

Variations will be made in the junction anneal and formation to test for the need of a capping oxide, and the effect of furnace temperature and time profiles on junction depth, sheet resistance, and junction quality will be measured.

Figure 1. Process variables.

Similar controlled process variations will be conducted using two other junction-formation techniques shown in Fig. 1. Some details for the POCl₃ gas diffusion and the spin-on source cases are shown in Figs. 2 and 3.

Standard metallization consisting of evaporated Ti/Ag contacts will be made on a control set from each lot. The remaining wafers of a given lot will constitute an experimental sample set for screen-printed metallization. Some of these will be screen-printed with test patterns in order to measure those printing parameters pertinent to the screen-printing process. Further details of the screen-printing experiments are given in Section IV.

A commercially available liquid* AR coating will be applied by a spin-on process in the first phase of this work. At a later stage, spraying of this coating will be evaluated.

Electrical testing of the completed cells will consist of illuminated power I-V curves on all cells with a selected set sampled for detailed

*Emulsitone Co., Whippany, NJ.

Figure 2. POCl_3 diffusion.

Figure 3. Spin-on source.

analysis. This set will be selected from the center and extremes of the distribution and detailed measurements such as spectral response, junction I-V, and physical examination will be conducted to determine the reasons for such performance and to relate these results with the process sequences. Some feedback will be included in the testing and sampling so that the process variations can be changed in such a way as to maximize the information obtained.

The experimental data collected from these measurements will be treated by the methods described in the section on analysis (Section V). A fairly extensive mathematical model of the cell performance, including explicitly the

metallization losses, represented the expected relations between cell performance and the controlled process variables. Initial work is designed both to validate the model and to determine actual distributions and sensitivity of the electrical parameters resulting from process variations. Statistical methods will then be used to identify the most critical variables.

A separate effort is being conducted in panel assembly and the statistical data on cell efficiency and performance characteristics generated by the above analysis will be used for deciding on an optimal cell matching scheme. Ultimately, a selection of the cell output will be used in an assembled panel.

The details of the equipment and processes described above and some preliminary results are given in Section III.

SECTION III

BASE LINE FABRICATION FACILITY

A. INTRODUCTION

The pilot operation is located at the RCA Solid State Division in Somerville, NJ. It is equipped with the latest apparatus and instrumentation for the production of semiconductor devices and is capable of being controlled precisely to generate data reflecting the effect of statistical as well as deliberate variations in the processing parameters. Special attention has been paid to maintaining lot identity and location control of all product wafers.

The equipment is monitored regularly and process control measurements are made according to the best industry practices, often based on American Society for Testing Material (ASTM) procedures.

B. BASIC PROCESS AND EQUIPMENT

1. Material

Silicon wafers are p-type, (100), chemically-mechanically polished on the front side and manually sawed and etched on the backside 0.5 mm thick. At this stage only 5- to 10-ohm-cm wafers are being used. Lower resistivity material in the range 0.6 to 2.5 ohm-cm has been delivered and will be used as a basic variable in the next period.

2. Junction Formation

Three methods are under test: ion-implantation of phosphorus or arsenic, a spin-on source of the same elements, and gaseous diffusion from phosphorus oxychloride. In all cases the back contact is made through a high-concentration boron diffusion. A few tests have been made using a mixture of ion implantation and spin-on for the front and back diffusions.

a. *Ion Implantation.* - The Somerville Extrion 200-1000 implant machine uses a gaseous source of phosphine or arsine for the n-type implant and boron trichloride for the p-type implant. The machine is capable of delivering up to 3-mA beam current in the range of 5 to 200 keV.

The implanter can accommodate 26 3-in.-diameter wafers at a time. Junction implant times are on the order of 10 minutes depending on species and experimental requirements. Until recently the wafer holders supplied by Extrion cast some shadow onto the wafers. New holders have been designed which are also capable of masking the surface peripherally so that a planar structure results which does not require further etching to define the junction. These holders will be available by mid-May.

Typical doses are 1×10^{15} phosphorus and 1.5×10^{15} arsenic atoms per cm^2 . Boron will be implanted into the back of the wafers at a dose of $\sim 1 \times 10^{15}$ atoms per cm^2 and simultaneously driven-in in the junction anneal step.

b. *Spin-on Diffusion Source.* - A Headway EC 100 spinner is used to apply spin-on diffusion source, dispensed from a hypodermic syringe. A variety of proprietary solutions made by Emulsitone Co., Whippany, NJ., has been used to obtain phosphorus, arsenic, and boron films. Care is taken to ensure proper ventilation and safety precautions in handling the toxic solutions.

c. *Phosphorus Oxychloride Deposition and Diffusion.* - A Thermo SPARTAN furnace is used, fitted with flowmeters, bubbler, and exhaust. Deposition and diffusion occur simultaneously. A typical cycle is 10 minutes preheat in nitrogen to reach thermal equilibrium, 45 minutes at temperature with oxychloride flowing, 10 minutes in nitrogen-10% oxygen while the wafers are slowly withdrawn at about 50 mm per minute by a programmed puller. Temperatures between 800 and 950°C have been used, and these are detailed in Table 1.

d. *Diffusion and Oxidation.* - When needed the substrates are oxidized or the dopants are driven in Thermco Pacemaker furnaces, equipped with programmed insertion and withdrawal mechanisms.

e. *Cleaning, Etching, and Photolithography.* - These operations are performed in laminar flow stations using procedures which are standardized for semiconductor device fabrication. All reagents are "Electronic Grade"; the rinse water is deionized, filtered, and monitored to ensure that its resistivity is over 18 Mohm-cm.

Wafers are "Standard Cleaned" first in SC-1, a 1:1:5 mixture of ammonia, hydrogen peroxide, and water, then in hydrofluoric acid, and finally in SC-2 which is hydrochloric acid, hydrogen peroxide, and water again in a 1:1:5

TABLE 1. MANUFACTURING DATA

Lot No. 25	Wafer No.	Source N	Dose A cm ⁻²	Source P	Dose A cm ⁻²	N kV	p kV	Time Min*	Temp °C	X _j μm	Sheet ρ N Ω/□	Sheet ρ P Ω/□	Life-Time μs	Metal Thickness μm
001	1-10	Phos Imp	1 x 10 ¹⁵	Boron Imp	5 x 10 ¹⁴	5	50	15	950	.3		NM ⁺	1.5	
002	11-35	Phos Imp	1 x 10 ¹⁵	Boron Imp	5 x 10 ¹⁴	5	50	30	950	.4	145**	NM ⁺	1.5	
003	36-60	Phos Imp	1 x 10 ¹⁵	Boron Imp	5 x 10 ¹⁴	5	50	30	925	.20**	193**	NM ⁺		
004	61-85	Phos Imp	1 x 10 ¹⁵	Boron Imp	5 x 10 ¹⁴	5	50			.2				
005	86-110	Phos Imp	1 x 10 ¹⁵	Boron Imp	5 x 10 ¹⁴	5	50							
006	111-135	Phos Spin	-	Boron Spin	-	-	-	45	850	.27		NM ⁺	2-4	
007	137-161	Phos Spin	-	Boron Spin	-	-	-	45	850	.26	7**	NM ⁺	2-4	
008	162-186	Phos Spin	-	Boron Spin	-	-	-	45	850	.23		NM ⁺		
009	187-213	Phos Spin	-	Boron Spin	-	-	-	45	850	.2		NM ⁺		
010	214-238	Phos Spin	-	Boron Spin	-	-	-	45	850	.25				
011	239-263	-	-	Boron Imp	1 x 10 ¹⁶	-	150	180	950			25		
012	In Process													
013	289-313	-	-	Boron Imp	1 x 10 ¹⁵		150	180	950					
014	In Process													

*Indicates that complete lot statistics are taken.

**All diffusions in addition have 10 min warm-up and cool-down unless otherwise specified.

+NM means sheet ρ not below that of wafer.

mixture at 85 to 95°C for over 15 minutes. This cleaning technique is specially designed to remove films that inhibit wetting, and to remove the thin native oxide; finally, SC-2 removes virtually all metallic contaminants that may reduce the carrier lifetime in the finished device. For preimplant cleaning, an equally good alternative method has been used, based on a mixture of equal volumes of sulphuric acid and hydrogen peroxide at over 80°C (systems). A standard photolithographic technique is used, based on Shipley A21350J, to produce the fine-line metal patterns used in the experimental stage. Wafers are stored and transported in fluorocarbon carriers with dust-tight lids and transferred to quartz boats wherever required. Oxides and glasses such as the spin-on dopant source are removed by etching in hydrofluoric acid, followed by rinsing in de-ionized water and drying.

f. Junction Definition. - When a spin-on source or phosphorus oxychloride is used to produce the junction, and in the case of ion implants before the edge mask wafer holder is used, it is necessary to either lap, grind, or etch the junction on the wafer periphery to separate the heavily doped n- and p-type regions from each other. This can be done conveniently by either an edge contour grinder or by lapping the edge with a slurry of garnet in water and then cleaning.

3. Metallization

During the initial phase of this work, while the details of screen-printing metallization are being investigated, the metal pattern is either evaporated through a metal mask or photolithographically defined.

The pattern is shown in Fig. 4. The back contact metal is not patterned. The metal is evaporated in a Veeco 775 equipped with an Airco-Temescal electron gun and planetary mechanism that permits uniform evaporation of 21 wafers at a time. The usual metallization is 0.2 μm of titanium followed by 3 μm of silver, and it is monitored by an Airco-Temescal XMS-3 thickness gage. A fraction of cells will continue to be metallized in this fashion for control purposes.

4. Antireflection Coating.

Emulsion titania silica film is applied using a Headway spinner to obtain a layer of about 700 to 800 nm. This is baked at an average temperature of

Figure 4. Metallization pattern.

450°C in a Watkins-Johnson variable-speed belt furnace having 6-heat-zone controls, in air. The wafers pass through the hot zone, which peaks at 500°C, in 10 minutes. The metallization is sintered at the same time.

C. DOCUMENTATION

Incoming wafers are inspected and measured at the receiving station and the data entered into the record (Fig. 5) together with the ordering details, vendor, lot numbers, and receiving dates. When wafers are drawn from the inventory, they are marked with the solar cell lot number by diamond scribing in small figures near the reference flat, and an entry is made into the solar cell travelog (Fig. 6). A process lot number is assigned and subsequent measurements and observations are entered onto the travelog. A copy of the shipped cell travelog is then filed. Individual measurements on each wafer are recorded at the various checkpoints on a log sheet like those shown in Figs. 7 and 8. New experimental runs or changes in scheduling are recorded on the form shown in Fig. 9.

Solar Cells - Incoming Inspection																								
Vendor _____					Vendor Lot # _____										Rec. Rep. # _____									
SC Lot # _____					SC/Vendor Type _____										Item _____									
Quan. Recv'd _____					Sample Size _____										Inspector _____ Date _____									
Instructions:																								
Criteria	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Total Defects	Total Items Rej.
Cracks																								
Scratches																								
Chip outs																								
Dimples/Pimples																								

Figure 5. Incoming wafer inspection sheet.

D. MEASUREMENTS

1. Resistivity and Sheet Resistance

A collinear Fells probe head in conjunction with a Keithley "Type-A11" instrument is used for both measurements. Bulk resistivity is measured with tungsten carbide, 40- μ m radius probe tips, loaded with 50 g, while the sheet resistance of the very thin junction layers is measured with "blunt" probe tips having 100- μ m radius, loaded with 40 g. The procedures outlined in ASTM F-84-73 and FF 374-74 are followed. Uniformity is checked by reading the sheet resistance in five places on each selected wafer.

2. Junction Depth

To obtain a junction depth measurement a Philtec Instrument Co. 2015 D groover is used, followed by staining the p-n-junction with the silver stain described in ASTM F 110-72, reagent 6.6. Since this is a destructive measurement, only one wafer per lot of 25 is checked for junction depth routinely. However, some batches are sampled in more detail to obtain statistical data.

Solar Cell Travelog

SC Lot No.		Quan.	Process Lot No.			
Process Description	Material	Operator	Date	Gross	Net	Special Instructions
Incoming Inspection						
Serialization						
SCC = 1 Bulk P Meas						
Clean	Code Z					
Dope						
	Spin-On					
	Q&S					
Clean						
Drive	T (°C)					Push t (min)
	N ₂ (CFH)					Zone t (min)
	O ₂ (CFH)					Pull t (min)
SCC = 2	Sheet ρ					
	Junc. Depth					
Clean						
Metal	E Gun					
	Screen On					
	Filament					
Clean						
AR Coating						
Electrical Test						
Ship						

Figure 6. Solar cell travelog.

3. Wafer Thickness

Thickness is measured on each incoming wafer in five places with a Bausch and Lomb Microline DR Optical Gage 25 B. The instrument is calibrated periodically against National Bureau of Standards thickness gages.

Solar Cells									
Bulk Resistivity Measurements									
SC Lot =		Date		Oper.		Process Lot =			
		Thickness	Factor	V_{FWD}	V_{RCU}	Factor	Bulk P		
	SN	(mil)	0.00254	(mV)	(mV)	4.53	(ohm-cm)		

Figure 7. Solar cell bulk resistivity measurement chart.

Solar Cells			
Sheet Resistivity Measurements			
Lot No.	Oper.	Date	Sheet of

Figure 8. Solar cell sheet resistivity measurement chart.

Date _____

Furnace Number	Temperature Requested	Requested by	Profile Check	Furnace Release	Comments

Figure 9. Chart for recording changes.

4. Antireflection Coating and Metallization Thickness

After baking the antireflection coating, a wafer is coated with an etch mask such as wax or etch-resistant tape in a way that permits a straight edge to be defined. This is done by etching in hydrofluoric acid; then the mask is removed. The step height or metal thickness is determined by a surface profilometer such as a Talysurf made by Engis Equipment Corp. A set of wafers with a known AR coating thickness has been collected and is used for visual comparison, as routine process control.

5. Electrical Measurements

All completed cells are electrically characterized by a simulated AM-1 illuminated I-V and power output measurement. This measurement is accomplished using an ELH photoflood lamp and dynamic electronic load. The calibration and measurement procedure will follow that specified by NASA-Lewis in their publication NASA TM X-71771.

A set of cells from the extremes of the performance distribution will be selected for detailed diagnostic measurements. These measurements will include spectral response, junction I-V characterization, lifetime (diffusion length), and, where appropriate, detailed impurity profiling (SIMS) and physical-chemical surface examination.

6. Furnace Temperature Profile

All furnaces are monitored weekly, and the data are recorded together with information on any adjustments. The absolute calibration is maintained by the in-house standards department, which carries out periodic checks on all instruments and refers these to National Bureau of Standards traceable standards.

E. SUMMARY OF PILOT LINE PRODUCTION RUNS FOR THE FIRST QUARTER

Twenty-two lots of wafers, 506 in all, were started. Of these, 10 lots were completed through junction formation.

The first objective was to test the operation of the line after staffing it with personnel drawn from the Power Device Engineering Model Shop at Somerville. This was found to be effective, and the next objectives were concerned with testing ion implantation and spin-on sources in conjunction with the diffusion temperature, aiming at 0.3- μ m junction depth and the sheet resistance requirements for 100 to 150 ohm/square for the n-type and less than 30 ohm/square for the back contact p-type diffusions.

The variations in processing are summarized in Table 1.

F. DATA EVALUATION

Data taken in the course of manufacture are recorded on the travelog. While starting the line an excess of data is being taken in order to find variations that are significant. Table 2 shows the result of applying normal statistics to the recorded data. Figures 10 and 11 are graphic representations of some of the statistical data. It is clear that ion implantation produces a much narrower distribution in sheet ρ than the spin-on source. How this affects the final efficiency has not yet been determined. Sheet ρ measurements on the p side revealed that the boron implant at a dose of 5×10^{14} atoms per cm^2 produced a sheet ρ higher than the wafer itself and could not be accurately measured with the four-point probe.

A higher boron dose ($\sim 1 \times 10^{15}$) will be used on future lots.

TABLE 2. RESULTS FROM APPLYING NORMAL STATISTICS TO RECORDED DATA

Parameter	n	$\bar{X}$	S^2	S	$\bar{X} + 3S$	$\bar{X} - 3S$	$\max_i - \bar{X}$	$\bar{X} - \min X_i$	$\max X_i$	$\min X_i$	Range
002 sheet ρ n	120	147	31	5.5	163	130	19	10	166	137	29
003 sheet ρ n	220	163	57	7.5	186	141	23	15	187	148	49
003 x_j	0.24	0.193	0.0024	0.0492	0.34	0.045	0.062	0.102	0.35	0.091	0.165
007 sheet ρ n	248	71	356	19	137	14.4	61	28	132	43	89
008 sheet ρ n	220	59	105	10.2	39	28	45	16	104	42	62
013 sheet ρ p	220	31	35	5.9	49	14	20	8.7	51	23	28

Definition of columns: n = number of readings

$\bar{X}$ = mean value of data set

S^2 = standard deviation squared

S = standard deviation

$\left. \begin{array}{l} \bar{X} + 3S \\ \bar{X} - 3S \end{array} \right\}$ upper and lower 3 σ limit

$\left. \begin{array}{l} \max_i - \bar{X} \\ \bar{X} - \min X_i \end{array} \right\}$ maximum deviation from mean

$\max X_i$ = maximum value of X

$\min X_i$ = minimum value of X

Figure 10. Statistical data, phosphorus spin-on source.

Figure 11. Statistical data, ion implantation.

SECTION IV

SCREENED-PRINTED METALLIZATION

A. CHEMICAL ANALYSIS OF THICK-FILM METALLIZATION INKS

Two additional Engelhard inks were obtained and analyzed by emission spectroscopy. The types and concentrations of cation constituents for the newer Ag (A-3441) and Al (A-3484) inks are listed in Table 3, along with those for the earlier Ag (A-3233) and Al (A-3113) inks. There is evidence of a reduction of B concentration in the new Ag ink with the addition of P, presumably due to enhance doping on n-type Si surfaces. The new Al (A-3484) has less Pb, and B has been completely removed. Since Al can serve as its own dopant, the addition of other group III elements was apparently deemed unnecessary. Testing with these inks has begun as described below.

B. SPECIFIC CONTACT RESISTANCE TEST RESULTS

The previously described dot-to-dot test pattern was screen-printed onto various uniformly doped n- and p-type silicon wafers, as well as onto p-type Si in which n-type junctions had been prepared by ion implantation of phosphorus. The latter n⁺-p junctions were thermally diffused to produce a junction depth of about 0.2 μm .

The uniformly doped wafers were fired at temperatures ranging from 550 to 700°C for the times specified in Table 4. The contact resistance was found to vary mostly with carrier concentration, as expected. In Table 4, for example, the Ag ink (A-3441), when fired on n-type (P) Si with a carrier concentration of $5 \times 10^{19}/\text{cc}$, yielded specific contact resistivities ranging from 1.8 to 0.1 ohm-cm^2 . The latter value was obtained when the Ag metallization was fired at 700°C for 10 minutes. However, when fired on n-type (Sb) Si with a carrier concentration of $5 \times 10^{18}/\text{cc}$, the specific contact resistance was not less than 2.3 ohm-cm^2 . As the carrier concentration was further reduced, e.g., to $8 \times 10^{15}/\text{cc}$, contact resistance rose abruptly to the kohm level.

Test results with Al ink (A-3484) were similar. Despite the fact that Al, a group III dopant, was applied to a group V-doped ($5 \times 10^{18}/\text{cc}$, Sb) wafer, specific contact resistance was 2.8 ohm-cm^2 when fired at 600°C for 10 minutes. When Al ink was sintered on wafers with lower carrier concentration of either dopant type, the specific contact resistance was in the kohm level.

TABLE 3. EMISSION SPECTROGRAPHIC ANALYSIS OF THICK-FILM INK CATION CONSTITUENTS
(ppm by weight)

Element	<u>Engelhard Formulations</u>			
	<u>Ag</u> <u>A-3233</u>	<u>Ag</u> <u>A-3441</u>	<u>Al</u> <u>A-3113</u>	<u>Al</u> <u>A-3484</u>
Cu	20-200	10-100	30-300	30-300
Al	100-1000	1000-10,000	S	S
Fe	10-100	10-100	150-1500	200-2000
Mg	1-10	50-500	30-300	50-500
Si	100-1000	600-6000	500-5000	300-3000
Pb	S	S	S	2-20
Ba	1-10	30-300	ND	ND
B	S	1000-10,000	S	ND
Sb	300-3000	100-1000	ND	ND
Bi	3-30	ND	ND	ND
Ti	3-30	30-300	10-100	30-300
Zn	300-3000	150-1500		10-100
Na	30-3000	30-300	30-300	30-300
Ni	ND	10-100	ND	10-100
Mn	ND	1-10	100-1000	150-1500
Ga	ND	ND	100-1000	150-1500
Ag	S	S	30-300	10-100
P	ND	600-6000	ND	ND
Au	ND	10-100	ND	3-30
Pd	ND	15-150	ND	6-60
Ca	ND	3-30	ND	ND
Cr	ND	ND	ND	10-100

S = element concentration is large and beyond range of emission spectroscopy
ND = not detected

TABLE 4. SPECIFIC CONTACT RESISTANCE ON UNIFORMLY DOPED SILICON

Engelhard Ag A-3441

A. <u>Si 5×10^{19}/cc n-type (phosphorus), (100)-plane</u>					
Firing Conditions		Least Square Fit		Coefficient of	Specific Contact
$^{\circ}\text{C}$	time (min)	$y = b + mx$		Determination	Resistance ($\Omega\text{-cm}^2$)
		$b(\Omega)$	$m(\Omega/\text{cm})$	r^2	
550	5	86	20	0.1	1.4
600	5	109	2	0.01	1.8
650	5	77	-15	0.38	1.3
700	5	9	5	0.18	0.2
500	10	105	1	0.002	1.7
600	10	80	17	0.77	1.3
650	10	7	6	0.21	0.1
700	10	7	2	0.46	0.1
B. <u>Si 8×10^{15}/cc, n-type (phosphorus), (100)-plane</u>					
550	5	open			
600	5	k Ω level			
650	5	k Ω level			
550	5	k Ω level			
+700	10				
C. <u>Si 0.2×10^{15}/cc, p-type (boron), (100)-plane</u>					
550	5	k Ω level			
600	5	579	172	0.88	9.2
650	5	590	214	0.77	9.6
550	5	597	234	0.96	9.7
+700	10				
D. <u>Si 5×10^{18}/cc n-type (antimony), (111)-plane</u>					
550	5	k Ω level		0.007	2.8
600	5	172	0.5	0.44	4.0
650	5	248	22	0.19	2.3
550	5	143	37		
+700	10				
E. <u>Si 8×10^{15}/cc, n-type (phosphorus), (100)-plane</u>					
550	5	open			
600	10	k Ω level			
F. <u>Si 0.2×10^{15}/cc, p-type (boron), (100)-plane</u>					
350	5	k Ω level			
600	10	k Ω level			
G. <u>Si 5×10^{18}/cc, n-type (antimony), (111)-plane</u>					
550	5	k Ω level			
600	10	170	19	0.91	2.8

Subsequently, Ag ink (A-3233) was printed and sintered at temperatures ranging from 550 to 850°C on ion-implanted (P) silicon with an approximate junction depth of 0.2 μm (sheet $\rho \approx 150$ ohm/square). As shown in Table 5, the specific contact resistance was quite varied, ranging from 10 to 1.7 ohm-cm². The latter value is associated with the 800°C sintering temperature. Higher dopant concentrations by ion implantation are now being sought to lower the required sintering temperature and specific contact resistance. In addition, tests on junctions formed by POCl₃ diffusion are in progress.

TABLE 5. SPECIFIC CONTACT RESISTANCE ON ION-IMPLANTED (P) SILICON

Engelhard Ag Ink (A-3233)					
Firing Conditions		Least Square Fit (Ω)		Coefficient of Determination	Specific Contact
Wafer No.	10 min @ Temp. ($^{\circ}\text{C}$)	$y = b + mx$		r^2	Resistance ($\Omega\text{-cm}^2$)
		$b(\Omega)$	$m(\Omega\text{-cm})$		
V60-50	550	306	72	0.81	5.0
"	600	625	42	0.40	10.1
"	650	545	34	0.24	8.8
"	700	287	48	0.13	4.7
60-51	700	329	117	0.47	5.3
"	750	-26	154	0.46	-0.8
"	800	103	28	0.47	1.7
"	850	423	13	0.28	6.9

C. SCREEN-PRINTING SOLAR CELL TEST PATTERNS

On five samples, each from the lot of ion-implanted (P) wafers (nos. V60-36) to V60-60), actual solar cell test patterns were printed with Ag inks, A-3233 and A3441. To simulate actual production conditions, the wafers were fired in a continuous belt kiln with a peak temperature of 800°C and a dwell time at the peak temperature of about 10 minutes. Both inks produced slightly irregular edge definition which was related to the choice of a 200 mesh screen. Changes in mesh (to 325), wire diameter, and screen emulsion thickness should help to alleviate this condition. Narrow, 0.127-mm (5-mil) line widths are especially sensitive to wire size differences, generally resulting in poorer line resolution. However, the remaining configurations in the test pattern printed well, including the dots, rectangles, and sheet resistance test bars.

D. METALLURGICAL ANALYSIS

The extent of penetration of the metals into the silicon substrates was determined by sectioning through screen-printed and fired metallization test patterns followed by microscopic examination and depth measurements. The sectioning was performed by angle lapping techniques to enlarge the field of observation by factors up to fifty-fold. Combined with the microscopic magnification, total enlargement factors up to 50,000-fold were available for examination. Furthermore, a variety of selected chemical etch compositions was applied to demarcate by staining any p-n junction that may have been found in the Si substrate underneath the metal patterns by doping from impurities, or from the metals themselves. Chemical staining was also useful to enhance the delineation of recrystallized or alloyed metal/Si regions, as well as localized structural defects.

Systematic analysis of the samples prepared with Ag and Al inks on homogeneously doped Si test wafers, as described in subsection 3, above, did not reveal any such junction formation within the detection limit of the analytical technique (a few tenths of a micrometer in depth). However, the samples with Al ink that were heated to 600°C for firing of the ink exhibited severe localized alloying. A photomicrograph of a typical n-type, (100)-plane Si sample is shown in Fig. 12. The shape of the dark rectangular areas indicates preferential reaction in (100)-plane crystallographic defects [on (111)-plane Si the alloy figures were triangular, typical of (111)-pits]. Some of these alloy spikes penetrated as much as 40 μm into the substrate Si. Electrical measurements indicated that these Si/Al alloy spikes were rectifying on n-type silicon substrates, and thus may not constitute an unacceptable contact on actual solar cells where the p-n junction is only 0.2 μm deep. The behavior of these samples is not unexpected, since the firing temperature was well above the Si/Al eutectic formation (577°C) and since no barrier layer (such as Ti) is used between the Si and the screened-on ink patterns.

The test samples prepared with Ag ink on n- and p-type Si test wafers were fired at temperatures up to 700°C. No evidence was found that would indicate junction formation, alloying, spiking, or other defect generation. A low-magnification photomicrograph of a typical sample is presented in Fig. 13.

Figure 12. Formation of Al/Si alloy patterns (dark areas) on n-type (100)-plane Si substrate test wafer 600°C-firing of a screened-on Al ink layer. The dark gray portion is part of a 5° angle-lapped region (shown here to a depth of 13 μm) which demonstrates the spiking of the alloyed areas. (150X)

Figure 13. Part of an angle-lapped screened-on Ag ink circular metallization pattern fired at 700°C on n-type (100)-plane Si substrate test wafer. The 5° angle section indicates a compact metallization layer (right center) of 12 μm thickness. No alloying or spiking is apparent. (150X)

Metallurgical and electrical measurements on actual solar cells having screen-printed Ag metallization patterns are now in progress. Cells with Ag ink A-3233 fired for 10 minutes at 850°C have shown evidence of Ag/Si localized penetration to a depth of about 3 μm , as seen in the photomicrograph in Fig. 14. This indicates that a temperature of 850°C for Ag may be excessive. Further tests at lower temperature are in progress.

Figure 14. Angle section (3°) through a screened-on A-3233 Ag ink metallization layer fired at 850°C (10 min). Localized spots of Ag/Si are visible to a depth of 3 μm . (385X)

It should be pointed out that some of the problems we have encountered with high contact resistance appear to be related to ion-implantation parameters that may cause a depletion of dopants on the Si surface, and on excessive accumulation just below the surface. Experiments are being designed to resolve these questions so that formation of good-quality contact at relatively low temperature becomes feasible. Metallization tests with conventionally fabricated cells (instead of ion-implanted cells) are also under way to obtain comparative data.

SECTION V

ANALYSIS

A. MATHEMATICAL MODEL OF CELL EFFICIENCY

The electrical properties of the cells are being analyzed by a procedure that is an extension of that used by R. J. Stirn [1]. The current-voltage curve is represented by a diode having two exponential terms, one with the quality factor $A = 1$ and the other with $A = 2$, and a phenomenological shunting resistance R_{sh} , leading to the general equation

$$I = I_{01}[\exp(\frac{eV}{kT}) - 1] + I_{02}[\exp(\frac{eV}{2kT}) - 1] + \frac{V}{R_{sh}} - I_L \quad (1)$$

where I_L is the light-generated short-circuit current. Values for I_{01} , I_{02} , and R_{sh} can be inferred from the observed behavior of the cells provided one uses the temperature dependences of the dark I-V characteristics. From these three values, one of the critical physical properties, the junction quality, can be deduced. By use of the characteristics of both small isolated diodes and full cells, it is also possible to distinguish between the inherent junction quality and the effects of localized defects that are known to degrade the properties of generally good junctions.

To obtain information on other cell variables, we model computationally the value of $I_L = I_{sc}$ (always on the basis of 1-cm^2 area). The subroutine that does this is the one used for modeling the quantum efficiency spectrum and total current collection as shown in Quarterly Report No. 3, p. 8, 9 [2]. There are seven physical variables of a cell that are used as parameters in this program: the front layer thickness, TF; front carrier diffusion length, LF; front surface recombination velocity, FSRV; the spectrum of the AR coating on the cell (identified simply by a code number); the back region ($\approx$ cell) thickness, TB; back carrier diffusion length, LB, and the back surface recombination velocity, BSRV. The wafer thicknesses currently being used are all sufficiently

1. R. H. Stirn, *Proc. IV Photovoltaic Specialists Conf.*, IEEE, New York, 1972, p. 72.
2. B. F. Williams, *Automated Array Assembly*, Quarterly Report No. 3, ERDA/JPL-954352-76/3, prepared under Contract No. 954352 for Jet Propulsion Laboratory, September 1976.

greater than the attainable values of LB that the devices are effectively insensitive to BSRV; this also obviates the need for considering any effect of the back surface on the value of I_{01} or I_{02} .

This procedure computes the maximum power point of Eq. (1) and next analyzes the effect of power losses associated with front contact by means of another subroutine that is in essence the same as that described in ref. [2], p. 10, 11. The constants of this program are the cell size, the thicknesses, and widths of the fine grid and bus bar metals, the fine grid line spacing, and the maximum power values I_m and V_m calculated previously. The physical variables of concern in this part of the computation are the Si sheet resistivity, ρ_g , the metal-Si contact resistivity, ρ_c , and the metal bulk resistivity, ρ_b . The values of ρ_g and particularly ρ_c are sensitive to the detailed nature of the metallization process.

After allowing for the contact losses, the calculated cell performance is matched to the measurements and diagnostic techniques used to identify problem areas in the processing. We expect this more comprehensive analysis to provide more information than has previously been available.

B. SIMULATION STUDY

After the cell efficiency mathematical model has been validated,* a simulation study can be performed to investigate the "quality" of the array module manufacturing sequences under consideration. The initial analysis will assume that the cell efficiency model independent variables are statistically independent and that each variable can be associated with one step in the manufacturing sequence or with the starting wafer. (If necessary, statistical dependence between disjointed pairs of selected variables can be added at a later time.) For each independent variable, a frequency distribution must be constructed from experimental results. Two methods will be used in the initial implementation to represent distributions. For normally distributed variables,

*Some modifications to the basic model formulation may be needed to reflect detrimental interaction between variables. Metal penetration through the junction is of particular concern.

the mean $\bar{X}$ and standard deviation S must be estimated. For other variables, uncertainty assessments will be expressed as an interval (a,b) , which defines the range of the variable, and an uncertainty profile n , which represents the shape of the frequency distribution of the variable. These profiles will be defined on the normalized range $(0,1)$ so that unique profiles for every variable will be unnecessary. Figure 15 shows some examples of possible uncertainty profiles.

Figure 15. Uncertainty profiles.

The analysis for a particular manufacturing sequence proceeds by using a random number generator and the appropriate frequency distribution information to generate a sample value for each of the process random variables. A cell efficiency estimate is then computed using the cell efficiency model. This procedure is repeated a specified number of times, N , in order to generate a frequency distribution for cell efficiency.

A criterion is needed to compare cell efficiency distributions of alternative manufacturing sequences. (Statistical techniques must first be used to show that the distributions are not equal.) The initial approach will be to specify a minimum acceptable cell efficiency allowable and to use the distribution to estimate the yield of the test step of the manufacturing sequence. (Adjustments for breakage and other losses must also be made.) Since lower efficiency cells are assumed rejected at the test step (100% reliable test

assumed), the *average* efficiency of cells in the array module will be increased. This average cell efficiency must be estimated using the cell efficiency distribution.

The estimates of test reject rates and final cell efficiency can then be used to update the preliminary estimates used in the cost model [3] and the model used to provide \$/W manufacturing cost estimates for each of the manufacturing sequences under consideration.*

The impact of improvements in the control of process variables can be investigated by modifying the frequency distributions of model variables affected and incorporating any necessary cost factors in the cost model data base. The above procedure can then be repeated to determine whether the proposed changes are cost effective. The accuracy of the cell efficiency model will determine the viability of this analytical approach.

3. B. F. Williams, *Automated Array Assembly*, Annual Report, ERDA/JPL-954352-77/1, prepared under Contract No. 954352 for Jet Propulsion Laboratory, May 1977, pp 78-83.

*The starting wafer cost must be considered when comparing alternatives.

SECTION VI

PANEL DESIGN

A. CELL MATCHING ANALYSIS

This analysis is being conducted to determine whether any cell measuring and sorting strategy can increase assembled panel generation capability compared with random cell selection for the panel. It is expected that 100% acceptance testing of cells will be required to avoid the possible use of inactive cells. This effort is directed to the issue of whether there should be sorting of good cells into performance categories.

It is still not possible to characterize the product distribution of a low-cost solar cell production line. This study is based on certain simplifying assumptions concerning cell property variability produced by such a line. Therefore, the results of this study should not be regarded as definitive. The computer models and techniques used in this study can be used for more exacting studies as product variability becomes better defined.

1. Assumptions

It is assumed that the only cell test to be performed will be a measurement of a test current (I_{test}) at AM-1 flux and at a preselected test voltage (V_{test}). The selected test voltage is in the middle of the range of voltages where P_{max} will occur; typically this is 460 mV. Since the AM-1 flux is known, then this test actually measures efficiency (η_{test}) at V_{test} .

In order to compute the panel output power with various cell combinations, a closed form function describing the cell I-V characteristic is required. Basically, there is a choice between two different expressions. The simplest function uses one exponential term to represent junction current leakage while the more complicated function uses two exponential terms. The one-term function requires knowledge of short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), and one point near the P_{max} point, i.e., (I_{test}) at (V_{test}) to solve for the constants (A, I_0) that will pass the characteristic equation through all three points. In contrast, the two-term I-V characteristic

requires one additional point (I , V) to find three constants (A , I_{o1} , I_{o2}) that will pass the characteristic curve through all four points. In order to use the one-term characteristic, the following assumptions have been made.

- (1) All usable cells have the same open-circuit voltage, V_{oc} .
- (2) The ratio of short-circuit current I_{sc} to test current (I_{test}) is the same for all cells at a value of I_{ratio} .

Some assumptions must also be made about the distribution of cells produced. The most logical assumption is that the measured test efficiencies η_{test} fit a normal (Gaussian) probability distribution; that is, that the probability of a cell having a given efficiency fits the curve in Fig. 16.

Figure 16. Gaussian probability distribution of test efficiency of cells.

The requirement of this curve is that the integral under a normalized curve over all values of X is equal to 1. This simply states that all cells measured have a measurable test efficiency. It is assumed that all cells between $\pm 3 \sigma$ (standard deviations) will be accepted for panel fabrication, which would consume 99.8% of all cell production. The final results will show that even if this "window" were narrowed, the conclusions would be unaffected.

It is assumed that all test efficiencies falling in arbitrarily defined ranges of test efficiencies will be separated into different bins. Thus any cell falling within the efficiency range defined by region I in Fig. 16 would be put in box I and so forth. For the purpose of this analysis, it is assumed that all cells in box I can be represented by the efficiency at the middle of the range I and so forth. For the purpose of this analysis, it is assumed deviations defining the various ranges have been picked, the analytical relationship of the Gaussian distribution can be used to find the cell populations of each box.

2. Analytical Model

The basic analytical relationship used in this circuit model is the well-known single exponential relationship between cell voltage and current. The key circuit relationships data processing steps used will be described in the logical sequence used in the model. For the particular case analyzed, the test efficiency points were:

$$\begin{aligned}\eta_{\max} &= 18\% & +3 \sigma \\ \eta_{\text{avg}} &= 15\% & \text{mean} \\ \eta_{\min} &= 12\% & -3 \sigma\end{aligned}$$

Five sort regions were chosen with the average efficiency in each bin being:

$$\begin{aligned}\eta[1] &= 12.62\% \\ \eta[2] &= 13.87\% \\ \eta[3] &= 15.0\% \\ \eta[4] &= 16.12\% \\ \eta[5] &= 17.38\%\end{aligned}$$

$$V_{\text{oc}} = 0.545 \text{ open-circuit voltage}$$

$$I_{\text{ratio}} = 0.75 \text{ ratio of short-circuit to test current.}$$

The value of I_{ratio} used is representative of terrestrial cells in use today. Further investigations can accommodate value in the range of 0.55 to 0.85, probably due to variations in series resistance.

$$AM-1 = 0.103 \text{ W/cm}^2 \text{ (AM-1 flux)} \quad (2)$$

The characteristic I-V expression referred to earlier is

$$I_L = I_{sc} - I_0 (e^{\lambda/AV_L} - 1) = I_L (V_L) \quad (3)$$

where $\lambda = e/kT = 38.647$, a known constant. For reference, the I-V characteristics for the five regions are shown in Fig. 17. By placing the points (I_{test}, V_{test}) , $(0, V_{oc})$ along with $I_{sc} = I_{test}/I_{ratio}$ in Eq. (3), two simultaneous equations are generated that define the A and I_0 for the particular cell's characteristic curve.

Figure 17. I-V characteristics of five sort regions.

A and I_0 are found by a Newton-Rapheson technique. In this manner, the constants for all cell bins are found $A[J]$, $I_0[J]$ for $J = 1$ to 5.

The fraction of production (Frac) that falls in equal regions found by numerical fit to the Gaussian distribution is:

$$\text{Frac}[1] = 0.047$$

$$\text{Frac}[2] = 0.264$$

$$\text{Frac}[3] = 0.378$$

$$\text{Frac}[4] = 0.264$$

$$\text{Frac}[5] = 0.047$$

The calculation which must be made is to compare the maximum performance of a circuit with the distribution of cells shown above, all operating at maximum efficiency with the same circuit operating at the design terminal voltage and each cell at the same current.

a. *Operation at Maximum Circuit Efficiency.* - The power produced by a P_L is given by

$$P_L = V_L I_L (V_L) \quad (4)$$

where $I_L (V_L)$ is given by Eq. (3). To find the maximum power, the derivative $\frac{d(P_L)}{d(V_L)}$ of Eq. (4) can be found readily in closed form. Then by using the Newton-Rapheson method, the value of voltage $V_{pmax}[J]$ in Eq. (4), the value of $P_{max}[J]$ per cm^2 of cell for all regions can be found. Each of the values of power must be multiplied by the appropriate area $\text{Frac}[J]$ to get the actual power. Therefore, the maximum total produced is given by

$$P_{mi} = \sum_{J=1}^{J=5} \text{Frac}[J] P_{max}[J] \quad (5)$$

In other words, P_{mi} is the maximum power that could be produced if the cells were sorted and assembled into five different panel types.

b. *String Operation.* - When power is produced by a string of cells, they must all have the same current density. However, the power to the panel is contributed in proportion to the areas $\text{Frac}[J]$. Thus, the expression for the string power as a function of current I_L , is given by

$$P_{\text{string}}(I_L) = \sum \text{Frac}[J] P_L(I_L) \quad (6)$$

Here the power as a function of current I_L is needed which can be found by solving Eq. (3) for $V_L(I_L)$, and, therefore, $P_L(I_L) = I_L * V_L(I_L)$. Here again the derivative of string power with respect to current $d(P_{\text{string}})/d(I_L)$ can be found in closed form. Then the value of I_L for maximum string power is found, I_{pms} . In this manner, the maximum string power found is

$$P_{\text{ms}} = V_{\text{string}}(I_{\text{pms}}) \quad (7)$$

Thus, the value of P_{ms} corresponds to the panel power produced if the panel were composed of the appropriate fractions of production $\text{Frac}[J]$ for the normal distribution. That is, P_{ms} represents the typical panel with no sorting.

c. *Results.* - The result of all these calculations is that

$$P_{\text{mi}} = 16.4 \text{ mW/cm}^2 - \text{independent optimized operation}$$

$$P_{\text{ms}} = 15.9 \text{ mW/cm}^2 - \text{string optimized operation}$$

Thus there is only a 2.95% gain in the power produced due to the sorting and selective assembly postulated in this analysis. For 100% test of wafers in an automated facility, we have shown [3] that the test cost is \$0.012/W. If the installed power supply costs \$1/W, this ~3% increase in output power saves 1.8¢/W, and, therefore, the implementation of this procedure is cost-effective. It is recognized that many assumptions had to be made to conduct this analysis. It is possible that other distributions of cells or a distribution of different cell characteristics could change the conclusions somewhat. It will probably not be worthwhile to pursue this issue further until the low-cost parameters are more completely characterized.

B. OPTICAL COUPLING TO THE CELLS

Three panel alternatives are being examined in terms of optical coupling. They are

- (1) Cell bonded to the front window
- (2) Cell bonded only to the substrate with air gap between cell and window.
- (3) Same as (2) except window has AR coatings.

Figure 18 shows these alternatives. The solar transmission to the cells in each of the three cases is 0.899, 0.828, and 0.886. The message from these calculations is that a 7.9% loss of power output occurs when the design is changed from front mount to back mount. A substantial fraction of this can be recovered if the cover glass is coated with an antireflection surface. The comparison may be somewhat questionable since the AR coating used is produced by an etch technique which selectively leaches material out of the glass surface. The porous layer created has an effective index less than solid glass. This porous layer, however, is susceptible to body oils and other environmental impurities which tend to destroy the antireflection character of the surface. We are now in the process of experimentally assessing the relative technical merit of these alternatives.

Figure 18. Optical coupling alternatives.

C. PANEL CONSIDERATIONS

1. Circuit design

The concept of the 4-ft-square panel has been previously described as a desirable size for a silicon solar array module. A panel voltage of 15.0 Vdc is an attractive basic voltage since it is suitable as a 12-Vdc battery charger and can be built up in modular fashion to most required voltage and power levels. Finally, a strong case can be made for location of circuit terminals on the diagonal of the panel. Given these considerations, it is possible to describe a limited number of cell and panel configurations which satisfy the three constraints. These sizes and configurations are summarized in Table 6. The bases of the designs shown are:

- A 1-in. border is left around the panel border (packing factor is calculated on the basis of the available 46 in. x 46 in. cell mounting area).
- Cells spaced 0.020 in. apart.
- Base line cell orientation is on a hexagonal system of axes. In some instances, it is necessary to adjust the angular orientation of the axes slightly to accommodate an integral number of cells. This adjustment is indicated by the angle shown in parenthesis under array configuration.
- Straightforward parallel connection of the circuit strings must be possible.

TABLE 6. PANEL SIZE AND CONFIGURATION SUMMARY

No. of Parallel Circuits	Cell Diam (in.)	Array Con- figuration	Nominal Panel Voltage (V)	Packing Factor (%)
1	8.48	5 x 6 (60°)	13.8	80.0
2	5.68	6 x 10 (51°)	13.8	71.8
3	4.73	9 x 11 (60°)	15.18	82.2
4	4.38	10 x 12 (60°)	13.8	85.4
5	3.63	11 x 15 (56°)	15.18	80.7
6	3.28	14 x 17 (56°)	13.8	76.3
7	3.10	14 x 17 (59°)	15.64	84.9

The conclusion of the investigation is that a wide range of cell sizes can be accommodated. The panel design discussion that follows is based on an 11 x 15 array of 3.63-in. (93.5-mm) cells. As the cells get smaller, the number of parallel strings gets larger, and it becomes more difficult to divide the array evenly into strings. Notice that the circuits with six or seven parallel strings do not terminate on the panel diagonal since both involve two passes on the panel of the electrical circuit. Thus, strictly speaking, the 3.63-in. cell is the smallest size which meets all three design constraints. The choice among the larger cell size alternatives must be based on consideration of circuit redundancy to achieve panel life and the feasibility of the appropriate cell geometry. On both counts, the 3.63-in.-diameter cells (which coincidentally deliver exactly 1 W maximum) arranged in five parallel strings would be entirely satisfactory.

2. Panel Design

Figure 19 shows the cell layout for the base line panel design. It contains 165 cells each 3.63 in. in diameter and positioned as shown on the drawings. Circuit terminations are bonded into the diagonal corners. Interconnection is made to the 1/4-in. stud shown using a nut and lockwasher. The stud is electrically isolated from the mounting structure by a plastic sleeve bonded to the backside of the panel. Double-strength clear-glass sheet has been used for the substrate and the window for the mechanical panel model shown in Fig. 20.

3. Structural Aspects and Panel Design

The basic aspect of the glass packaging approach is the similarity to honeycomb structural panels. A matrix of epoxy dots with spacer disks takes the place of the honeycomb core. The cover sheets are the two glass sheets; therefore, the two glass sheets must be of equal thickness for proper functioning. The shear stress on the epoxy dots can be determined from the horizontal beam. This shear stress at 50-psf loading for two 1/8-in. sheets is 50 psi at the center and 100 psi at the outer edges. Assuming a 5% area

(a)

(b)

(c)

Figure 19. Cell layout for base line panel design.

Figure 20. Photograph of mechanical panel model.

coverage allowance for the dots, this becomes a 2000-psi bond stress. At present, a 50% mixture of epoxy (Epan 828) and polyamide is being used which has a bond strength of 3000 psi.

The border of epoxy 1/2 to 1 in. wide may be needed for sufficient bond strength and as a sealant. At present several 1-ft² assemblies and a 2- x 2-ft assembly have been made without cells using 1/8-in. sheet glass.

Using 1/8-in. glass, a 4-ft panel would weigh 53 lb. Reduction of the glass thickness to single strength would increase panel breakage beyond normal architectural standards when loaded to design values. In order to cut weight and gain the cost saving (22%) of 0.093-in. glass over 1/8-in., it may be necessary to increase the core thickness. However, this must be done without impacting internal construction costs.

D. SYSTEM APPLICATIONS

The panel design being pursued is based on the concept that it should require the simplest kind of mounting superstructure and achieve the maximum packing factor. The panel design to meet these requirements was shown in Fig. 19. The panel can deliver 165-W peak power at a nominal voltage of 15.2 Vdc.

The panel is designed for electrical termination on diagonal corners through a 1/4-in. stud terminal which is intended for panel interconnection at a junction boxed on the backside of a 30-panel photovoltaic unit as shown in Fig. 21. The terminations are structurally bonded between the panel glass sheets to provide field ruggedness for the panel. The panel perimeter is sealed against moisture penetration by a duplex sealant of polyisobutylene and structural epoxy. Panels can be glazed into the unit frame using conventional insulated glass window techniques. The design is configured to meet the expected environmental stresses of wind, snow, rain, and hail and have a useful life in excess of 20 to 30 years.

1. System Configuration

A possible system configuration for the proposed panels would be to wire them in series-parallel fashion so that a 30-panel unit would operate at 225 Vdc. Twelve units can be wired in series-parallel fashion to form a power section which nominally has an output of 675 Vdc but can be electrically reconfigured to a circuit of four series units to accommodate shifting of the maximum power point at reduced panel isolation. We have called this twelve-unit assembly a power section as shown in Fig. 22. The tilt angle (ϵ) for a power section, its spacing (s) from adjacent sections, and presence or orientation (θ) of a reflecting panel must all be determined from system analysis with performance and cost effectiveness the primary criteria.

In summary, the system analysis will be required to account for:

- geometry parameters
- diurnal insolation variation
- shadowing
- load matching

Figure 21. Panel design of electrical connections.

Figure 22. Power section and tilt angles.

2. Solar Array Superstructure

It is necessary to structurally secure solar panels to the earth at a cost which does not significantly add to the cost of the basic panel which is estimated at \$5.00/ft². This cost will include the land on which the installation is located and the superstructure which secures the panels to the land. If we estimate the cost of the land as \$1000/acre and a fence surrounding it at \$15/ft, a 1-mile² site would cost approximately \$1 million or \$0.036/ft².

For maximum land usage (i.e., maximum collector area per land area), the angle of inclination should be 0°, a flat collector. Panel inclination is desirable from a solar flux standpoint. In order to maintain full exposure on collectors without self-shadowing for a solar altitude angle of 23° (from the

horizontal) (44°N latitude location) the row spacing is 15.1 ft. This results in a land usage ratio (LUR) of 0.584; for a 40° angle of inclination, spacing is 25.24 ft and the LUR is 0.487. A flat (horizontal) collector with 3-ft-wide access paths between each section (20 x 288 ft) has an LUR of 0.859. See Table 7 for comparisons.

TABLE 7. LAND USAGE

<u>Inclination Angle (degrees)</u>	<u>LUR</u>	<u>BTU/Yr/Ft^{2*}</u>	<u>BTU/Mi^{2**}/Yr</u>
0	0.859	267,200	6.399×10^{12}
20	0.584	303,720	4.945×10^{12}
40	0.487	314,206	4.266×10^{12}

*Collector area

**Land area

Because the land is inexpensive compared with the collector, a tilted collector is the most cost-effective.

It is desirable to keep the number of ground support points (piles, bell footings, spread footings, caissons) to a minimum due to their relatively high cost (\$25 - \$100 per ground support point (GSP) depending on ground conditions and type of GSP employed). Consequently, GSPs become more economical as loading per point is increased.

To achieve this objective, a cantilevered four-point support structure could be employed (see Fig. 23). This structural scheme has been evaluated on a cost basis for both lumber and steel construction; see Tables 8 and 9.

Quantity and load-bearing capacity of GSPs are the same for lumber or steel. In terms of cost comparisons:

<u>Cost/Unit</u>		<u>Cost/Unit</u>	
Lumber	\$144	Steel	\$533
Creosote	\$ 50	Galv.	\$121 or paint \$13.25
Total	\$194	\$654	or \$546

TABLE 8. SUPERSTRUCTURE COST USING LUMBER CONSTRUCTION

Designation	Length Linear Ea. (ft)	FBM* Ea.	Quantity	Total FBM	\$/FBM	Cost/ Unit
A	24	72	2	144	0.340	\$48.96
B	20	33-1/2	7	233-1/2	0.255	59.50
C ₁	4	2-2/3	24	64	0.440**	28.16
C ₂	24	16	2	32	0.220	7.04
Totals				473-1/2		\$143.66

*FBM - foot board measure

**2:1 markup for cutting lumber to size

NOTE:

Cost to creosote wood - \$106/1000 FBM
 473-1/2 FBM x \$106/1000 FBM = \$50.17

Total cost (material only) \$194

TABLE 9. SUPERSTRUCTURE COST USING STEEL CONSTRUCTION

Designation	Type	Size Designation (in.)	Quan.	Length Ea. (ft)	lb/ft	lb/Unit	\$/lb	\$ Cost/ Unit
A	I-beam	5 x 3 x 0.21 web	2	24	10	480	0.255	122.40- 110.16**
B	Channel	36 x 1.4 x 0.71 web	7	10	4.1	287	0.255	73.19
C ₁	Channel	1-3/4 x 1-1/4 x 1/4 thick	24	4	2.34	225	1.0*	112.32 63.3% of total
C ₂	L-angle	1-3/4 x 1-1/4 x 1/4 thick	2	24	2.34	112	0.50	112.32
Total						1104		\$533

*2:1 markup was used to compensate excessive cutting

**using 5-in. channel reduces lb/ft to 9 lb

NOTE:

Galvanizing - \$220/ton of steel (for over 20-ton run)

\$121/unit to galvanize - 400 ft²/ton x 0.06/ft² to spray x 0.552
 ton = 13.25/unit to paint

Figure 23. Ground support structure.

To determine cost/unit/area:

- *Wood* (with creosote) $\$194/\text{unit} \times 1 \text{ unit}/480 \text{ ft}^2 = \$0.404/\text{ft}^2$ not including GSPs $\$0.404 \times 15,707,520 = \$6.35 \text{ million for } 1 \text{ mile}^2$.
- *Steel* (with paint) $\$546/\text{unit} \times 1 \text{ unit}/480 \text{ ft}^2 = \$1.14/\text{ft}^2$ not including GSPs $\$1.14 \times \$15,707,520 = \$17.9 \text{ million for } 1 \text{ mile}^2$.

Wood construction (creosote-impregnated) would, therefore, be favored for cost.

Additional design and analysis is required to refine these numbers and to better deal with the question of ground support point design and cost. In addition, the question of power distribution and conditioning must be addressed to determine the cost impact of the required hardware.

SECTION VII

CONCLUSIONS

A program has been developed to identify the significance of changes in the primary variables associated with array module manufacturing on array module performance. This program encompasses both analytical and experimental efforts, with the analytical effort focusing on distributions in the cell parameters and the interactions of these distributions. 506 wafers were started in this interval with about half completed through junction formation. Preliminary results indicate:

- (1) The lower the diffusion temperature, the better the short-circuit current, indicating that the carrier lifetime is degraded at higher temperatures.
- (2) Tighter distribution of sheet resistance is obtained with ion-implanted junctions than with spin-on source diffusions.

A cell matching analysis based on an assumed Gaussian distributed cell performance curve with $\sigma = 1\%$ suggests that 100% test and matching is a cost-effective procedure for power supply costs above \$0.50/W. For our 4- x 4-ft panel, several design criteria indicate that cell size of 3.6-in. diameter is optimum.

As finished wafers/panels emerge from our manufacturing operation, the effect of the variations in primary variables on panel performance will be documented.