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SURFACE EFFECTS ON SEMICONDUCTORS

PDO 6984892, Final Report

E. L. Rauch, Project Leader

Published January 1976

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Department 863

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Final Report

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Prepared by E. L. Rauch, D/863, under PDO 6984892

Semiconductor bi-polar and field-effect transistors were contaminated with sodium ions, subjected to high temperature reverse bias, measured electrically, and examined internally to study the effects of inversion, depletion, and accumulation in crystalline silicon. This study was terminated because of the inability to induce electrical degradation through surface contamination at a level consistently high enough to permit statistically valid correlations and conclusions.

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CONTENTS

Section	Page
SUMMARY	6
DISCUSSION.	7
SCOPE AND PURPOSE	7
ACTIVITY.	7
<u>Selection of Semiconductor Types. . . . .</u>	7
<u>Preparation and Application of Contamination. . . . .</u>	8
<u>2N2484 (NPN) Transistors. . . . .</u>	9
<u>2N2605 (PNP) Transistors. . . . .</u>	10
<u>2N3112 P-Channel Low-Current Junction Field-Effect Transistors . . . . .</u>	11
<u>2N4118A N-Channel Field-Effect Transistors. . . . .</u>	18
<u>M113 P-Channel Enhancement MOS Field-Effect Transistors . . . . .</u>	25
ACCOMPLISHMENTS	25
FUTURE WORK	25
BIBLIOGRAPHY.	28
DISTRIBUTION.	29

ILLUSTRATIONS

Figure		Page
1	2N3112 With Lid Removed (Polaroid)	9
2	2N2484: 6-Degree Cross Section; Junctions Delineated With a Preferential Etch (200X Polaroid).	12
3	2N2484: 6-Degree Cross Section; Oxide Over Junction Areas (400X Polaroid)	12
4	2N2484: Collector-Base Characteristics After 0.1 Percent Solution, 10 Second Air Dry (Polaroid)	13
5	2N2484: 0.1 Percent Solution (Polaroid)	13
6	2N2484: 0.1 Percent Solution, Device 60, Lead Corrosion (Polaroid)	14
7	2N2484: 0.1 Percent Solution, Device 60, Surface Corrosion (Polaroid)	14
8	2N2484: 0.1 Percent Solution, Device 51, Lead Corrosion (Polaroid)	15
9	2N2484: 0.1 Percent Solution, Device 51, Surface Corrosion (Polaroid)	15
10	2N2484: Base Post, 0.001 Percent Solution, Device 62, Lead Corrosion (Polaroid)	16
11	2N2484: 0.001 Percent Solution, Device 62 (Polaroid)	16
12	2N2484: 0.00001 Percent Solution, Device 71, Emitter Post, Lead Corrosion (Polaroid).	17
13	2N2484: 0.00001 Percent Solution, Device 71, Base Post, Lead Corrosion (Polaroid)	17
14	2N2484: 0.00001 Percent Solution, Device 80, Surface Contamination (Polaroid)	18
15	2N2605: 0.1 Percent Solution, Device 20, 22 Hours, Surface Metal Dissolved (Polaroid)	19
16	2N2605: 0.1 Percent Solution, Device 15, 22 Hours (Polaroid).	19

17	2N2605: Device 16 Collector-Base Characteristics (Polaroid).	20
18	2N2605: Device 7 Collector-Base Characteristics (Polaroid).	20
19	2N2605: Device 2 Collector-Base Characteristics (Polaroid).	21
20	2N2605: Device 4 Collector-Base Characteristics (Polaroid).	21
21	2N2605: Device 5 Collector-Base Characteristics (Polaroid).	22
22	2N2605: Device 4 Common Emitter Characteristics (Polaroid).	22
23	2N3112: P-Channel FET Device 7127 (300X Polaroid)	23
24	2N3112: P-Channel FET Device 7127 (600X Polaroid)	23
25	2N4118A: N-Channel FET Device 7402 (100X Polaroid)	24
26	2N4118A: N-Channel FET Device 7402 (300X Polaroid)	24
27	M113: MOS FET Device 7250 (100X Polaroid). . .	26
28	M113: MOS FET Device 7250 (200X Polaroid). . .	26
29	M113: MOS FET (Protective Diode) Device 7250 (Polaroid)	27

TABLES

Number		Page
1	Semiconductors Used in Evaluation.	8
2	2N2484 (NPN) Electrical Test Results	10
3	Data From Physical Examination of 2N2484 (NPN) Transistors.	11

SUMMARY

An investigation was made of the effects of positive ion contamination in producing inversion, depletion, and accumulation in semiconductor devices. Sodium chloride was used as a source of positive ion contamination because sodium ions have a high diffusion rate in silicon oxide. The investigation included bi-polar and field-effect semiconductors.

Although electrical degradation was produced at a level which would pose serious reliability problems, the rate of occurrence and repeatability was not compatible with the goals of this study. Further, the contamination of internal surfaces of assembled devices does not simulate the contamination that can occur during wafer fabrication. Contamination can be introduced during any number of supplier wafer processing steps prior to metal deposition.

The investigation was terminated when it became evident that an ion contamination level sufficient to produce statistically significant electrical degradation corroded the aluminum metal systems severely enough to preclude obtaining meaningful data.

DISCUSSION

SCOPE AND PURPOSE

Degradation of electrical characteristics of semiconductors occurs as the result of mobile ions on and in the junction passivation material. The underlying silicon is then depleted, inverted, or accumulated depending on the ion polarity and level of contamination, the type of semiconductor material, and the conductivity of the semiconductor material.

These effects may alter the junction depletion region enough to include new areas of imperfection, produce channels through which leakage currents may flow, or provide recombination centers for minority carriers. The electrical parameters affected, the potential at which the onset of degradation occurs, and the magnitude of degradation depend on device configuration, the type of device, and the degree of ion contamination.

This investigation attempted to contaminate groups of bi-polar (NPN and PNP) transistors, P- and N-channel junction field-effect transistor, and insulated gate field-effect transistors in a controlled manner with sodium ions.

The purpose of the investigation was to provide a more complete understanding of contamination effects on electrical parameters. This would permit a more comprehensive evaluation of new semiconductors and failure analyses of all types of semiconductor devices that fail as a result of surface contamination.

ACTIVITY

Selection of Semiconductor Types

Five types of semiconductors particularly susceptible to surface contamination were selected for evaluation. These included NPN low-current high-gain bi-polar transistors, PNP bi-polar transistors, insulated gate field-effect transistors, P-channel junction field-effect transistors, and N-channel junction field-effect transistors. Each group of commercial grade semiconductors was procured with a single manufacturing date code to provide homogeneity with the group (Table 1).

Samples of each device type were examined to determine if these units were acceptable for use in the evaluation. Key electrical parameters, including leakage current, low current gain, and offset voltage, were measured to determine their magnitude and

Table 1. Semiconductors Used in Evaluation

Designation	Quantity	Manufacturer	Date Code
2N2484 (NPN)	200	Fairchild	335
2N2605 (PNP)	200	National	7247
2N3112 (P-Channel)	200	Siliconix	7124
2N4118A (N-Channel)	200	Siliconix	7402
M113 (MOS FET P-Channel)	100	Siliconix	7250

distribution. Samples of each type were dissected, examined, and photographed to determine the type of structure, materials, and general workmanship.

Preparation and Application of Contamination

A 10-percent solution of chemically pure sodium chloride and distilled water was prepared using 3.6 grams of sodium chloride in 100 milliliters of distilled water. A calibrated syringe was used to prepare further dilution by successive steps to obtain 0.1-, 0.001-, and 0.00001-percent saturated solutions of sodium chloride for contaminating the semiconductor devices.

The solutions were applied to the semiconductor dies after removing the tops of the cases with a cutting tool. A typical opened device is shown in Figure 1. Several methods of applying the sodium solution were investigated.

- Method 1A: A hypodermic syringe was used to fill the case with solution. The liquid was allowed to evaporate and form a film of sodium chloride on the interior surface of the case and over the die.
- Method 1B. The same procedure was used as in Method 1A; however, the solution was allowed to remain only for a specified time after which the device was rinsed in water and air dried.
- Method 2. The device was submerged in a solution for a specified time followed by a rinse and air dry.

Figure 1. 2N3112 With Lid
Removed

2N2484 (NPN) Transistors

A lot of 200 2N2484 (NPN) transistors was screened electrically using the Tektronix 576 curve tracer to determine that the devices were stable and that no abnormal or unstable leakage currents existed. This was followed by recorded measurements on 75 serialized units for leakages and gain at 4 levels of current using the Fairchild 600 semiconductor tester.

Three groups of 10 each of the serialized units were treated with 0.1, 0.001, and 0.00001 percent solutions of sodium chloride using Method 2 and an application time of 10 seconds. Five additional devices were used as a control group.

No change in characteristics was noted when the devices were retested after treatment. A high temperature reverse bias of 20 volts was applied to the collector base junctions for 4 hours at 125°C. Electrolysis produced corrosion of the metallization and bond wires which was a function of the level of contamination (Table 2). Post HTRB electrical tests on the remaining units did not show any degradation in leakage or current gain.

Table 3 lists the results of a physical examination of a 2N2484 (NPN) transistor. A cross section of a 2N2484 (NPN) device is

Table 2. 2N2484 (NPN)
Electrical Test Results

Percent of Sodium Chloride Contamination	Number of Open Circuits
0.1	10
0.001	5
0.00001	3

shown in Figures 2 and 3. Figures 4 through 14 show die surfaces and effects of various levels of sodium chloride contamination.

2N2605 (PNP) Transistors

The lot of 200 2N2605 (PNP) transistors was screened for abnormal characteristics or unstable leakage using the Tektronix curve tracer.

Twenty units were tested with the Fairchild 600 semiconductor tester and data was recorded. Parameters included ICBO, IEBO, and HFE at five levels of collector current.

The units were submitted to a 5-hour soak in a 0.00001 percent solution of sodium chloride using Method 2. The surface metal was badly eroded but the gold bond wires were not affected. No electrical degradation was noted on retest or following a 24 hour, 20 V, $\pm 125^{\circ}\text{C}$ HTRB.

The same units were further subjected to a 0.1 percent solution of sodium chloride for 22 hours. The surface aluminum metallization was entirely removed except under the gold ball bonds. Electrically ICBO increased slightly. The maximum value was 40 nanoamperes. A 24-hour HTRB was performed at 20 V and 125°C . Nine devices were electrically degraded; ICBO increased and the low current HFE increased because of large leakage currents. Electrically the leakage appeared as a step increase at low voltages, which is an indication of an inversion channel. Figures 15 through 22 show the effects of various levels of contamination on these devices.

Sodium-chloride-induced contamination of the 2N2605 does not appear to be a practical way of evaluating surface contamination. Severe damage to the metal system and gross contamination occurred at contamination levels high enough to cause electrical degradation.

Table 3. Data From Physical Examination of 2N2484
(NPN) Transistors

Feature	Data
Case Size	TO 18 Metal Can
Internal Post	Gold Plated
Bond Wire	25.4 μm Aluminum
Die Geometry	Concentric Ring
Emitter Junction Passivation	Silicon Oxide
Collector Junction Passivation	Silicon Oxide
Base Width	1.1 μm
Base Diffusion Depth	6.5 μm
Epitaxial Thickness	20 μm
Guard Ring	N + Diffusion

2N3112 P-Channel Low-Current Junction Field-Effect Transistors

These devices are manufactured by Siliconix. The drain and source are connected to overlay aluminum bonding pads and connected to the posts with 1-mil (25.4 μm) gold ball bonds. The gate diffusion is internally connected to the die bulk material. The die is mounted on a nail-head isolated post. No guard-ring or channel stop diffusion is used (Figures 23 and 24).

The lot was screened using the curve tracer for unusual characteristics, and measurements of pinch-off voltage, drain source leakage, and gate source leakage were recorded for a sample.

Ten devices were contaminated with a 0.00001 percent solution of sodium chloride for 1 hour using Method 2. The devices were then retested and found to be essentially unchanged. An HTRB test was performed with the gate-to-source voltage of 10 V at 125°C for 24 hours. Upon retest the units showed an increase of approximately 10 percent in pinch-off voltage and leakage currents. Contamination of the junctions should have produced an inversion of the P-drain and source and decreased the pinch-off voltage and drain source current. It is concluded that the induced leakage is at the surface and not at the junction interface or related to the inversion phenomenon.

Figure 2. 2N2484: 6-Degree Cross
Section; Junctions
Delineated With a
Preferential Etch (200X)

Figure 3. 2N2484: 6-Degree Cross
Section; Oxide Over
Junction Areas (400X)

Figure 4. 2N2484: Collector-Base Characteristics After 0.1 Percent Solution, 10 Second Air Dry

Figure 5. 2N2484: 0.1 Percent Solution.

Figure 6. 2N2484: 0.1 Percent Solution,
Device 60, Lead Corrosion

Figure 7. 2N2484: 0.1 Percent Solution,
Device 60, Surface Corrosion

Figure 8. 2N2484: 0.1 Percent Solution, Device 51, Lead Corrosion

Figure 9. 2N2484: 0.1 Percent Solution, Device 51, Surface Corrosion

Figure 10. 2N2484: Base Post,
0.001 Percent Solution,
Device 62, Lead Corrosion

Figure 11. 2N2484: 0.001 Percent
Solution, Device 62

Figure 12. 2N2484: 0.00001 Percent
Solution, Device 71,
Emitter Post, Lead Corrosion

Figure 13. 2N2484: 0.00001 Percent
Solution, Device 71, Base
Post, Lead Corrosion

Figure 14. 2N2484: 0.00001 Percent
Solution, Device 80,
Surface Contamination

Experiments disclosed that higher levels of contamination caused corrosion of the overlay aluminum interconnects. Additional evaluation therefore does not appear to be justified.

2N4118A N-Channel Field-Effect Transistors

These devices were manufactured by Siliconix with a common date code of 7402. However, both ultrasonic bonded aluminum wire and ball-bonded gold wire processes were used in the lot. The bond pads and overlay metallization for the source and drain are aluminum. The gate diffusion is internally connected to the die bulk material and the die is attached to an isolated gold pad connected to an isolated lead. A guard field diffusion is used to reduce the effects of inversion. Figures 25 and 26 show internal construction and die surface.

Ten units were electrically tested for pinch-off voltage, IDSS, and IGSS leakage. The units were then subjected to a 1-hour soak in a 0.00001 percent solution of sodium chloride using Method 2. The electrical characteristics were retested and were essentially unchanged. Following a 24-hour HTRB test at 125°C and with 10 V applied between the gate and source-drain, the devices were retested. IDSS in general decreased an average of 24 percent, indicating a closing down of the channel.

IGSS remained unchanged on all units except two devices which had an increase in IGSS in the picoampere range. Pinch-off voltage remained unchanged.

Figure 15. 2N2605: 0.1 Percent Solution,
Device 20, 22 Hours, Surface
Metal Dissolved

Figure 16. 2N2605: 0.1 Percent Solution.
Device 15, 22 Hours

Figure 17. 2N2605: Device 16
Collector-Base
Characteristics

Figure 18. 2N2605: Device 7
Collector-Base
Characteristics

Figure 19. 2N2605: Device 2
Collector-Base
Characteristics

Figure 20. 2N2605: Device 4
Collector-Base
Characteristics

Figure 21. 2N2605: Device 5
Collector-Base
Characteristics

Figure 22. 2N2605: Device 4
Common Emitter
Characteristics

Figure 23. 2N3112: P-Channel
FET Device 7127 (300X)

Figure 24. 2N3112: P-Channel
FET Device 7127 (600X)

Figure 25. 2N4118A: N-Channel
FET Device 7402 (100X)

Figure 26. 2N4118A: N-Channel
FET Device 7402 (300X)

From a study of the diffusion profile and physical construction of the device it was anticipated that an accumulation of the N-channel diffusion or a depletion of the P-gate-substrate diffusion would occur from contamination with positive ions. This is an opposite affect to the measured decrease in IDSS.

Increased levels of sodium contamination created severe damage to the aluminum metallization. Further evaluation does not appear warranted.

M113 P-Channel Enhancement MOS Field-Effect Transistors

A sample of this device was opened and examined to determine construction detail and materials used in fabrication of the device. A static discharge protective zener is connected between the gate and case. Gold wire is ball-bonded to the aluminum metallization pads (Figures 27 through 29).

Ten devices were tested on the curve tracer for threshold voltage and drain cut-off leakage.

Based on evaluations performed on other device types it was concluded that the low levels of contamination would chemically erode the diode and gate overlay metallization and no attempt was made to contaminate these units.

ACCOMPLISHMENTS

Relatively high concentrations of sodium ions are required to degrade the electrical characteristics of assembled bi-polar and field-effect transistors. The doped oxides, guard fields, and overlaying metallization used during manufacture apparently provides an effective protection so that degradation does not occur with minute levels of positive ion contamination. Relatively low concentrations of sodium chloride are sufficient to corrode the aluminum thin film metallization used on semiconductor devices.

FUTURE WORK

The investigation and correlation of inversion, depletion, and accumulation of layers on semiconductors with electrical characteristics through the application of controlled levels of sodium chloride does not appear feasible. The high levels of contamination required to produce electrical degradation produce severe chemical reactions and degrade thin metal plating. Consequently it is recommended that the investigation be terminated.

Figure 27. M113: MOS FET Device
7250 (100X)

Figure 28. M113: MOS FET Device
7250 (200X)

Figure 29. M113: MOS FET (Protective Diode) Device 7250

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