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AN INTERPROCESSOR INTERFACE FOR DATA TRANSFER BETWEEN
PDP-8/L AND NOVA 1220 DEDICATED GAMMA ENERGY ANALYSIS
SYSTEMS

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MASTER

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AND NOVA 1220 DEDICATED GAMMA ENERGY ANALYSIS SYSTEMS

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RICHLAND, WASHINGTON

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ABSTRACT

A method for data communication between PDP-8/L and NOVA 1220 computer based multichannel analyzer systems is described. The method is implemented by modification of each system's operating program with appropriate I/O subroutines and by installation of a minor amount of hardware logic to a NOVA general purpose interface board. The method provides for high speed transfer of gamma energy analysis data between a Nuclear Data Corporation 50/50 system and a Tracor-Northern Corporation 660 system.

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INTRODUCTION

Qualitative and quantitative analysis of radioactive nuclides may be conducted for gamma ray emitting mixed nuclides using high resolution lithium drifted germanium [Ge(Li)] diode detectors, fast analog to digital conversion, core memory data storage, and computer program data reduction. Two separate "turn key" systems provided by prominent vendors in the field are the Nuclear Data Corporation 50/50 System (Figure 1) and the Tracor-Northern Corporation 660 System (Figure 2). The former is based on a Digital Equipment Corporation PDP-8/L computer and the latter on a Data General NOVA 1220 Computer. Each system has 24 bit word size peripheral data storage in 4K (K=1024) blocks. The computers have 4K by 12 bit and 8K by 16 bit memories respectively.

As dedicated systems, each unit was custom programmed compactly in assembly language for data reduction independently of data collection and storage which is a strict hardware function. The 50/50 system software was designed for efficient use in detector systems setup, evaluation and design and/or analysis of unordinary samples. The 660 system software was designed for automated analysis capable of using tabulated information on-line to select spectral regions of interest and/or parameters for proper reduction to final sample constituent reports. It was desirable that the two systems be capable of reducing data originating in either system as the need arose.

An interprocessor hardware interface was designed and implemented such that each machine became a peripheral to the other. Existing software was modified to allow program control of the hardware and word size restructuring. This document describes the system background and approach to the design of the interface and to the modification of the systems which provide the communication requirement noted above.

SUMMARY

Both the interprocessor hardware interface and the driving software were built and used for data communication between the two separate computer based gamma energy analysis systems. The resulting interface provides a method for high speed data transfer of energy spectra bi-directionally between disparate systems. The interface was implemented from both standard components and off the shelf materials.

DISCUSSION

BACKGROUND

Gamma Energy Analysis (GEA) is commonly performed with a suitable detector system over a 50 keV to 2 MeV gamma energy range which covers nearly all of the energies spontaneously emitted by radionuclides of interest. Since gamma events can occur very frequently, the industry developed fast counting hard-wired analyzers with computer type memories under direct control of an analog to digital converter (ADC). The computer memories used are typically core type, 4K by 24 bit word or channel* systems.

The large block of data produced by the analysis which is shown in the spectral histogram (Figure 3), gave users a tremendous problem in rapidly reducing the collected data into meaningful results. Early systems physically printed the data directly using mechanical and optical printers ranging in speed from 40 to 200 channels per second for later hand calculation. Clearly, faster automated systems were needed to speed up production.

The introduction of low cost mini computers provided a quick and accurate means of reducing the voluminous data. While other software systems using large scale batch computers were in use, the first local real time automation example was the 50/50 system. Subsequent systems have been patterned after this in both custom and commercial systems.

THE 50/50 SYSTEM

The 50/50 system consists of four psuedo-independent analyzers, each with a separate ADC, clock timer, and 4K by 24 bit memory module. Data

*Channel is a holdover from very early scanning single channel analyzer systems.

may be collected and visually displayed both during and after collection without computer support. At reduction time, the operator actuates the memory block of interest for on line work.

When brought on line, the computer can access the memory address register, the memory data registers, and various functions within memory control. Since the analyzer data is 24 bits/word, the memory data register is split into two 12 bit addressable fields. The computer may read and/or set a 12 bit address in one operation but requires two functions to operate on the 24 bit data word. These interface functions are found in the analyzer which is on an extension of the computer's input/output (I/O) bus. The operator performs functions on the data by using a custom two character command language with modifiers which are initiated through a system teletypewriter (TTY) terminal. The computer program which services the TTY commands on interrupt basis performs its function in the background after it completes decoding in the foreground. All analyzer control functions are executed by programmed I/O and the program returns to an interrupt monitor at the end of each function. Typical functional commands are Reduce Peak (RP) and Print Data (PR).

The 50/50 program is highly interactive, depending on operator sequencing of parameter input for each peak to be reduced. Although compactly written in assembler, the program requires additional table storage in the last page (128 channels) of each analyzer block. Little room is available to allow for automatic sequencing of commands for routine analyses. However, the system is excellent for detector development and unusual samples.

THE 660 SYSTEM

Although similar in concept and operation to the 50/50 system, the 660 system has only two 4K data modules driven by a single ADC. Currently operated in a single 4K mode, the memory and ADC can be set up for recent detector resolution improvements to yield separations of one part in 8K.

The 660 operator performs data reduction through a console unit in much the same manner as for the 50/50. However, automatic peak selection and reduction use tables stored in the computer, thus requiring a larger memory (8K) than the 50/50 system capability. In contrast by using the 660 system, both interaction and modification of analysis steps are sacrificed to expedite routine sample analyses.

Computer control of the memory is via extension of the I/O bus to the analyzer interface. Since the machine is a 16 bit processor, the 24 bit memory data is divided into fields of 8 and 16 bits.

Not noted previously is the analytical collection time data (in seconds) which is stored in the first channel of the appropriate memory block. The 660 assumes this to be channel 0 and the 50/50 system assumes it to be channel 1. Energy scale in the remaining memory is dependent on the calibration of the ADC.

PROCESSOR INTERFACE

Preliminary Considerations

At the time of purchase of a second 660 system (Figure 2), it was known that a need existed to reduce data originating in either a 660 or the 50/50 system by the other. At that time it was decided to interface the 50/50 to a 660 system using a general purpose interface board from Data General Corporation (4040/1) which was purchased at that time. Preliminary study showed that an interprocessor interface could be implemented quite easily by making a few changes to the purchased board and software.

To produce a relatively simple interface incorporating as many readily available components as possible was the primary goal of the interface design. Some limiting design policies were established to enhance simplicity. First, since rewriting software interrupt service routines for the compactly written systems would be too involved, interrupt logic was avoided. Second, since data is only transferred after completion of data collection the option of programmed I/O would be adequate with proper attention to procedure and software switch design. With these policies in mind, the following features were implemented.

Design Features

Due to space limitations in the PDP-8/L, all interface logic is external and by convenience was placed on the 4040/1 board in the NOVA 1220. In addition to integrated circuit chip sockets for user logic, this board contains data latch registers, "busy-done", and decode logic. All that remained was the addition of the PDP-8/L device decode and control logic.

An additional I/O connector was wired to each computer system (Figures 4 and 5). The connector for the PDP-8/L was wired directly to the I/O bus of the 50/50 system. The connector for the 660 was wired to available user pins on the back plane for the top I/O board slot of the mainframe (Figure 5) of the NOVA central processing unit (CPU).

Due to the physical placement of the counting systems, a 25 foot cable was built for system connection. Multiconductor flat ribbon cable was used with alternate conductors wired to ground to improve noise immunity. Termination of PDP-8/L I/O control signals of short duration was also included in the interface.

All user logic was provided by use of standard integrated circuit logic chips (Figure 6). Since both machines have TTL logic, no special signal transformations were necessary.

Logic Control Functions

As mentioned data transfer is effected by direct programmed I/O. For this, a set of software instructions were defined to operate on the interface. This section describes the function of each command used directly in the software control of the interface. Definitions of computer instructions and hardware signals may be found in the appendices, Figure 8 and references 1 - 3.

<u>Command</u>	<u>Source</u>	<u>Description</u>
ARSB	50/50	At IOP4 time device code 62 ₈ sets DONE.
DIA NDNS	660	Device code 66 ₈ loads data from the input register as buffer A onto the I/O bus.
DOA NDNS	660	Device code 66 ₈ loads the output register as buffer A from an accumulator.
DIB NDNS	660	Device code 66 ₈ causes a load of an accumulator with zero data.
DIBS NDNS	660	Same as DIB NDNS except that DONE is cleared and BUSY is set on device 66 ₈ .
IDIR	50/50	At IOP1 time, device 61 ₈ generates AC Clear to clear the PDP-8/L accumulator. At IOP4 time, the contents of the interface output register are gated out and OR'd into the PDP-8/L accumulator.
IPIS	50/50	At IOP2 time, device 62 ₈ and with $\overline{\text{DONE}}$ produces $\overline{\text{I0SKIP}}$ in the PDP-8/L.
NIOS NDNS	660	Device 66 ₈ sets its BUSY and clears DONE; no data is transferred.
ODIR	50/50	At IOP1 time, device 62 ₈ strobes PDP-8/L accumulator data into the interface input register.
SKPDN NDNS	660	Device code 66 ₈ causes an instruction skip if DONE is nonzero.

SOFTWARE MODIFICATIONS

As mentioned above, existing software was compactly written primarily for program space conservation. Therefore, major revisions to the basic operating systems was not practical. The overall approach to software modification included writing self contained subroutine overlays to little used existing routines in each system. The following is a brief description of the affected areas, scope of the new routines, and the basic logic of each.

50/50 Program

One interactive feature of the 50/50 system is the ability to set a visual marker bar ("MARKER") at a selected point in the spectrum under program control. Another routine ("TYPED") is used to type blocks of data in a special format. These two routines are rarely used at the expense of each other in overlay fashion. Their core locations were thus delegated for use by the new interface driver subroutine "XRfer".

The new subroutine (Appendix A) requires 75 decimal locations beginning at octal memory location 5000. Actual data transfer is controlled by a bidirectional routine (XR) set up at initialization time. The remaining hardware control functions are those used for normal 50/50 data reduction operation.⁴ The flow of the program is described in the following paragraphs.

After the system monitor has successfully matched the "XR" command, an indirect jump is executed to the start of the subroutine. An initial message is typed to assure the operator of the data direction. The direction is sensed by the condition of the switch farthest to the left on the computer console switch register (SR). Normal operation mode is to the 660 system with the switch in the reset position. The message is slightly different for the opposite condition (Figure 9).

After the initial message is typed the program halts to allow for final checks by the operator. At this point, the computer has not accessed the analyzer. Therefore, the operator can reselect the memory bank of interest and can also reselect directional mode if an assumptive error has been made. When conditions are satisfactory, the operator must actuate a continue command on the computer console.

After continuation of the program, the memory bank is brought on line, the direction is again sensed and the interface is initialized. From this point the computer reads/stores/transfers 12 bits of data at a time until end of transfer is sensed. For every 24 bit analyzer word, two interprocessor transfers are made and each transfer is made only if the interface logic is reset. No data restructuring is provided or necessary in this routine.

When the end of the transfer is sensed by software counter an ending message is typed (Figure 9). As the message is finished, the analyzer is returned to off-line status and the computer returns to the TTY interrupt monitor. Provided no other routines are executed by the operator, the program may be restarted with the TTY 'alt mode" key as with other commands.

660 Program

The 660 system software was designed in the same fashion as that of the 50/50. The system is basically a foreground terminal interrupt monitor with execution of decoded commands in the background. A maximum of 26 decoded commands (A-Z) with modifiers may be provided at system purchase time. As in the case of the 50/50, a little used routine (transfer of data between analyzer memory subfields) was sacrificed for the interprocessor operations. In the following discussion of the new 660 subroutine (Appendix B), only departures from the 50/50 subroutine features are discussed.

As implied above, the 660 system command language is much more restrictive than that of the 50/50 system. In general, only one character from the 660 console terminal is required to start a routine and any modifiers/switches must be handled by the executing routine. The new subroutine is entered with a "T" command decoded to relocatable entry point "TRANS" with directional modifier of either "I" or "O" (in/out).

The routine performs transfers/stores beginning directly after an initialization message. Unlike the 50/50 routine and because of data restructuring problems, a separate I/O driver is used for each direction. By design, the most significant 12 bits (MSB) of analyzer data are transferred first followed by the least significant bits (LSB). Since the NOVA central processing unit (CPU) is 16 bit, accumulator data is shifted for compatability with an 8MSB/16LSB format in the analyzer memory data registers. The restructuring is performed in the NOVA primarily from hardware considerations and secondarily due to availability of adequate program space.

Three additional differences are in the TRANS routine. First a programmed halt does not exist as only the directional mode is a variable and only one memory bank logically exists. Second, a software switch exists to assure that time data is stored in channel zero and that channel one is always skipped. The final difference is due to a design policy for the operating procedure. In order to assure that the two systems have synchronized transfer, the 50/50 system must be initialized first. The systems complete the transfer automatically and type a final message.

SYSTEMS PERFORMANCE

The interface and software were designed to effect analyzer core-to-core data transfer taking into account differences in hardware. The hardware and software were tested at various stages to assure correct implementation. The interface has proven to be effective and simple as was originally anticipated. Although no exact measurements of total transfer time for a spectrum were made, a stop watch estimate of less than 250 milliseconds was made exclusive of operator setup and message printout.

Although the interface worked exactly as planned, some unforeseen side effects were discovered. From past maintenance experience, it was known that the 50/50 hardware is extremely sensitive to interconnecting cable lengths and signal levels. While the 50/50 system would operate correctly in original normal modes, data transfer operations tended to induce random cross talk problems between memory modules not "on-line" physically or logically. It was found that a few weak chips in the analyzers were marginally sensitive to signal degradation on the PDP-8/L I/O bus as a result of activity on the extended bus cable. All problems were corrected by replacing three chips on the 50/50 memory control and routing modules and the project was successfully completed.

REFERENCES

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2. "Introduction to Programming PDP-8 Family Computers, "Digital Equipment Corporation, Maynard, Massachusetts, 1969.
3. "PDP-8/L Maintenance Manual," Volume II, Digital Equipment Corporation, Maynard, Massachusetts, 1970.
4. ND40-9006: Special Peak Reduction Program for Atlantic Richfield Hanford Company, June 1969, for use on PDP-8/L computer.
5. "NOVA-ARIS II (ARHCO)-AB-3E," Special Peak Reduction Program for Atlantic Richfield Hanford Company, July 1975, for use on NOVA 1200 computer.

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APPENDIX A

50/50 PROGRAM LISTING

This appendix contains the assembled source listing for the 50/50 system overlay subroutine and system linkages.


```

/ PROGRAM XRFER
/ 6-17-75
/
/ AUTHOR: GL TROYER
/ PROCESS CONTROL LAB.
/ ATLANTIC RICHFIELD HANFORD CO.
/
/ PROGRAM TO XFER DATA
/ BETWEEN 50/50 ANALYZER
/ AND ARIS ANALYZER.
/
/ OVERLAY OF MARKER/TYPE
/ ROUTINES, ACCESS FROM ASR35
/ KEYBOARD WITH 'XR'ALTMODE,
/ SETUP, CONTINUE ON CPU
/
/ SR(0)=0 OUT TO ARIS
/ SR(0)=1 IN FROM ARIS
/
/ RECYCLE WITH ALTMODE
/
/ DEVICE CODES 61 AND 62
/ DEFINITIONS FOR ASSEMBLY
PRINT = 4467 /PRINT ENTRY POINT
CONN = 6371 /GRAB MCA
BSF = 6372 /SKIP MCA NOT BUSY
CLRM = 6365 /CLEAR MCA ADDRESS
/ AND READ RESTORE MEM CYCLE
ARSB = 6624 /RESET IP10 6624
RMLA = 6457 /READ,CYCLE,INCR ADD
CRMM = 6443 /READ MEMORY MOST
CSMM = 6342 /SET MEMORY MOST
CLMM = 6341 /CLEAR MEMORY MOST
CSML = 6352 /SET MEMORY LEAST
CLML = 6351 /CLEAR MEMORY LEAST
EACS = 6335 /ERASE, WRITE, INCR ADR
END = 5471 /RETURN TO MONITOR
IPIS = 6622 /INTR-PROC I/O SKIP 6622
/
/ MONITOR DECODE VALUE
/
*300
0300 4756 4756 /DECODE (XR)
/
/ INDIRECT JUMP FROM MONITOR
/
*342
0342 5000 5000 /BEGN
/
/ ENTRY FOR START OF ROUTINE
/ FROM MONITOR
/
*5000
/
5000 4467 BEGN, PRINT
5001 0605 0605 /FE
5002 2240 2240 /R
5003 4065 4065 / 5
5004 6055 6055 /0-
5005 6560 6560 /50
5006 4000 4000 / 8
5007 7604 CLA OSR /GET MODE FROM SR
5010 7500 SMA /SR(0)=1 IN

```

5011	5217		JMP OUT	/SR(0)=0	OUT
			/		
5012	4467	IN,	PRINT		
5013	0622		0622	/FR	
5014	1715		1715	/OM	
5015	4000		4000	/S	
5016	5222		JMP PCON		
			/		
5017	4467	OUT,	PRINT		
5020	2417		2417	/TO	
5021	4000		4000	/S	
			/		
5022	4467	PCON,	PRINT		
5023	0122		0122	/AR	
5024	1123		1123	/IS	
5025	4744		4744	/CR-LF	
5026	4000		4000	/S	
5027	7402		HLT	/PAUSE	
			/		
			/PAUSE FOR OPERATOR CHECK		
			/		
5030	6373	CONT,	CONN BSF	/GRAB MCA, SKIP READY	
5031	5230		JMP .-1	/WAIT	
5032	6205		CLRM	/CLEAR 50-50 ADDRS	
5033	0624		ARSB	/RESET ARIS, 50-50	
5034	7200		CLA	/RESET ACCUM	
5035	1302		TAD P128	/GET CHAN OFFSET	
5036	3303		DCA CHAN	/SET CHANNEL CNTR	
5037	7404		OSR	/GET MODE SR	
5040	7710		SPA CLA	/SR(0)=0	OUT
5041	5255		JMP IIN	/SR(0)=1	IN
			/		
			/DATA TO ARIS		
			/		
5042	1305	IOUT,	TAD ODIR	/GET MODE	
5043	3311		DCA XFRI	/SET XFRI MODE	
5044	6372	ICON,	BSF	/SKIP MEM NOT BUSY	
5045	5244		JMP .-1	/WAIT	
5046	6443		CRMM	/READ MOST	
5047	4306		JMS XFR	/OUT MOST	
5050	6457		RMLA	/READ LEAST, MEM CY, INC AD	
5051	4306		JMS XFR	/OUT LEAST	
5052	2303		ISZ CHAN	/DONE?	
5053	5244		JMP ICON	/NO RECYCLE	
5054	5266		JMP FIN	/YES, FINISH	
			/		
			/DATA TO 50	/50	
			/		
5055	1304	IIN,	TAD IDIR	/GET MODE	
5056	3311		DCA XFRI	/SET XFRI MODE	
5057	4306	IICN,	JMS XFR	/GET MOST	
5060	6343		CSMM CLMM	/SET MOST	
5061	4306		JMS XFR	/GET LEAST	
5062	6353		CSML CLML	/SFT LEAST	
5063	6335		EACS	/MEMCY, INC. ADDRS	
5064	2303		ISZ CHAN	/DOE?	
5065	5257		JMP IICN	/NO, RECYCLE	
			/		
			/TRANSFER DONE, SAY SO.		
			/		
5066	4467	FIN,	PRINT		
5067	2422		2422	/TR	
5070	0116		0116	/AN	
5071	2306		2306	/SF	

5072	0522		0522	/ER
5073	4003		4003	/ C
5074	1715		1715	/OM
5075	2014		2014	/PL
5076	0524		0524	/ET
5077	0547		0547	/E CR
5100	4400		4400	/LF\$
5101	5471		END	/RETURN TO MONITOR
/				
/CONSTANTS AND VARIABLES				
/				
5102	0200	P128,	200	/CHAN OFFSET TO AVOID
				/LAST 128 CHAN OF MEM DATA CONSTANTS
5103	0000	CHAN,	0	/CHAN COUNTER
5104	6615	IDIR,	6615	/DATA IN COMMAND
5105	6621	ODIR,	6621	/DATA OUT COMMAND
/				
/I/O HANDLER				
/				
5106	0000	XFR,	0	
5107	6622		IPIS	/SKIP IF READY
5110	5307		JMP .-1	/CHECK AGAIN
5111	0000	XFRI,	0	/ I-O COMMAND
5112	6624		ARSB	/SET I-O BUSY, =0
5113	5706		JMP I XFR	/RETURN

APPENDIX B

ARIS PROGRAM LISTING

This appendix contains the assembled source listing of the transfer subroutine for the NOVA computer. The system user symbol table (DUSR entries) is also included.

0001 TRANS

000030 .DUSR DAC=30
000031 .DUSR CNTRL=31
000032 .DUSR MISS=32
000033 .DUSR MPER=33
000100 .DUSR MADRS=100
000101 .DUSR BINM=101
000102 .DUSR BINL=102
000103 .DUSR LONUM=103
000105 .DUSR DIFF=105
000104 .DUSR HINUM=104
000106 .DUSR MOST1=106
000107 .DUSR LEST1=107
000110 .DUSR MOST2=110
000111 .DUSR LEST2=111
000112 .DUSR LIMIT=112
000113 .DUSR INOUT=113
000114 .DUSR RTRN1=114
000115 .DUSR RTRN2=115
000116 .DUSR RTRN3=116
000117 .DUSR RTRN4=117
000120 .DUSR RTRN5=120
000121 .DUSR RTRN6=121
000122 .DUSR RTRN7=122
000123 .DUSR SPACE=123
000124 .DUSR ADDNT=124
000125 .DUSR SUBNT=125
000126 .DUSR FORMA=126
000127 .DUSR ERROR=127
000130 .DUSR TABST=130
000131 .DUSR TTYR=131
000132 .DUSR MCRT=132
000133 .DUSR MCOMP=133
000134 .DUSR ASBIN=134
000135 .DUSR SBASC=135
000136 .DUSR BTIPE=136
000137 .DUSR ADDEC=137
000140 .DUSR ZTYPE=140
000141 .DUSR MSTOP=141
000142 .DUSR ASCII=142
000143 .DUSR TSPAC=143
000144 .DUSR CRLF=144
000145 .DUSR RUNMD=145
000146 .DUSR IMSK=146
000147 .DUSR RDENC=147
000150 .DUSR MDENC=150
000165 .DUSR TYPMS=165
000166 .DUSR COMSK=166
000360 .DUSR ORIGIN=360
.EOT

0002 TRANS

```

;TRANSFER ROUTINE.  ENTER AFTER "T"
;SUBTASK
;T 1 (IN FROM PDP-8L)
;T 0 (OUT TO PDP-8L)

;
.TITL  TRANS                      ;NS-660-NOVA: PDP-8/L TRANSFER
.ENT   TRANS
;
.NREL
NDNS=66
000066
00000'006126 TRANS: JSR @FORMAT
00001'006131 JSR @TTYR
00002'040504 STA 0,SWAP ;STORE CHAR TEMP
00003'006165 JSR @TYPMS ;FRONT FIRST HALF
00004'000112' MSS1 ;OF I/O MSG.
00005'020501 LDA 0,SWAP ;RETRIEVE CHARACTER
00006'024407 LDA 1,CHARR
00007'122415 SUB# 1,0,SNR ;2ND CHAR "I"?
00010'000410 JMP ICON ;YES
00011'024405 LDA 1,CHARR+1 ;NO TEST NEXT CHAR
00012'122414 SUB# 1,0,SZR ;2ND CHAR "O"?
00013'002127 JMP @ERROR ;NO MATCH, ERROR
00014'000431 JMP OCON ;YES
00015'000111 CHARR: "I" ;IN FROM PDP-8
00016'000117 "O" ;OUT TO PDP-8
00017'000354 JMP ORIGIN-4 ;RETURN TO EXEC
;
;ENTRY FOR IN FROM PDP-8
;
00020'006165 ICON: JSR @TYPMS ;TYPE I/O
00021'000123' MSS2
00022'004451 JSR SETC ;STORE I/O INSTRUCTIONS.
00023'004541 GETD: JSR IIXR ;GET MSB 50/50
00024'152440 SUBO 2,2 ;ZERO TEMP AND CARRY
00025'165000 MOV 0,1 ;MOVE MSG TO AC1
00026'034461 LDA 3,M4 ;GET BIT COUNTER
00027'125200 MOVR 1,1 ;SHIFT RIGHT 1 BIT
00030'151200 MOVR 2,2 ;AND TRANSFER TO AC(2)
00031'175404 INC 3,3,SZR ;SHIFTED 4 BITS?
00032'000775 JMP .-3 ;NO
00033'102400 SUB 0,0 ;CLEAR AC(0)
00034'004530 JSR IIXR ;GET LSB 50/50
00035'143000 ADD 2,0 ;ADD IN HIGH BITS
00036'004507 JSR MOXFR ;AND OUTPUT TO MEM
00037'010446 ISZ ONE ;INCREMENT TIME CHANNEL FLAG
00040'000402 JMP .+2 ;FOR 50/50-ARIS COMPATIBILITY
00041'060332 NIOP 32 ;SKIP CHANNEL ONE
00042'010447 ISZ CLMIT ;XFR DONE?
00043'000760 JMP GETD ;NO GET MORE
00044'000424 JMP XFINI ;YES FINISH
;
;ENTRY FOR OUT FROM ARIS
;
00045'006165 OCON: JSR @TYPMS ;TYPE I/O
00046'000130' MSS3
00047'004425 JSR SETC+1
00050'004505 OUTD: JSR MIXFR ;GET ANALYZER DATA
00051'040435 STA 0,SWAP ;STORE LSB
00052'030435 LDA 2,M4 ;GET BIT COUNTER

```

```

0003 TRANS
00053'101120 MOVZL 0,0 ;SHIFT 1 BIT LEFT
00054'125100 MOVL 1,1 ;INTO AC1
00055'151404 INC 2,2,SZR ;SHIFTED 4 BITS?
00056'000775 JMP .-3 ;NO
00057'121000 MOV 1,0 ;SEND MSB
00060'004515 JSR IOXR ;TO 50/50
00061'020425 LDA 0,SWAP ;SEND LSB
00062'004513 JSR IOXR ;TO 50/50
00063'010422 ISZ ONE ;SKIP CHANNEL ONE ONLY
00064'000402 JMP .+2 ;FOR 50/50-ARIS
00065'060332 NIOP 32 ;SKIP CHANNEL ONE
00066'010423 ISZ CLMIT ;XFR DONE
00067'000761 JMP OUTD ;NO CONT
;YES FINISH

00070'006165 XFINI: JSR @TYPMS ;TYPE LAST
00071'000136 MSS4 ;MESSAGE
00072'000725 JMP CHARR+2 ;RETURN

;
00073'061566 SETC: DIBS 0,66 ;CLEAR AC(0), CLEAR I/O
00074'061466 DIB 0,66 ;CLEAR AC(0) ONLY
00075'126520 SUBZL 1,1 ;GENERATE +1
00076'066131 DOBS 1,31 ;BRING ANALYZER ON-LINE
00077'063030 DOC 0,DAC ;RESET ANALYZER ADDRESS
00100'020410 LDA 0,KIMIT ;RESET CHANNEL
00101'040410 STA 0,CLMIT ;COUNTER
00102'102000 ADC 0,0 ;GENERATE -1
00103'040402 STA 0,ONE ;SKIP FLAG
00104'001400 JMP 0,3 ;RETURN

;
00105'000000 ONE: 0 ;COUNTER
00106'000000 SWAP: 0 ;TEMPORARY STORE
00107'177774 M4: -4 ;MINUS FOUR
00110'170200 KIMIT: 170200 ;COUNTER FOR
00111'000000 CLMIT: 0 ;IGNORING LAST 128 CHANNELS

;
; I/O MESSAGES
MSS1: .TXT * TRANSFER 50/50 *

00112'052040
00113'040522
00114'051516
00115'042506
00116'020122
00117'030065
00120'032457
00121'020060
00122'000000

MSS2: .TXT *TO ARIS.*

00123'047524
00124'040440
00125'044522
00126'027123
00127'000000

MSS3: .TXT *FROM ARIS.*

00130'051106
00131'046517
00132'040440
00133'044522

```

0004 TRANS

00134'027123

00135'000000

MSS4: .TXT * XFR DONE.<15><12>*

00136'020040

00137'043130

00140'020122

00141'047504

00142'042516

00143'006456

00144'000012

;
; I/O DRIVERS;
; ANALYZER TO-FROM CPU

00145'063530	MOXFR:	SKPBZ DAC	; DAC BUSY?
00146'000777		JMP .-1	; NO, TRY AGAIN
00147'066030		DOB 1,DAC	; NO OUT DATA MSB
00150'061130		DOAS 0,DAC	; OUT DATA LSB, START
00151'063530		SKPBZ DAC	; ANALYZER BUSY?
00152'000777		JMP .-1	; NO TRY AGAIN
00153'060332		NIOP 32	; KICK ADDRESS
00154'001400		JMP 0,3	; RETURN

00155'060330	MIXFR:	NIOP 30	; DO MEMORY CYCLE
00156'063530		SKPBZ DAC	; MEMORY BUSY?
00157'000777		JMP .-1	; YES TRY AGAIN
00160'065430		DIB 1,DAC	; LOAD MSB
00161'060430		DIA 0,DAC	; LOAD LSB
00162'060332		NIOP 32	; KICK ADDRESS
00163'001400		JMP 0,3	; RETURN

;
;
;
; CPU TO-FROM NDNS

00164'063666	II XR:	SKPDN NDNS	; TEST I/O BUSY
00165'000777		JMP .-1	; NO, TRY AGAIN
00166'060466	XFR2:	DIA 0,NDNS	; YES XFR TO FROM CPR
00167'060160		NIOS NDNS	; SET I/O BUSY
00170'101220		MOVZR 0,0	; CORRECT FOR
00171'101200		MOVR 0,0	; HARDWARE
00172'101200		MOVR 0,0	; DESIGN SCREW UP
00173'101200		MOVR 0,0	
00174'001400		JMP 0,3	; RETURN

00175'103140	IOXR:	ADDOL 0,0	; SHIFT LEFT
00176'103140		ADDOL 0,0	; TO MATCH PDP-8
00177'100000		COM 0,0	; FLIP TO ZERO TRUE
00200'063666		SKPDN NDNS	; I/O DONE?
00201'000777		JMP .-1	; NO, TRY AGAIN
00202'061066		DOA 0,NDNS	; LOAD DATA REG OUT
00203'060166		NIOS NDNS	; DO IT TO IT
00204'001400		JMP 0,3	; RETURN

;
; END

0005	TRANS
CHARR	000015'
CLNIT	000111'
GETD	000023'
ICON	000020'
IXR	000164'
IOXR	000175'
KIMIT	000110'
M4	000107'
MIXFR	000155'
MOXFR	000145'
MSS1	000112'
MSS2	000123'
MSS3	000130'
MSS4	000136'
NDNS	000066
O	000000U
OCN	000045'
ONE	000105'
OUTD	000050'
SETC	000073'
SWAP	000106'
TRANS	000000'
XFINI	000070'
XFR2	000166'

APPENDIX C

INTERFACE PARTS LIST

This appendix presents the materials and parts used in designing the hardware interface.

<u>Quantity</u>	<u>Item</u>	<u>Source</u>	<u>Part Number/Value</u>
1 each	Universal Interface Board (UIB)	Data General Corporation	4040
1 each	IC Socket Option to UIB	Data General Corporation	4041
25 feet	I/O Bus Cable	Shop Built	NA
2 each	Hex Inverter	Stock	NC836 P
1 each	Hex Inverter	Stock	SN15836N
2 each	Dual 4 input OR	Stock	SN7425
2 each	Quad 2 input AND	Stock	SN7408
3 each	Quad 2 input NAND	Stock	MC858P
3 each	Resistor	Stock	180 ohm
1 each	Resistor	Stock	100 ohm
1 each	Capacitor	Stock	0.05 uf
1 each	Diode	Stock	1 watt
2 each	Connector (socket)	Stock	52 pin cannon
2 each	Connector (pin)	Stock	52 pin cannon

Figure 1

Nuclear Data Corporation 50/50 System

Cabinet racks above and to right of teletypewriter console contain peripheral memories, routing, display, interface, and hardwire control of four analyzers. Computer and paper tape photoreader are in cabinet to right of console. Detector systems are at left and right borders.

Figure 2

Tracor-Northern, Inc. 660 Systems

Cabinet racks on left and right each contain an analyzer, interface and computer. Systems peripherals include TI 733 ASR consoles and internal cassette tape drives. Center rack contains a Tracor-Northern Inc. 880 system for X-ray energy analysis.

GAMMA ENERGY ANALYSIS

Figure 3

Typical Ge(Li) Gamma Ray Spectrum of Mixed Isotopes

Figure 4

50/50 System Interface Unit

Interface unit contains photoreader power supply and bus connectors. Interprocessor cable and connector are at right of unit with the cable entering at the top.

Figure 5

NOVA 1220 Computer Backplane

The interprocessor cable and connector is shown at the upper left. Wiring from the connector to the proper interface board pins is shown at the upper wire wrap rows of the computer backplane.

Figure 6

General Purpose Interface Board

The lower half of the board contains standard supplied logic. User logic integrated circuit chips are located in the occupied sockets of the upper half of the board.

Figure 7

NOVA Board Locations

Lower slots of NOVA processor chassis contain central processor, memory and console interface. Highest slot position contains the interprocessor interface board.

NOTE: ALL PIN AND NOVA SIGNALS AS REFERENCED IN "HOW TO USE NOVA COMPUTERS" ON 4040 GENERAL PURPOSE INTERFACE BOARD WITH 4041 OPTEN. DISPLAYED LOGIC ADDED TO 4040 BOARD.

DEVICE	LOC	USED
SN15836N	7B	II
SN7425	8A, 9B	III
SN7408	7A, 8B	III
MC836P	6A, 9A	III
MC858P	3A, 4A, 5A	III

INTERPROCESSOR SIGNAL CONNECTIONS

4040 SIGNAL LABEL	NOVA REAR PANEL 52 PIN CANON CONNECTOR	NOVA REAR PANEL 52 PIN CANON CONNECTOR	4040 BOARD WIRE WRAP PIN NOS.
ACCO	3	A57	8A-12A IDAT0
AC0	4	A59	8-12 IDAT1
AC02	5	A49	9-11 IDAT2
AC03	6	A47	10-10A IDAT3
AC04	7	A76	1-22 IDAT4
AC05	8	A78	2-21 IDAT5
AC06	9	A77	6-20A IDAT6
AC07	10	A65	7-20 IDAT7
AC08	11	A84	2A-28A IDAT8
AC09	12	A86	3-28 IDAT9
AC10	13	A88	4-27 IDAT10
AC11	14	A92	5-26A IDAT11
BUS00	15	A61	34A
BUS01	16	A63	29
BUS02	17	A67	41
BUS03	18	A69	6A
BUS04	19	A71	48
BUS05	20	A73	49
BUS06	21	A75	49A
BUS07	22	A77	57
BUS08	23	A81	67
BUS09	24	A83	68A
BUS10	25	A85	68
BUS11	26	A87	69
INTREQ	27	B69	136
IOP1	28	B11	72A
IOP2	29	B12	72
IOP3	30	B15	76
IOP SKIP	31	B4	71
AC CLEAR	32	A89	70A
MB03	33	B31	82
MB04	34	B19	83
MB05	35	B23	84A
MB06	36	B27	93
MB07	37	B49	98A
MB08	38	B34	131
GAD	1/50

APPROVED FOR CONFORMANCE WITH DESIGN CRITERIA		DATE	U. S. ATOMIC ENERGY COMMISSION	
BY: [Signature]			RICHLAND OPERATIONS OFFICE	
FOR: [Signature]			Atlantic Richfield Hanford Company	
APPRO: [Signature]			Richland, Washington 99352	
REVISION		DATE	50/50 - ARIS	
DPTD APPD			INTERFACE LOGIC FOR	
CHECKED			NOVA 4040/1 BOARD	
DRAWN			SCALE	
CLASS FIELD			BLOS NO	
NOT RECD			222-S/200-W	
CLASSIFICATION			INDEX NO	
NONE			SK-2-22586	
DATE			SHEET NO	
			1	

REV NO	REV DATE	REV BY	REV FOR	DESCRIPTION	REV NO
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Figure 8

Diagram of Added Interface Logic to 4040/1 Board

*XRFER 50-50 TO ARIS
TRANSFER COMPLETE

*

T I TRANSFER 50/50 TO ARIS. XFR DONE.

A.

*XRFER 50-50 FROM ARIS
TRANSFER COMPLETE

*

T O TRANSFER 50/50 FROM ARIS. XFR DONE.

B.

Figure 9

System Console Messages

Part A shows the system console messages for data transfer from the 50/50 to the 660 system. Part B shows the opposite direction. Operator inputs are underlined.

Figure 10
System Block Diagram