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A Control System for Wind-Powered Generators

Gerald J. Kroth

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A CONTROL SYSTEM FOR WIND-POWERED GENERATORS

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ABSTRACT

A desirable control system for wind-powered generators would be versatile, automatic, reliable, and inexpensive. A small logic device consisting of one or a few integrated circuits which could meet these requirements is described. The system is versatile enough to be used over a wide range of situations which require fast, precise control.

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A CONTROL SYSTEM FOR WIND-POWERED GENERATORS

Introduction

In a system of wind-powered generators, a reliable yet inexpensive control system is desirable. Such a system would be completely automatic so it could be left unattended for long periods. It would respond to electrical representations of data such as bearing temperature, vibration, wind velocity, turbine velocity, torque, or any other pertinent data. It would respond by starting or stopping the turbine, controlling the loading, or sounding an alarm. A microprocessor-based controller capable of these functions is described in this report.

Background

A microprocessor is a logic device of one or a few integrated circuits (IC's). It can perform several functions (e.g., arithmetic logic, control) and respond to the results of some operations. In short, it is a programmable logic-state machine.

The F-8 microcomputer system was selected for this application as it is well suited for control functions. The main components of this F-8 system are the 3850 Central Processor Unit (CPU), the 3853 Static Memory Interface (SMI), and the 3861 Peripheral Input/Output Interface (PIO). Other components in the controller are the 2708 erasable, programmable, read-only memory (E PROM), a 4096 x 8 random access memory (RAM), and serial teletype interface circuits.

System Description

The system was designed to be suitable for general-purpose use. It is divided into seven functional blocks,

- CPU
- Static Memory Interface
- Program Storage
- I/O Interface
- Off-Board Signal Buffer/Drivers
- Teletype Interface, and
- 4K RAM,

as shown in Figure 1. The first six items are contained on a 9 x 10-1/2 in. printed circuit board. The 4K RAM is on a separate 2-1/2 x 5 in. wire wrap board.

Figure 1. Block Diagram of Control System

The CPU is the heart of the system. It performs most of the processing functions and provides control and timing for the rest of the system. It also contains two 8-bit bidirectional latched I/O ports. The CPU responds to interrupts from either the local timers or from external sources. The clock circuit logic is part of the CPU chip and can be timed by external crystal, R-C circuit, or from an external oscillator. The clock frequency must be between 1 and 2 MHz.

The SMI provides all logic required to interface up to 65,536 bytes of static memory. In response to control signals from the CPU, it generates the necessary signals to read from and write to static RAM devices. The SMI also contains a programmable interrupt timer as well as logic to service external interrupts.

The program storage is a static, 1024 x 8 ultraviolet-erasable, read-only memory device. It can store up to 1024 8-bit words of program data.

The I/O interface provides two 8-bit latched input/output ports, a programmable interrupt timer, and logic to service external interrupts.

The off-board drivers are buffered on all output, address, and control lines. They are capable of driving up to 20 TTL loads. The data bus is driven by bidirectional drivers which are controlled by the memory interface. They will drive up to 30 TTL loads.

Either RS-232 or current loop teletype interface is available. The option is made by installing jumpers on the board.

The 4K RAM is not located on the main computer but is a separate (optional) item. It consists of eight 4096 x 1 static memories in parallel. All address and data lines come from the main board. Some controls come from the computer and others are generated on the memory board.

There are provisions for mounting two 16-pin DIP sockets on the main board. These may be used for any additional circuitry that may be required by the user.

The system requires two power supplies with the following specifications:

+5 Vdc $\pm$ 5%, 1.0 A

$\pm$ 12 Vdc $\pm$ 5%, 0.1 A

The -5 volts used by the memories is regulated down from the -12V supply by an onboard regulator.

This system was designed to be usable in a variety of applications which can accommodate the particular three-chip F-8 system described here, and is presently being used in several other systems here at Sandia. One is being used to control, by program, the temperature in an electric furnace. The furnace is used to subject test specimens to time/temperature profiles over a long period. The profile can be programmed into the computer which then precisely controls the

temperature, using thermocouples for feedback. Another application is in a weapons arming sequence. It is also planned for use as a controller for positioning mirror arrays at the Solar Thermal Test Facility.

Sample Program Flow Diagram

The flow diagram (Figure 2) is for a program which will determine if wind speed is within set limits and respond accordingly. The input signal is the output of an anemometer, a square wave, its frequency being directly proportional to the wind velocity.

The first section of the program sets the interrupt timer, then compares the wind speed with a preset value by counting cycles. If a preset number of cycles is counted before the timer runs out, the wind speed is too high and the program goes to the OVERSPEED routine. If the timer runs out before the counter is full, the program is interrupted and is directed to the INT1 program.

The INT1 program is much the same as just described except that a timer interrupt from here means the wind is below a predetermined velocity, and the program is directed to the UNDER-SPEED routine. If the counter fills before the timer interrupt, the program goes to the RUN routine.

The OVERSPEED, UNDERSPEED, and RUN routines cause the computer to take the action required by the user for that particular status. This could be any number of actions and can be determined by the user at the time of creating the program.

a.

b.

Figure 2.

APPENDIX

Drawings and Sample Printout

[7:45:22]

WSRPT.F8

TITLE 'WIND SPEED CHECK. TEST ANEMOMETER OUTPUT'
* TO DETERMINE IF WITHIN LIMITS MINSP AND MAXSP.

*

	BASE	HEX	
	SYMBOL		
	XREF		
WS	EQU	H'05'	
INT1A	EQU	H'0030'	
INT1H	EQU	H'00'	
INT1L	EQU	H'30'	
INT2A	EQU	H'0070'	
INT2H	EQU	H'00'	
INT2L	EQU	H'70'	
TIM1	EQU	T'254'	254 = 3.95M SEC TIMER TIME
TIME	EQU	T'254'	
MXSP1	EQU	250	MAX SPEED COUNT IS 250
MXSP2	EQU	004	TIMES 4 FOR 1KHZ LIMIT.
MINSP	EQU	170	MIN. SPEED IS 170HZ
CTR0	EQU	0	
CTR1	EQU	1	
CTR2	EQU	2	

*

*

ORG	0	
CLR		
OUTS	0	CLEAR
OUTS	1	INPUT
OUTS	4	PORTS
OUTS	5	
OUTS	6	DISABLE 3851 INTERRUPTS

*

START	LI	TIM1	
	OUTS	H'0F'	LOAD TIMER WITH TIM1
	LIS	03	SET CONTROL FOR
	OUTS	H'0E'	TIMER INTERRUPT
BGIN	LI	INT1H	LOAD
	OUTS	H'0C'	INTERRUPT
	LI	INT1L	VECTOR
	OUTS	H'0D'	ADDRESS
	LI	253	NO. OF INTERRUPTS
	LR	CTR2,A	X 3.95 MS =1 SEC.

*

	LI	MXSP2	LOAD
	LR	CTR1,A	COUNTERS
LD1	LI	MXSP1	WITH MAXIMUM
	LR	CTR0,A	SPEED COUNT
	EI		
ZR01	INS	WS	
	BNZ	ZR01	WAIT FOR WS = LU
HI1	IN	WS	WAIT FOR
	BZ	HI1	RISING EDGE
ZR02	INS	WS	WAIT FOR
	BNZ	ZR02	FALLING EDGE
	DS	CTR0	COUNT
	BNZ	HI1	WS
	DS	CTR1	CYCLES
	BNZ	LD1	
	DI		IF PROGRAM GETS TO HERE, <<<<<<<<<
	BR	BGIN	OVERSPEED CONDITION EXISTS.

*

*

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